Homework Set 1 for Module 2

Due at the Beginning of Class (12:30 pm) on Wednesday, October 3

Name: _____ Class No: __ __ __ __ - __ Lab Div: ____

Signature: _____ Score: _____ / 120

1. [40 points] Assume a hypothetical microprocessor has the following A.C. timing specifications:

Description	Parameter	Value
Bus clock period	t_{CY}	100 ns
Address generation delay	t_{AD}	30 ns
Address hold time	t_{AH}	10 ns
Read setup time	t_{RS}	20 ns
Read hold time	t_{RH}	10 ns
Write data generation delay	t_{DD}	40 ns
Write hold time	t_{WH}	20 ns
Write float delay (after write hold)	t_{WZ}	10 ns

Consider interfacing this microprocessor to an SRAM chip that has the following specifications:

Description	Parameter	Value
Address access time	t_{AA}	20 ns min
Chip enable access time	t_{CE}	20 ns min
Output enable access time	t_{OE}	10 ns min
Output hold from CE' negation (or address change)	t_{OH}	0 ns min
Output float delay (after output hold)	t_{OZ}	30 ns max
Input data setup time	t_{IS}	20 ns min
Input data hold time	t_{IH}	10 ns min
Write pulse width	t_{WP}	10 ns min
Address valid prior to memory write	t_{AW}	20 ns min
Chip enable valid prior to memory write	t_{CW}	20 ns min

On the timing diagram worksheet for this problem (link on homework page), sketch a memory READ cycle followed immediately by a memory WRITE cycle. Assume 0 ns rise and fall times. For generating CE′, OE′, and WE′, assume a 10 ns PLD is used. Indicate when the READ and WRITE occur, and draw the "FedEx" lines for both the READ and WRITE cycles. <u>*Determine and label*</u> the read timing margin and write timing margin that is available on read and write cycles, respectively.

Grading:

- 24 points, sketch of timing chart (6 waveforms @ 4 points each)
- 3 points, identification of read timing margin
- 3 points, identification of write timing margin

2. [40 points] You are given a system design goal of running a `9S12C128` CPU (5 V) in *expanded narrow mode* with **one cycle of stretch** at the CPU's **maximum clock speed of 25 MHz** (i.e. $\mathbf{t_{CYC}}$ **= 40 ns**). Your job is to determine if an **`LC4032B-5T44C`** PLD used in conjunction with a **`7C199-10`** SRAM satisfies this constraint. Using the worksheet for this problem (link on homework page), draw a detailed read cycle timing diagram annotated with all pertinent CPU, PLD, and memory timing parameters (run the ispLever Performance Analyst to determine the "glue logic" propagation delay). Clearly identify the read timing margin available and the duration of bus fighting (if any) that occurs as a consequence of excessive SRAM read float delay. (Note: Assume rise and fall times are 0 ns, and that each ECLK half-cycle is exactly 20 ns)

   Grading:
   - 8 points, glue logic propagation delay determination
   - 16 points, waveform sketches and parameter annotation
   - 8 points, identification of read timing margin available
   - 8 points, identification of bus fighting/duration

3. [40 points] Determine the ***maximum clock speed*** a `9S12C128` CPU (5 V) can run at in *expanded narrow mode* **without stretch** if a **`7C199-10`** SRAM is used in conjunction with an `LC4032B-25T44C` PLD to implement the "glue" logic (round your result to the nearest one-tenth MHz). Note that your determination should include an SRAM **read timing margin of 10%.** Show your calculations, and draw a detailed, to-scale read timing diagram on the worksheet provided for this problem (link on homework page). Clearly identify the read timing margin available and the duration of bus fighting (if any) that occurs as a consequence of excessive SRAM read float delay. (Note: Assume rise and fall times are 0 ns; grading key on worksheet.)

   Grading:
   - 8 points, calculation of maximum bus clock speed
   - 8 points, glue logic propagation delay determination
   - 16 points, waveform sketches and parameter annotation
   - 8 points, identification of bus fighting/duration