ECE 362 Lab Verification / Evaluation Form

Experiment 5

Evaluation:

IMPORTANT! You must complete this experiment during your scheduled lab period. All work for this experiment must be demonstrated to and verified by your lab instructor *before the end* of your scheduled lab period.

STEP	DESCRIPTION	MAX	SCORE
1	Measuring a Port Pin (Thought Questions)	4	
2	Investigating the Sample Period (Thought Questions)	3	
3.1	Delay Loop Timing – Theoretical Calculations	4	
3.2	Delay Loop Timing - Measurements	4	
4.1	Observing Bus Signals – Fixing the Error	2	
4.2	Observing Bus Signals – Read Cycle Timing	4	
4.3	Observing Bus Signals – Write Cycle Timing	4	
	TOTAL	25	

Signature of Evaluator: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. *You will not receive credit for this lab experiment unless this statement is signed in the presence of your lab instructor.*

"In signing this statement, I hereby certify that the work on this experiment is my own and that I have not copied the work of any other student (past or present) while completing it. I understand that if I fail to honor this agreement, I will receive a score of ZERO and be subject to possible disciplinary action."

Printed Name: _____ Class No. __ __ __ __ - __

Signature: _____ Date: _____

Experiment 5: Microprocessor Bus Timing Analysis

Instructional Objectives:
- To learn how a logic analyzer can be used for logic and timing analysis
- To investigate delay routines, and the actual associated timing
- To observe and analyze microcontroller instruction timing on a machine cycle level

References:
- *Tektronix TLA 714 Reference Guide* – on Lab Experiments page
- *MC9S12C Family Data Sheet,* pp. 123-125 – on 9S12C References page
- *Multiplexed External Bus Interface (MEBI) Block User Guide* – on 9S12C References page
- Practice Homework for Module 2 – on Practice Homework page
- *HCS12 External Bus Design* (AN2287) – on Practice Homework page
- *Examples of External Bus Design* (AN2408) – on Practice Homework page
- Lecture Module 2-B

Prelab Preparation:
- Read the description of the lab exercises thoroughly
- Read the pages listed above in the *MC9S12C Family Data Sheet*
- Read the *Tektronix TLA 714 Reference Guide*
- Write the subroutine *delay* (Section 3.1 of this experiment)

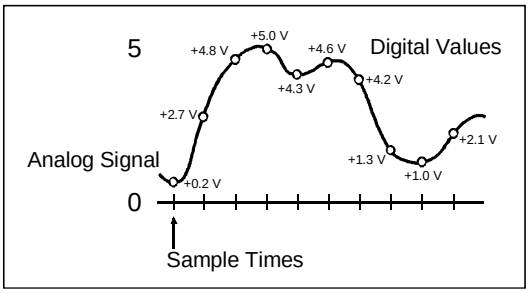
Introduction

Digital circuits are great, when they work. But we all know that they won't work the first time, and we must therefore have a development tool to use for designing and debugging digital circuits. Logic analyzers have long been the tool of choice, allowing us to see the logical level of signals at discrete points in time.

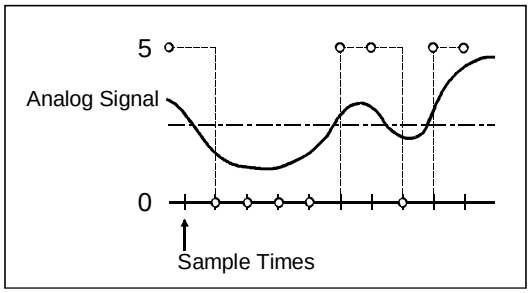
In this experiment we will learn how to use the logic analyzer. We will begin investigating the logic analyzer by making state changes to one of the HC(S)12's output pins and comparing the sampled waveforms recorded by the logic analyzer and digital oscilloscope. We will then measure the timing parameters of a square wave generated through the use of delay loops, and finally analyze the timing of internal read and write operations on the HC(S)12.

Measurement of Logic Signals

We will begin by investigating how the Tektronix TLA 714 measures logical signals. The TLA 714 combines a 2 channel digital oscilloscope (DSO) and 64-channel logic analyzer (LA). The DSO samples the input signal at a rate up to 250 MHz and displays the actual (sampled) waveform. The LA also samples the input signals, but for each sample determines whether the input voltage corresponds to logic "0" or logic "1", when compared against the threshold level for the selected logic family (i.e., TTL, CMOS, etc.). Thus the LA is used to show the logical state of a signal at discrete points in time and the DSO is used to show the actual voltage levels of a signal at discrete points in time.



Digital Oscilloscope Sampled Signal



Logic Analyzer Sampled Signal

The TLA 714 operates via highly sophisticated circuitry, some of which includes an embedded microprocessor and A/D assembly to do the real-time input data capture, and a single board computer to allow us to view and manipulate the data using Windows. The DSO and LA are controlled through a program called TLA 700.

Let's begin by loading a system configuration file into the TLA 714. In TLA 700, go to `File→Load System` and load the file **default.tla** *from the TLA desktop.* The system setup is pre-configured for this exercise.

Now take a few minutes to read through the *TLA 700 Reference Guide* while experimenting with each window to understand the basic functions and configurations. After you have a thorough understanding of how to use TLA 700, reload the system file **default.tla**.

Step 1. Measuring a Port Pin

Download the file **la_ex12.asm** from the course web site. Compile and load this file into the HC(S)12 target system. Notice that this program will change the state of Pin 0 of Port A (PA0) on the HC(S)12 from 0 to 1, and then back to 0 again. We will record and analyze the transitions using the TLA 714.

First, we must set up the TLA 714 to capture the correct data. Go to the Trigger Window inside TLA 700 and click on the **If/Then** button. Select 'Anything' under the **If** menu, and select 'Go To' 'State 2' under the **Then** menu. Click OK. Back in the Trigger Window click on the **If/Then** button in State 2. Select 'Channel PA0' 'Goes' 'High' under the **If** menu and select 'Trigger All Modules' under the **Then** menu. This will cause the LA Trigger Event to be the rising edge of PA0. Next open the DSO Setup Window and click on the Trigger tab. Make sure that the Event Type is set to 'Wait for System Trigger'. This will cause the DSO to trigger at the same time as the LA.

Now that the system is configured correctly, click on the RUN button in the main window. This will cause the TLA 714 to wait for the rising edge on PA0. Execute the program on the HC(S)12. Notice that the TLA 714 will acquire data for a certain length of time after the event, and then stop. Also notice the waveforms generated in the Waveform Window: there should be one waveform for the DSO data and one for the LA data. Go to the Waveform Window and zoom in on the PA0 rising edge transition point.

Thought Questions:

1. After you press the RUN button, but before the program executed on the HC(S)12, was the TLA 714 acquiring data? Why or why not?
2. Why do the DSO and LA plots show the signal changing at different times?
3. For the DSO data, why doesn't the transition look "square"?
4. What are the Sample Periods for the DSO and LA?
5. Why is there less DSO data than LA data?
6. For what total length of time did the LA record samples? (HINT: look at the Listing Window)
7. For the LA data, how many of the samples were stored before the "event" occurred? What percentage of the total number of samples does that correspond to?

Step 2. Investigating the Sample Period

Next we will investigate the role of Clocking in data acquisition. Go to the LA Setup Window and change Clocking to 50 ns. Leave the DSO sampling rate unchanged. Now repeat the exercise in Step 1.

Thought Questions:

1. For what total length of time did the LA record samples now?
2. Why is the total length of time recorded different than before?
3. How could you have predicted the result found in Question 1?
4. Why is it best to keep the DSO Sample Period relatively small?

Step 3. Delay Loop Timing

For this part of the experiment we will be investigating the timing of delay loops. Download the skeleton file **la_ex3.asm** from the course web site. You will be writing the subroutine **delay**, which simply produces a delay of 6 ms. The main program repeatedly toggles PA0 after calling **delay**, effectively creating a square wave on PA0.

3.1. Theoretical Calculations

Write the subroutine **delay**.

1. Calculate the total period length of the square wave (rising edge to rising edge). Show your calculations in the space provided.

2. Calculate the duty cycle of the square wave. The duty cycle is defined as the percentage of time that the waveform is in its asserted state (i.e., if a signal has a period of 10 ns and is asserted high for 4 ns, it has a 40% duty cycle).

3.2. Delay Loop Measurement

Set the Sample Period of the LA to 50 µs. This will allow you to record several periods of the square wave in the Waveform Window. Change the Sampling Period of the DSO to allow you to record one full period of the square wave (calculate this before trying it out). Execute your program and acquire both LA and DSO data. Measure the period and duty cycle for both the DSO and LA data and compare your measurements and theoretical calculations. Indicate your results in the table below. In addition, make a printout of the Waveform Window, showing at least one full period of DSO and LA data. Annotate your printout by hand with the measured period and duty cycle values.

	Period (ms)	Duty Cycle
Theoretical Calculation		
Measured LA Data		
Measured DSO Data		

Step 4. Observing Bus Signals

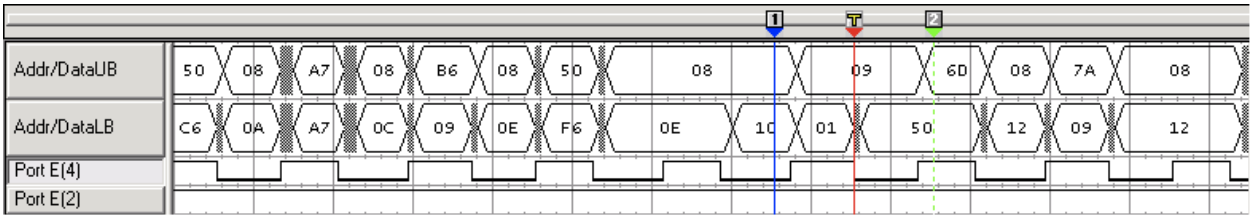
In this section we will investigate the internal timing parameters of the HC(S)12 address and data busses. As mentioned in class, by default the HC(S)12 operates in (Normal) Single Chip Mode. However, in order to interface an external memory component to the HC(S)12, it must operate in Expanded Wide Mode or Expanded Narrow Mode. Though we will not interface external memory, we will operate the HC(S)12 in Special Expanded Wide Mode with *internal visibility turned on.* This will allow the internal bus activity to be seen on Ports A, B, and E.

Step 4.1. Observing Bus Signals – Example

In this example, the following instructions were executed and the internal bus activity was monitored:

Instructions	Listing file output (.LST)

`nop`
`nop`
`ldaa $0950`
`ldab $0901`
`staa $0902`
	`080A [01] A7`
	`080B [01] A7`
	`080C [03] B60950`
	`080F [03] F60901`
	`0812 [03] 7A0902`



Addr/DataUB *is the upper byte of the address/data bus,* ***Addr/DataLB*** *is the lower byte of the address/data bus,* ***Port E(2)*** *is the read/write signal, and* ***Port E(4)*** *is the E-Clock.*

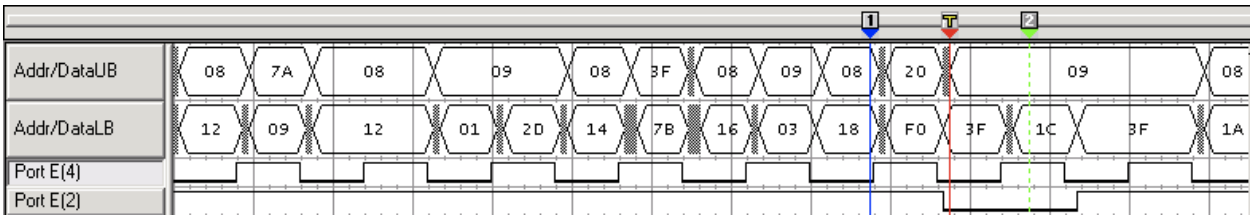
A trigger was setup to trigger the logic analyzer module when `$0950` shows up on the Addr/Data bus. The microcontroller fetches two bytes at a time by putting the address on the bus when the E-clock is low. The first fetch occurs when addr/data bus has the address (`$0950`) and it fetches (`$6D`), which was the value at memory address ($0950). The microcontroller fetches more instructions and the execution of the first two instructions doesn't show on the addr/data bus because they do NOT access any memory.

Note that the load instruction is read from location `$080C` a few cycles before it is executed. This is due to microprocessor pipelining. Pipelining is a method used to create a more efficient processor by doing multiple things simultaneously. As the processor is executing previous instructions, it fetches a few instructions ahead.

In the next example, the following instructions were executed and the internal bus activity was monitored:

Instructions	Listing file output (.LST)

`staa $093F`
`stab $0903`
`bra #$F0`
	`0812 [03] 7A093F`
	`0815 [03] 7B0903`
	`0818 [03] 20F0`



After the **`staa $093F`** *instruction is fetched, it is executed and the address* **`$093F`** *appears on the addr/data bus and* **`$1C`** *is written to the memory (R/W or Port E(2) is low).*

4.2. Observing Bus Signals – Fixing the Error

Step (a):
Load the **bus.tla** system file *from the TLA desktop*. This will configure the TLA 714 to capture the bus activity. Take a few minutes to make sure that your system is set up correctly. Trace the wires from the port pins into the TLA 714 and compare the signals (as named in the LA Setup Window) with the chart on the last page of this experiment. To facilitate an active learning environment, one of the signals has been named incorrectly in the **bus.tla** file. *Find this error and correct it.* **DO NOT change the wiring configuration on the EVB.**

Notice in the TLA 700 system configuration that the HC(S)12 is utilizing a 16-bit multiplexed bus. For all memory read and write operations the address is on the bus during the first half of the cycle, while the data is allowed on the bus during the second half of the cycle. In order to interface an external memory component to the HC(S)12, we would have to make use of a *transparent latch*, to make the address and data available at the same time. For read and write operations to internal memory, the HC(S)12 follows a similar process (latching), though the bus signals are not externally viewable. As a result, for read and write operations to internal memory we will only have access to the E Clock, R/W, Data, and Address lines. However, these signals provide a large amount of information about the HC(S)12 internal timing.

Step (b):
Download the file **la_ex4.asm** from the course web site. Compile and load this file into the HC(S)12 target system. Notice that the file contains startup code used to place the HC(S)12 into **Special Expanded Wide Mode**, followed by four load and store (read and write) instructions. After assembling the code, identify the address (using the **la_ex4.lst** file) that will be used to setup the trigger of the logic analyzer.

Step (c):
Set up the TLA 714 so that it will capture data when a certain word value shows up on the addr/data bus. Make sure to setup the trigger to trigger on the load and store instructions, not the startup code.

Step (d):
Execute the program and acquire the corresponding data into the TLA 714. Make a printout displaying the fetch and execute cycles for the four load and store instructions. Clearly indicate on your printout the fetch cycles and their corresponding execute cycles. In addition, make a printout of the execute cycle for each type of instruction (i.e., one of the load and one of the store). Measure the parameters listed below for the read and write operations.

4.2. Read Cycle

Measure the values for the following parameters:

1. t_{CYC} = _____ ns
2. t_{AD} = _____ ns
3. t_{AH} = _____ ns

Identify a fetch cycle and compare the addr/data bus values with the listing file. Also identify a memory read operation (execution of a load operation) and compare the addr/data bus values with the listing file.

4.3. Write Cycle

Measure the values for the following parameters:

1. t_{CYC} = _____ ns
2. t_{AD} = _____ ns
3. t_{AH} = _____ ns
4. t_{DD} = _____ ns (write data delay time)

Identify a write cycle and compare the addr/data bus values with the listing file.

Pin	LA Probe	Name
PA7	A0(7)	Addr/Data(15)
PA6	A0(6)	Addr/Data(14)
PA5	A0(5)	Addr/Data(13)
PA4	A0(4)	Addr/Data(12)
PA3	A0(3)	Addr/Data(11)
PA2	A0(2)	Addr/Data(10)
PA1	A0(1)	Addr/Data(9)
PA0	A0(0)	Addr/Data(8)
PB7	A1(7)	Addr/Data(7)
PB6	A1(6)	Addr/Data(6)
PB5	A1(5)	Addr/Data(5)
PB4	A1(4)	Addr/Data(4)
PB3	A1(3)	Addr/Data(3)
PB2	A1(2)	Addr/Data(2)
PB1	A1(1)	Addr/Data(1)
PB0	A1(0)	Addr/Data(0)
PE4	A2(4)	E Clk
PE2	A2(2)	R/W

HC(S)12 Internal Bus Signals

