C.3 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure C-5** with the actual timing values shown on table Table C-4. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

C.3.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

Figure C-5 General External Bus Timing

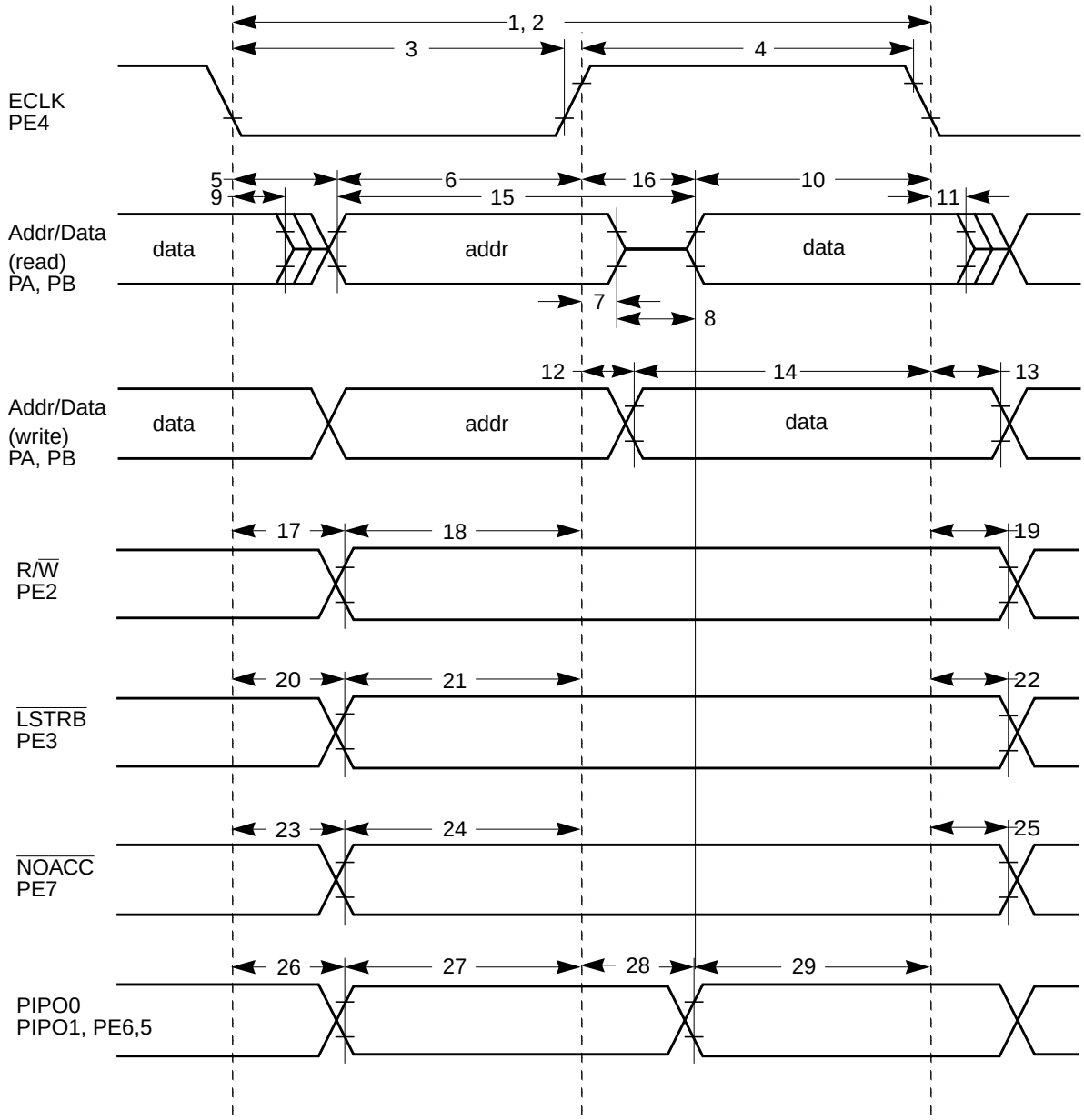

Table C-4 Expanded Bus Timing Characteristics (5V Range)

Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40˚C to +140˚C, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time(1) (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Read/write delay time	t_{RWD}			7	ns
18	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
19	D	Read/write hold time	t_{RWH}	2			ns
20	D	Low strobe delay time	t_{LSD}			7	ns
21	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
22	D	Low strobe hold time	t_{LSH}	2			ns
23	D	NOACC strobe delay time	t_{NOD}			7	ns
24	D	NOACC valid time to E rise (PW_{EL}–t_{LSD})	t_{NOV}	14			ns
25	D	NOACC hold time	t_{NOH}	2			ns
26	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
27	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns
28	D	IPIPO[1:0] delay time(1) (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
29	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Table C-5 Expanded Bus Timing Characteristics (3.3V Range)

Conditions are VDDX=3.3V+/-10%, Junction Temperature -40˚C to +140˚C, C_{LOAD} = 50pF

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Frequency of operation (E-clock)	f_o	0		16.0	MHz
2	D	Cycle time	t_{cyc}	62.5			ns
3	D	Pulse width, E low	PW_{EL}	30			ns
4	D	Pulse width, E high[1]	PW_{EH}	30			ns
5	D	Address delay time	t_{AD}			16	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	16			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	15			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			15	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	15			ns
15	D	Address access time(1)	t_{ACCA}	29			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	15			ns
17	D	Read/write delay time	t_{RWD}			14	ns
18	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	16			ns
19	D	Read/write hold time	t_{RWH}	2			ns
20	D	Low strobe delay time	t_{LSD}			14	ns
21	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	16			ns
22	D	Low strobe hold time	t_{LSH}	2			ns
23	D	NOACC strobe delay time	t_{NOD}			14	ns
24	D	NOACC valid time to E rise (PW_{EL}–t_{LSD})	t_{NOV}	16			ns
25	D	NOACC hold time	t_{NOH}	2			ns
26	D	IPIPO[1:0] delay time	t_{P0D}	2		14	ns
27	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	16			ns
28	D	IPIPO[1:0] delay time(1)	t_{P1D}	2		25	ns
29	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.