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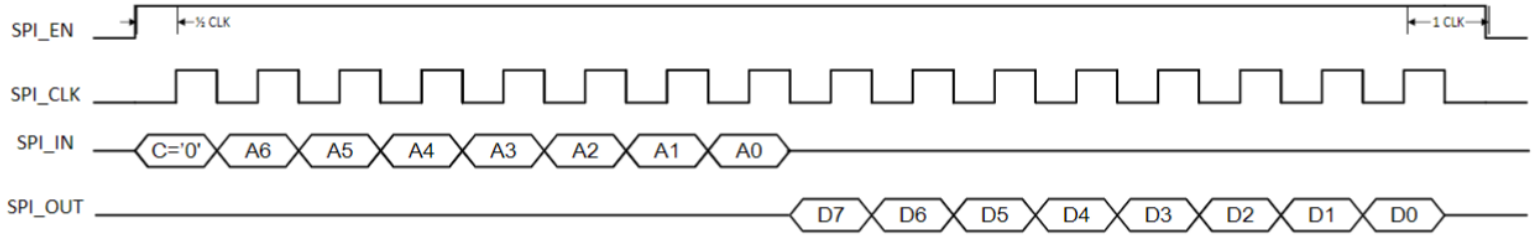
1. What is the frequency range for the imager's master clock signal?
   10-40MHz
2. What is the maximum frequency for the SPI clock signal?
   40MHz
3. Draw the SPI read block diagram and describe how would you use this information to develop the FSM in Verilog?

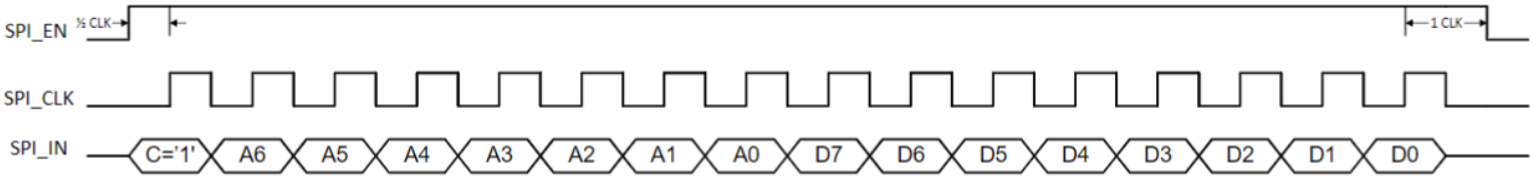


(1) Change SPI_EN into high when making the control bit on the SPI_IN pin '0'. And keep it in the whole reading part of the FSM

(2) Send the address of the register being read out immediately after this control bit. Launch each bit of address on the falling edge of the SPI_CLK.

(3) After the sending of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. So we should receive data on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first.

4. Draw the SPI write block diagram and describe how would you use this information to develop the FSM in Verilog?



(1) Change SPI_EN into high when making the control bit on the SPI_IN pin '1'. And keep it in the whole writing part of the FSM

(2) The data is sampled by the CMV300 on the rising edge of the SPI_CLK. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. SPI_EN has to remain high for 1clock period after the last data bit is sampled.

(3) One write action contains 16 data bits: one control bit, 7 address bits and 8 data bits. When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time.