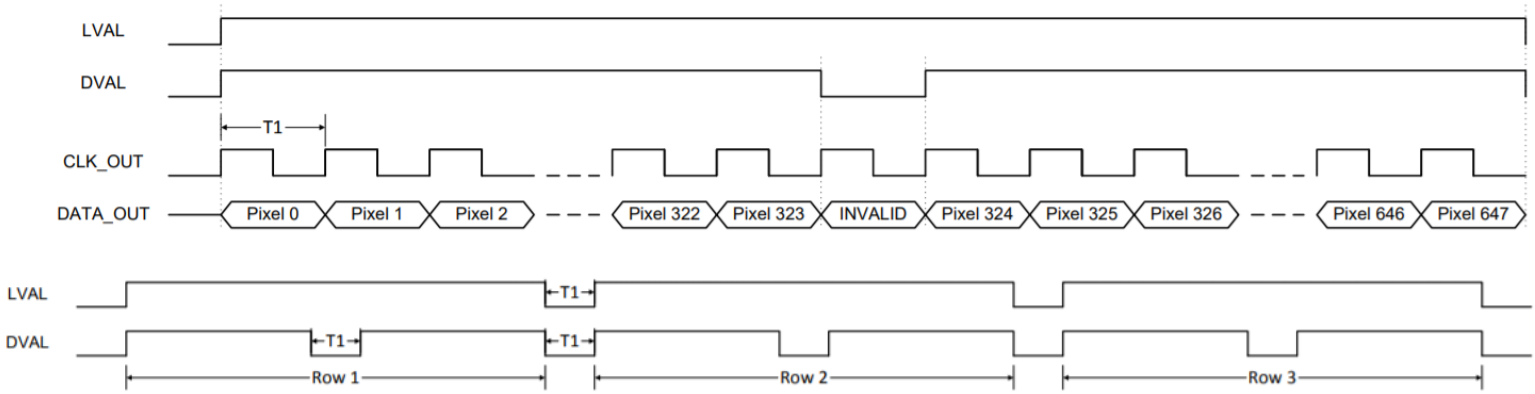
Name: Junzhe Wu Net id: Junzhew3

1. Look over the online documentation for front panel. What is maximum data transfer rates when using Block Throttled Pipe Out?
   320 MB/s (USB 3.0)
2. Describe the output signals from the image sensor necessary to acquire an image in parallel read out mode?
   LVAL: Indicates validity of the readout of a row
   DVAL: Indicates valid pixel data on the outputs
   CLK_OUT: It is advised to sample the parallel output data on the falling edge of the CLK_OUT
   DATA_OUT: Carries the pixel data from the image sensor.
3. Draw a block diagram of the FSM that will enable you to read a single frame of data from the image sensor. Summarize how would you implement the FSM in Verilog.



(1) Keep LVAL high when reading one row's pixel data and keep it low between the reading of two row's pixel data for T1 time.

(2) Keep DVAL low between the reading of two row's pixel data and also keep it low between the reading of pixel 323 and 324.