Processor Architecture

Tomasulo Algorithm

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Tomasulo Algorithm

Tomasulo's algorithm is a hardware algorithm designed for dynamic scheduling of instructions in an out-of-order execution machine. The algorithm was designed by Robert tomasulo at IBM in 1967 for the IBM 360/91.

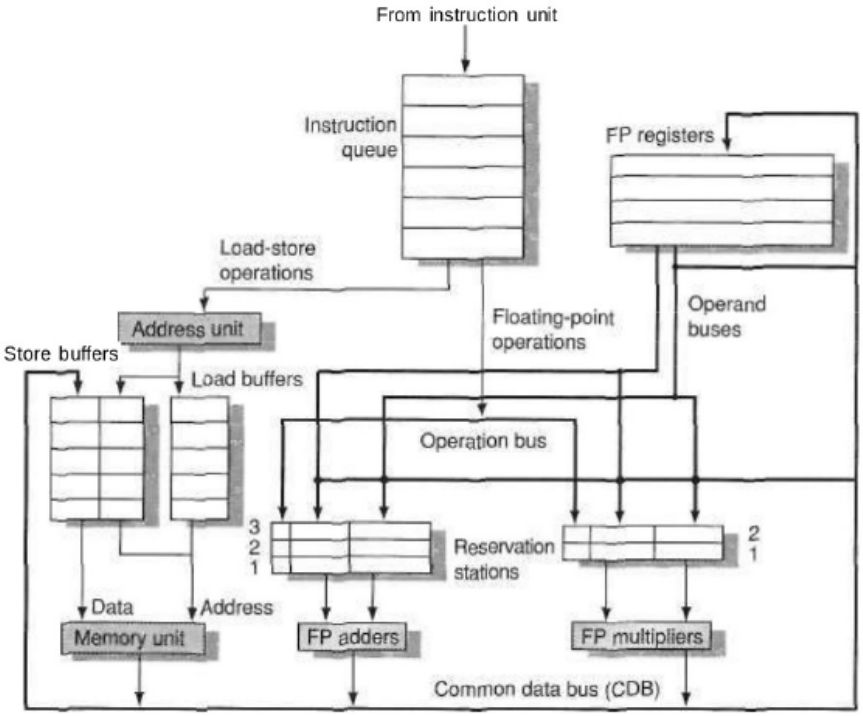

Figure 1: IBM 360/91

The essential components involved in the tomasulo algorithm are:

Instruction queue

Instructions are fetched from the instruction memory and temporarily stored in the instruction queue. Instructions are dispatched from this queue one by one as the execution unit gets free.

Reservation Stations

Register allocation table

Reorder buffer

ALU

Common Data bus

Architecture

The processor on which we are simulating the Tomasulo algorithm is an 8-bit processor.

Verilog Implementation

Observation

Appendix

References

Wikipedia, Tomasulo Algorithm