ADC BASICS:

In electronics, an analog-to-digital converter (ADC, A/D, A–D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal. An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. Typically the digital output is a two's complement binary number that is proportional to the input, but there are other possibilities. There are several ADC architectures. Due to the complexity and the need for precisely matched components, all but the most specialized ADCs are implemented as integrated circuits (ICs).

An analog-to-digital converter (abbreviated ADC) is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form. The TSC_ADC_SS (Touchscreen_ADC_subsystem) is an 8 channel general purpose ADC, with optional support for interleaving Touch Screen conversions. The TSC_ADC_SS can be used and configured in one of the following application options:

8 general purpose ADC channels

4 wire TS, with 4 general purpose ADC channels

5 wire TS, with 3 general purpose ADC channels

ADC used is 12 bit SAR ADC with a sample rate of 200 KSPS (Kilo Samples Per Second). The ADC samples the analog signal when "start of conversion" signal is high and continues sampling 1 clock cycle after the falling edge. It captures the signal at the end of sampling period and starts conversion. It uses 12 clock cycles to digitize the sampled input; then an "end of conversion" signal is enabled high indicating that the digital data ADCOUT<11:0> is ready for SW to consume. A new conversion cycle can be initiated after the previous data is read. Please note that the ADC output is positive binary weighted data.

Pin Type Description:

AN[7:0] I Analog Input

VREFN Power Analog Reference Input Negative Terminal

VREFP Power Analog Reference Input Positive Terminal

Functional Description:

Before enabling the TSC_ADC_SS module, the user must first program the Step Configuration registers in order to configure a channel input to be sampled. There are 16 programmable Step Configuration registers which are used by the sequencer to control which switches to turn on or off (inputs to the AFE) which channel to sample, and which mode to use (hardware-triggered or software-enabled, one-shot or continuous, averaging, where to save the FIFO data, and more).

Hardware-Synchronized or Software-Enabled:

The user can control the start behavior of each step by deciding if a channel should be sampled immediately (software-enabled) after it is enabled, or if the channel should wait for a hardware (HW) event to occur first (a HW event must either be mapped to the touch screen PEN event or mapped to the HW event input signal, but not both). Each step can be configured independently using the STEPCONFIGx register.

Open Delay and Sample Delay:

The user can program the delay between driving the inputs to the AFE and the time to send the start of conversion signal. This delay can be used to allow the voltages to stabilize on the touch screen panel before sampling. This delay is called “open delay” and can also be programmed to zero. The user also has control of the sampling time (width of the start of conversion signal) to the AFE which is called the “sample delay”. The open delay and sample delay for each step can be independently configured using the STEPDELAYx register.

Averaging of Samples (1, 2, 4, 8, and 16) Each step has the capability to average the sampled data. The valid averaging options are 1 (no average),

2, 4, 8, and 16. If averaging is turned on, then the channel is immediately sampled again (up to 16 times) and final averaged sample data is stored in the FIFO. Each step can be independently configured using the STEPCONFIGx registers.

One-Shot (Single) or Continuous Mode :

When the sequencer finishes cycling through all the enabled steps, the user can decide if the sequencer should stop (one-shot), or loop back and schedule the step again (continuous). If one-shot mode is selected, the sequencer will take care of disabling the step enable bit after the conversion. If continuous mode is selected, it is the software's responsibility to turn off the step enable bit.

Analog Front End (AFE) Functional Block Diagram:

The AFE features are listed below, and some are controlled by the TSC_ADC_SS:

• 12-bit ADC

• Sampling rate can be as fast as every 15 ADC clock cycles

• Support for internal ADC clock divider logic

• Support for configuring the delay between samples also the sampling time

Operational Modes:

The sequencer is completely controlled by software and behaves accordingly to how the Step Registers are programmed. A step is the general term for sampling a channel input. It is defined by the programmer who decides which input values to send to the AFE as well as how and when to sample a channel input. The choices for each step can all be programmed using the STEPCONFIGx registers.

A step requires using these registers:

• STEPENABLE: Enables or disables the step

• STEPCONFIGx: Controls the input values to the ADC (the reference voltages, the pull up/down transistor biasing, which input channel to sample, differential control, HW synchronized or SW enabled, averaging, and which FIFO group to save the data).

• STEPDELAYx: Controls the Open Delay (the time between driving the AFE inputs until sending the SOC signal to the AFE), and also controls the Sample Delay (the time for the ADC to sample the input signal)