



# IN1006 Systems Architecture (PRD1 A 2022/23)

<b>爺</b>   My Moodle   <u>IN1</u>	⚠   My Moodle   IN1006_PRD1_A_2022-23   COURSEWORK 1: Weekly Assessed Quiz   Quiz 6_ Weekly Assessed Quiz 2022		
Started on Thursd	lay, 8 December 2022, 5:47 PM		
State Finishe	ed .		
Completed on Thursd	Completed on Thursday, 8 December 2022, 6:00 PM		
Time taken 12 min	s 44 secs		
Grade 10.00 (	out of 10.00 (100%)		
Question 1			
Correct			
Mark 1.00 out of 1.00			
Which of the following is a	a pair of non-volatile memories?		
Select one:			
O a. DRAM and Flash			
O b. EPROM and DRAM	1		
O c. DRAM and SRAM			
<ul><li>d. ROM and Flash</li></ul>		<b>~</b>	
O e. SRAM and EEPROI	М		
answer.	the question are SRAM, VRAM and DRAM, The only option that does not contain any of them is the		
The correct answer is: RO	M and Flash		
Question 2			
Correct			
Mark 1.00 out of 1.00			
Which of the following sta	stements about the different types of memory that can be found in a computer is correct?		
oa. A computer can o	perate without a RAM.		
O b. A computer can o	perate without a ROM.		
O c. A computer canno	ot operate without virtual memory.		
O d. A computer must	always have a full memory hierarchy with L1 cache, L2 cache, RAM and secondary memory.		
e. A computer can o	perate without a cache and secondary memory.	<b>~</b>	
Your answer is correct.			
The correct answer is:			

A computer can operate without a cache and secondary memory.

Question 3
Correct
Mark 1.00 out of 1.00

Assume a computer having a main memory of  $2^{32}$  bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address 000063FA<sub>16</sub> map?

#### Select one:

- O a. Block 1024
- O b. Block 573
- O c. Block 1
- o d. Block 799
- O e. Block 64
- Of. Don't know/no answer

As the computer has a memory with  $2^{32}$  bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits (1024 =  $2^{10}$ ), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 =  $2^5$ ) or, equivalently, the offset (O) field must be 5 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

TAG (32 <sup>nd</sup> to 16 <sup>th</sup>) BLOCK (15 <sup>th</sup>to 6 <sup>th</sup>bit) OFFSET (5 <sup>th</sup>to 1 <sup>th</sup>tit)

The hexadecimal address  $000063FA_{16}$  corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0110 0011 1111 1010

And if we convert 110 0011 111<sub>bin</sub> to decimal, we get 799<sub>dec</sub> So the given address will map to block 799 in cache.

The correct answer is: Block 799

Question 4
Correct
Mark 1.00 out of 1.00

Assume a computer having a main memory of  $2^{32}$  bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address  $000063FA_{16}$  map?

#### Select one:

- a. Block 399
- O b. Block 512
- O c. Block 201
- O d. Don't know/no answer
- O e. Block 124
- Of. Block 58

As the computer has a memory with  $2^{32}$  bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits  $(512 = 2^9)$ , so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ( $64 = 2^6$ ) or, equivalently, the offset (O) field must be 6 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32 <sup>nd</sup> to 16 <sup>th</sup>) BLOCK (15 <sup>th</sup>to 7 <sup>th</sup>bit) OFFSET (6 <sup>th</sup>to 1 <sup>th</sup>tit)

The hexadecimal address  $000063FA_{16}$  corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0110 0011 1111 1010

And if we convert 110001111<sub>bin</sub> to decimal, we get 399<sub>dec</sub> So the given address will map to block 399 in cache.

The correct answer is: Block 399

Correct			
Mark 1.00	out of 1.00		
Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 64 blocks where each block contains 16 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.			
Select	one:		
O a.	T= 16 , O= 8 and B = 8		
	T= 28 , O= 2 and B = 2		
	T= 22 , O= 4 and B = 6		
O d.	Don't know/no answer		
O e.	T= 8 , O= 16 and B = 8		
O f.	T= 24 , O= 4 and B = 4		
	computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 Thus, the total size of the tag, block and offset (TBO) fields is 32.		
As the	cache has 64 blocks, it can be indexed with 6 bits $(64 = 2^6)$ . So the size of the block field (B) is 6.		
As eac	h block has 16 bytes, it can be indexed with 4 bits (16 = $2^4$ ). So the size of the offset field (B) is 4.		
Thus ,	the tag (T) field is: TBO - B - O = 32 - 6 - 4 = 22.		
The co	rrect answer is: T= 22 , O= 4 and B = 6		
Question Correct			
	out of 1.00		
IVIAIR 1.00			
Which	of the following <i>best</i> describes why a memory hierarchy is needed?		
Select	one:		
O a.	SRAM is cheaper than DRAM per unit of memory.		
O b.	Don't know/no answer		
O c.	It is useful to be able to exceed physical memory limits.		
O d.	Processor speeds have increased faster than SRAM speeds.		
O e.	DRAM is cheaper than SRAM per unit of memory.		
<ul><li>f.</li></ul>	Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.		

 ${\sf Question}\, 5$ 

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

Question 7
Correct
Mark 1.00 out of 1.00

Assume a computer having a cache whose block size is 1024 bytes. Which of the following programs would lead the most effective use of the sequential locality?

#### Select one:

- a. A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points.
- ~

- b. A program that reads 2000 data points from a file and prints them to the computer terminal.
- Oc. A program with that computes the sum of 9999 numbers stored in a file.
- Od. A program with 900 instructions that processes an array with 300 data points.
- e. A program with 50 instructions that reads and transforms data in a file which can grow dynamically.
- Of. Do know the answer.

Sequential locality refers to the common feature of programs that instructions and data tend to be accessed sequentially.

As the block size of the computer is 1024 bytes only the program with the 800 instructions processing the array of 200 data points would be possible to fit in one block and thus execute as many times as required without the need to transfer further data and/or instructions from the main memory to the cache. The existence of a loop in this program would not affect sequential locality either since the jump from the last to the first instruction of the loop in the program would not cause any transfers to and from the main memory because all instructions of the program can fit in the cache and would be loaded at the start of the program's execution.

All other options given may lead to data/instructions transfers between cache and the main memory thus violating sequential locality.

The correct answer is: A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points.

Question 8

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 32 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

### Select one:

- $\bigcirc$  a. T= 28, O= 2 and B = 2
- O b. T= 16, O= 8 and B = 8
- $\odot$  c. T= 22, O= 5 and B = 5
- Od. Don't know/no answer
- O e. T= 8, O= 16 and B = 8
- $\bigcirc$  f. T= 24, O= 4 and B = 4

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them  $(4,294,967,296 \pm 2^{32})$ . Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 32 blocks, it can be indexed with 5 bits (32 =  $2^5$ ), so the size of the block (B) field is 5 bits.

As each block has 32 bytes, so it can be indexed with 5 bits ( $32 = 2^5$ ) or, equivalently, the offset (O) field must be 5 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 5 - 5 = 22.

The correct answer is: T=22, O=5 and B=5

Question 9

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 128 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

## Select one:

- O a. T= 8, O= 16 and B = 8
- O b. T= 24, O= 4 and B = 4
- O c. T= 16, O= 8 and B = 8
- $\odot$  d. T= 20, O= 5 and B = 7
- O e. Don't know/no answer
- O f. T= 28 , O= 2 and B = 2

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 =  $2^{32}$ ). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 128 blocks, it can be indexed with 7 bits (128 =  $2^{7}$ ), so the size of the block (B) field is 7 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 =  $2^5$ ) or, equivalently, the offset (O) field must be 5 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 7 - 5 = 20.

The correct answer is: T=20, O=5 and B=7

Suppose we have a byte-addressable computer using direct mapping with 16-bit main each block contains 8 bytes, determine the size of the tag field.	memory addresses and 16 blocks of cache. If
Select one:	
<ul><li>a. 9</li></ul>	✓
O b. 8	
O c. Don't know/no answer	
O d. 4	
O e. 16	
O f. 5	
The total size of the tag, block and offset fields is 16. 16 blocks of cache can be indexed with 4 bits $(32 = 2^4)$ , so block needs 4 bits.	
Each block has 8 bytes so it can be indexed with 3 bits (8=2 <sup>3</sup> ); thus 3 bits are needed for byte within a block.	or the offset to determine the address of each
Finally, the tag field is: $16 - 4 - 3 = 9$ .	
The correct answer is: 9	
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 $\begin{array}{c} \text{Question 10} \\ \text{Correct} \end{array}$ 

Mark 1.00 out of 1.00

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