# IN1006 Systems Architecture (PRD1 A 2022/23)



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| **State** | Finished |
| **Completed on** | Thursday, 8 December 2022, 4:41 PM |
| **Time taken** | 14 mins 29 secs |
| **Grade** | **10.00** out of 10.00 (**100**%) |

Question **1**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of $2^{32}$ bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000053AA_{16}$ map?

Select one:

- a. Block 334 ✔
- b. Block 512
- c. Block 201
- d. Block 58
- e. Don't know/no answer
- f. Block 124

As the computer has a memory with $2^{32}$ bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

**TAG ($32^{nd}$ to $16^{th}$) BLOCK ($15^{th}$ to $7^{th}$ bit) OFFSET ($6^{th}$ to $1^{st}$ bit)**

The hexadecimal address $000053AA_{16}$ corresponds to the binary address:

**0000 0000 0000 0000 0101 0011 1010 1010**

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**101 0011 10**10 1010

And if we convert $101001110_{bin}$ to decimal, we get $334_{dec}$ So the given address will map to block 334 in cache.

The correct answer is: Block 334

Question **2**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 64 blocks where each block contains 16 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 24 , O= 4 and B = 4
- b. T= 16 , O= 8 and B = 8
- c. T= 22 , O= 4 and B = 6 ✔
- d. T= 28 , O= 2 and B = 2
- e. Don't know/no answer
- f. T= 8 , O= 16 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = $2^{32}$). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 64 blocks, it can be indexed with 6 bits (64 = $2^6$). So the size of the block field (B) is 6.

As each block has 16 bytes, it can be indexed with 4 bits (16 = $2^4$). So the size of the offset field (B) is 4.

Thus , the tag (T) field is: TBO - B - O = 32 - 6 - 4 = 22.

The correct answer is: T= 22 , O= 4 and B = 6

Question **3**

Correct

Mark 1.00 out of 1.00

Which of the following is the correct sequence of steps undertaken when a cache miss occurs?

Select one:

- a. Activate memory controller, stall processor, request data item from lower level of hierarchy, load data item into cache, resume processor.
- b. Stall processor, request data item from lower level of hierarchy, activate memory controller, load data item into cache, resume processor.
- c. Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor. ✔
- d. Don't know/no answer
- e. Stall processor, request data item from lower level of hierarchy, load data item into cache, activate memory controller, resume processor.
- f. Activate memory controller, request data item from lower level of hierarchy, stall processor, load data item into cache, resume processor.

The correct sequence of steps is: stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct answer is: Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

Question **4**

Correct

Mark 1.00 out of 1.00

A 24-bit address generates an address space of _____ locations.
(select a value below to fill in the blank)

Select one:

- a. 16,777,216 ✔
- b. 4,294,967,296
- c. 1024
- d. 4096

Your answer is correct.

The number of addressable locations in the system is called an address space. The answer is 2 to the power 24 = 16,777,216.

The correct answer is: 16,777,216

Question **5**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 16 blocks where each block contains 16 bytes. Determine the size of the tag field in the memory addresses used by this computer.

Select one:

- a. 5
- b. 32
- c. 24 ✔
- d. 3
- e. 16
- f. Don't know/no answer

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = $2^{32}$). Thus, the total size of the tag, block and offset fields is 32.

As the cache gas 16 blocks, it can be indexed with 4 bits (16 = $2^4$), so the size of the block field is 4 bits.

As each block has 16 bytes, we need 4 bits for the offset field to access each byte in the block (16=$2^4$) bytes .

Finally, the tag field is: 32 - 4 - 4 = 24.

The correct answer is: 24

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. Don't know/no answer
- b. 32
- c. 8 ✔
- d. 16
- e. 4
- f. 3

Your answer is correct.

The total size of the tag, block and offset fields is 16.

32 = $2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has 8=$2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 8

Question **7**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 9 ✔
- b. 16
- c. 8
- d. 5
- e. 4
- f. Don't know/no answer

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = $2^4$), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=$2^3$); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 9

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following statements about ROM is correct?

- a. ROM is a type of L2 cache memory.
- b. ROM stores the operating system of a computer.
- c. ROM is needed to support the mapping of cache memory addresses to main memory addresses.
- d. ROM stores the program that boots a computer. ✔
- e. ROM is a type of L1 cache memory.

Your answer is correct.

ROM stores the program that boots a computer.

The correct answer is:
ROM stores the program that boots a computer.

Question **9**

Correct

Mark 1.00 out of 1.00

Which type of memory is built with capacitors that slowly leak their charge hence they must be refreshed every few milliseconds to prevent data loss?

Select one:

- a. SRAM
- b. DRAM ✔
- c. Registers
- d. Cache

Your answer is correct.

The correct answer is: DRAM

Question **10**

Correct

Mark 1.00 out of 1.00

What is a bit of SRAM constructed from?

Select one:

- a. Three transistors and a floating-gate transistor.
- b. Don't know/no answer
- c. Six transistors ✔
- d. Four transistors.
- e. One transistor and one capacitor
- f. Two capacitors and a floating-gate transistor.

A bit of SRAM is constructed from 6 transistors.

The correct answer is: Six transistors

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