IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

The reason for the implementation of the cache memory is?

Select one:

- a. To increase the internal memory of the system
- b. To reduce the memory access and cycle time
- c. To mitigate the difference in speeds of operation of the processor and memory ✔
- d. All of the mentioned

Your answer is correct.

The correct answer is "to mitigate the difference in speeds of operation of the processor and memory". Cache will not increase the physical memory size or reduce the memory access and cycle time

The correct answer is: To mitigate the difference in speeds of operation of the processor and memory

Question **2**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *sequential locality?*

Select one:

- a. Don't know/no answer
- b. Items in memory tend to get used more than once when accessed.
- c. Instructions tend to be accessed sequentially. ✔
- d. Items get placed in cache lines in the order that they enter.
- e. Items stored together in memory get used together.
- f. Items get removed from the cache based on the order that they enter.

Sequential locality refers to the common feature of programs that instructions tend to be accessed sequentially.

The correct answer is: Instructions tend to be accessed sequentially.

Question **3**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 16 blocks where each block contains 16 bytes. Determine the size of the tag field in the memory addresses used by this computer.

Select one:

- a. 5
- b. 32
- c. 24 ✔
- d. Don't know/no answer
- e. 3
- f. 16

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset fields is 32.

As the cache gas 16 blocks, it can be indexed with 4 bits (16 = 2^4), so the size of the block field is 4 bits.

As each block has 16 bytes, we need 4 bits for the offset field to access each byte in the block (16=2^4) bytes .

Finally, the tag field is: 32 - 4 - 4 = 24.

The correct answer is: 24

Question **4**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Block 512
- b. Block 399 ✔
- c. Block 58
- d. Don't know/no answer
- e. Block 201
- f. Block 124

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32^{nd} to 16^{th}) BLOCK (15^{th} to 7^{th} bit) OFFSET (6^{th} to 1^{st} bit)

The hexadecimal address $000063FA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 11**11 1010

And if we convert 110001111_{bin} to decimal, we get 399_{dec} So the given address will map to block 399 in cache.

The correct answer is: Block 399

Question **5**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000053AA_{16}$ map?

Select one:

- a. Block 124
- b. Block 334 ✔
- c. Block 58
- d. Block 201
- e. Don't know/no answer
- f. Block 512

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32^{nd} to 16^{th}) BLOCK (15^{th} to 7^{th} bit) OFFSET (6^{th} to 1^{st} bit)

The hexadecimal address $000053AA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0101 0011 1010 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**101 0011 10**10 1010

And if we convert 101001110_{bin} to decimal, we get 334_{dec} So the given address will map to block 334 in cache.

The correct answer is: Block 334

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 32
- b. Don't know/no answer
- c. 16
- d. 8
- e. 5
- f. 3 ✔

The total size of the tag, block and offset fields is 16.
$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 3

Question **7**

Correct

Mark 1.00 out of 1.00

Which type of memory is built with capacitors that slowly leak their charge hence they must be refreshed every few milliseconds to prevent data loss?

Select one:

- a. SRAM
- b. Registers
- c. DRAM ✔
- d. Cache

Your answer is correct.

The correct answer is: DRAM

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. Don't know/no answer
- b. 32 D flip-flops and 16 RS flip-flops.
- c. 64 RS flip-flips
- d. 32 D flip-flops and 32 RS flip-flops
- e. 32 D flip-flops.
- f. 64 D flip-flops ✔

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

Question **9**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 4
- b. Don't know/no answer
- c. 16
- d. 8
- e. 5
- f. 3 ✔

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 3

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *temporal locality*?

Select one:

- a. Items get written to memory locations in the order that the processor accesses the memory locations.
- b. Items get removed from the cache based on the order that they enter.
- c. Don't know/no answer
- d. Items get placed in cache positions in the order that they enter.
- e. Items in memory tend to get used more than once when accessed. ✔
- f. Items stored together in memory get used together.

Temporal locality refers to the common feature of programs that items in memory tend to get used more than once when accessed.

The correct answer is: Items in memory tend to get used more than once when accessed.

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