IN1006 Systems Architecture (PRD1 A 2022/23)

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State	Finished
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Grade	**8.90** out of 10.00 (**89**%)

Question **1**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below?

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 1 ✔
- b. 3
- c. 4
- d. 2
- e. Don't know/no answer
- f. 5

All instructions have some dependency with another.

The correct answer is: 1

Question **2**

Correct

Mark 1.00 out of 1.00

What does the acronym ILP stand for?

Select one:

- a. Don't know/no answer
- b. Inductive Logic programming
- c. Information Leak Prevention
- d. Instruction Level Parallelism ✔
- e. Integer Linear programming
- f. Integer Logic Parallelism

ILP stands for Instruction Level Parallelism in the context of systems architecture. See: http://en.wikipedia.org/wiki/Instruction_level_parallelism

The correct answer is: Instruction Level Parallelism

Question **3**

Correct

Mark 1.00 out of 1.00

In what way are compilers usually used to prevent pipeline hazards?

Select one:

- a. Rearrange instructions such that an instruction that does not affect the decision is executed after the decision filling the bubble that would occur if the pipeline were to stall.
- b. Preventing data hazards by releasing the results before they are written to the registers.
- c. Use of deep pipelines to maximise throughput.
- d. A method to avoid control hazards by predicting what way a conditional branch instruction will execute in advance.
- e. Rearranging the instructions to avoid data hazards where possible. ✔
- f. Don't know/no answer

Compliers can be used to rearrange the instructions to avoid data hazards.

The correct answer is: Rearranging the instructions to avoid data hazards where possible.

Question **4**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. lw d1, 8($t0)
2. lw d2, 9($t0)
3. lw d3, 10($t0)
4. add e1, d1, d2
5. add e2, d1, d3
6. add e3, d2, d3

Which of the architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

- a. MISD
- b. Do not know the answer
- c. SIMD ✔
- d. MIMD
- e. SISD or SIMD
- f. SISD

Your answer is correct.

Instructions 1-3 fit with SIMD as they involve the same instruction upon different data. Instructions 4-6 also fit with SIMD for the same reason.

Thus, SIMD is the best option for the above code.

The correct answer is: SIMD

Question **5**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'data hazard'?

Select one:

- a. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- b. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions. ✔
- c. A gap in the pipeline where some or all of the stages are not processing an instruction.
- d. Don't know/no answer
- e. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- f. Waiting for the next instruction to be fetched after a branch is taken.

A data hazard occurs when an instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

The correct answer is: Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following describes best the concept of "out-of-order" execution?

- a. An instruction and a data queue are used to regulate the execution of instructions by the CPU. ✔
- b. Instructions are executed in two separate CPUs operating in parallel.
- c. Instructions are loaded first to cache before brought to the CPU for execution.
- d. Instructions are executed in pipelines.
- e. Do not know the answer

Your answer is correct.

Instructions are not given to the CPU for execution immediately when they are due. They are placed in a queue and are moved from it to the CPU only when all the data that they need are available. Also the data D produced by an instruction I are placed in a queue and only when the data of all the instructions that were earlier than I are also written in the queue data, D are written to memory.

The correct answer is:
An instruction and a data queue are used to regulate the execution of instructions by the CPU.

Question **7**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,c
4. add h, e, d
5. add f, a, b

Select one:

- a. Don't know/no answer
- b. 2
- c. 3 ✔
- d. 1
- e. 4
- f. 5

Instructions 1, 2 and 3 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2 and 4 (i.e. d – the MIPS pipeline has two stages between execution and write to register). However 3, 4, 5 have no dependences. Therefore the largest size block of non-dependent instructions is 3.

The correct answer is: 3

Question **8**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 3
- b. 4
- c. 2
- d. Don't know/no answer
- e. 1 ✔
- f. 5

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

Question **9**

Incorrect

Mark -0.10 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,b
4. add h, g, k
5. add f, a, h

Select one:

- a. Don't know/no answer
- b. 2 ✖
- c. 3
- d. 5
- e. 1
- f. 4

Your answer is incorrect.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. In the above block:

- Instructions 1, 2 and 3 have no dependency.
- There is a dependency between 4 and 3 (due to g).
- There is a dependency between 4 and 5 (due to h).

Therefore the largest size block of non-dependent instructions is 3.

The correct answer is: 3

Question **10**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. sub d2, b1 ,c1
3. add e1, d1, d2
4. sub e2, d1, d2

Which of the architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

- a. MISD ✔
- b. MIMD
- c. SISD or SIMD
- d. Do not know the answer
- e. MIMD or SISD
- f. SIMD

Your answer is correct.

Instructions 1-2 fit with MISD as they involve different instructions upon the same data. Instructions 3-4 also fit with MISD for the same reason.

Thus, MISD is the best option for the above code.

The correct answer is: MISD

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