IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the following flip-flops is most often used to construct SRAM?

Select one:

- a. J flip-flip
- b. Clocked RS flip-flip
- c. D flip-flop ✔
- d. SR flip-flop
- e. Don't know/no answer
- f. RS flip-flip

A D flip-flip is the form of flip-flop used in SRAM as one (D) input specifies what is to be written.

The correct answer is: D flip-flop

Question **2**

Correct

Mark 1.00 out of 1.00

Assume a computer having a cache whose block size is 1024 bytes. Which of the following programs would lead the most effective use of the sequential locality?

Select one:

- a. A program with 50 instructions that reads and transforms data in a file which can grow dynamically.
- b. A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points. ✔
- c. A program that reads 2000 data points from a file and prints them to the computer terminal.
- d. A program with 900 instructions that processes an array with 300 data points.
- e. Do know the answer.
- f. A program with that computes the sum of 9999 numbers stored in a file.

Sequential locality refers to the common feature of programs that instructions and data tend to be accessed sequentially.

As the block size of the computer is 1024 bytes only the program with the 800 instructions processing the array of 200 data points would be possible to fit in one block and thus execute as many times as required without the need to transfer further data and/or instructions from the main memory to the cache. The existence of a loop in this program would not affect sequential locality either since the jump from the last to the first instruction of the loop in the program would not cause any transfers to and from the main memory because all instructions of the program can fit in the cache and would be loaded at the start of the program's execution.

All other options given may lead to data/instructions transfers between cache and the main memory thus violating sequential locality.

The correct answer is: A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points.

Question **3**

Correct

Mark 1.00 out of 1.00

Which of the following best describes a cache memory in *Harvard Architecture*?

Select one:

- a. An arrangement where data and instructions appear in the same cache.
- b. Don't know/no answer
- c. A cache where each data item can be assigned to any block as needed.
- d. A cache where the last n-bits of a block's address denotes which grouping of cache lines are used.
- e. An arrangement where the data and instruction caches are separated. ✔
- f. A cache where the assignment of data items (blocks) to cache lines is determined by the last n-bits of the data item's address.

The Harvard cache architecture refers to an arrangement where the data and instructions are split into separate caches.

The correct answer is: An arrangement where the data and instruction caches are separated.

Question **4**

Correct

Mark 1.00 out of 1.00

A 24-bit address generates an address space of _____ locations.
(select a value below to fill in the blank)

Select one:

- a. 16,777,216 ✔
- b. 4096
- c. 4,294,967,296
- d. 1024

Your answer is correct.

The number of addressable locations in the system is called an address space. The answer is 2 to the power 24 = 16,777,216.

The correct answer is: 16,777,216

Question **5**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 4
- b. 8
- c. Don't know/no answer
- d. 5
- e. 16
- f. 3 ✔

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 3

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose the cache access time is 10ns, main memory access time is 200ns and the cache hit rate is 90%. What is the EAT for the processor to access an item in the cache?

Select one:

- a. Don't know/no answer
- b. 210ns
- c. 29ns ✔
- d. 10ns for 90% of the times.
- e. 10ns
- f. 200ns

EAT = 0.9*10ns + (1-0.9)*200ns = 29ns

The correct answer is: 29ns

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following *best* describes why a memory hierarchy is needed?

Select one:

- a. Don't know/no answer
- b. DRAM is cheaper than SRAM per unit of memory.
- c. SRAM is cheaper than DRAM per unit of memory.
- d. It is useful to be able to exceed physical memory limits.
- e. Processor speeds have increased faster than SRAM speeds.
- f. Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs. ✔

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 32 D flip-flops and 32 RS flip-flops
- b. 64 RS flip-flips
- c. 64 D flip-flops ✔
- d. 32 D flip-flops.
- e. 32 D flip-flops and 16 RS flip-flops.
- f. Don't know/no answer

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

Question **9**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 8
- b. Don't know/no answer
- c. 5 ✔
- d. 3
- e. 16
- f. 32

The total size of the tag, block and offset fields is 16.
$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 5

Question **10**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 128 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. Don't know/no answer
- b. T= 8 , O= 16 and B = 8
- c. T= 24 , O= 4 and B = 4
- d. T= 28 , O= 2 and B = 2
- e. T= 20 , O= 5 and B = 7 ✔
- f. T= 16 , O= 8 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 128 blocks, it can be indexed with 7 bits (128 = 2^7), so the size of the block (B) field is 7 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 7 - 5 = 20.

The correct answer is: T= 20 , O= 5 and B = 7

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