IN1006 Systems Architecture (PRD1 A 2022/23)

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Started on	Thursday, 15 December 2022, 4:29 PM
State	Finished
Completed on	Thursday, 15 December 2022, 4:40 PM
Time taken	11 mins 15 secs
Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. sub d2, b1 ,c1
3. add e1, d1, d2
4. sub e2, d1, d2

Which of the architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

○ a. Do not know the answer

○ b. SIMD

○ c. MIMD

● d. MISD ✓

○ e. MIMD or SISD

○ f. SISD or SIMD

Your answer is correct.

Instructions 1-2 fit with MISD as they involve different instructions upon the same data. Instructions 3-4 also fit with MISD for the same reason.

Thus, MISD is the best option for the above code.

The correct answer is: MISD

Question **2**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a ‘data hazard’?

Select one:

○ a. Waiting for the next instruction to be fetched after a branch is taken.

● b. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions. ✓

○ c. A gap in the pipeline where some or all of the stages are not processing an instruction.

○ d. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

○ e. Don't know/no answer

○ f. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch

A data hazard occurs when an instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

The correct answer is: Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Question **3**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. add d2, b2 ,c2
3. add d3, b3 ,c3
4. add d4, b4, c4
5. add d5, c5, b5

Which of the four architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

● a. SIMD ✓

○ b. SISD

○ c. MIMD

○ d. Do not know the answer

○ e. MIMD and MISD

○ f. MISD

Your answer is correct.

Instructions 1-5 above are the same (add) and are executed upon different data. Thus, SIMD is the most suitable architecture.

The correct answer is: SIMD

Question **4**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, c ,d
3. add f, e , b
4. add h, k, g
5. add m, k, w

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

○ a. Move instruction 5 before instruction 1.

● b. Move instructions 4 and 5 before instruction 3. ✓

○ c. Do not know the answer.

○ d. No compiler optimisation is possible.

○ e. Move instruction 4 before instruction 3.

Your answer is correct.

Instruction 3 depends on instruction 2 (due to b). Instructions 4 and 5 can be moved before it in the program without affecting the overall program outcome. This move would make instruction 3 to load b in the 7th cycle in a pipeline execution (assuming that instruction 1 starts in cycle 1). In the 7th cycle however instruction 2 will have written b to memory (this would happen in cycle 5 of the pipeline). So the data hazard would no longer be present.

The correct answer is:
Move instructions 4 and 5 before instruction 3.

Question **5**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. sub d2, b1 ,c1
3. add d3, b2 ,c2
4. sub d4, b2, c2

Which of the architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

○ a. SISD or SIMD

○ b. MIMD or SISD

○ c. SISD or SIMD

● d. SIMD or MISD ✓

○ e. Do not know the answer

○ f. MIMD or MISD

Your answer is correct.

Instructions 1-2 fit with MISD as they involve different instructions upon the same data. Instructions 3-4 also fit with MISD for the same reason.

Instructions 1, 3 fit with SIMD as they involve the same instruction upon different datasets. Instructions 2-4 also fit with SIMD for the same reason.

Thus, MISD or SIMD would be the best options for the above code.

The correct answer is: SIMD or MISD

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'stall'?

Select one:

○ a. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch

● b. Waiting for the next instruction to be fetched after a branch is taken. ✓

○ c. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

○ d. A gap in the pipeline where some or all of the stages are not processing an instruction.

○ e. Don't know/no answer

○ f. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

A stall occurs in response to a control hazard. It involves waiting for the next instruction to be fetched after a branch is taken.

The correct answer is: Waiting for the next instruction to be fetched after a branch is taken.

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a ‘control hazard’?

Select one:

● a. Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check. ✓

○ b. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

○ c. A gap in the pipeline where some or all of the stages are not processing an instruction.

○ d. Don't know/no answer

○ e. Loading instructions into pipeline which try to access memory at the same stage.

○ f. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Your answer is correct.

A control hazard occurs when an instruction I has been loaded to a pipeline although due to some condition check which is already being executed in the pipeline it turns out that I should not be executed.

The correct answer is: Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check.

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following describes best the concept of "out-of-order" execution?

○ a. Instructions are executed in two separate CPUs operating in parallel.

○ b. Instructions are executed in pipelines.

○ c. Instructions are loaded first to cache before brought to the CPU for execution.

○ d. Do not know the answer

● e. An instruction and a data queue are used to regulate the execution of instructions by the CPU. ✓

Your answer is correct.

Instructions are not given to the CPU for execution immediately when they are due. They are placed in a queue and are moved from it to the CPU only when all the data that they need are available. Also the data D produced by an instruction I are placed in a queue and only when the data of all the instructions that were earlier than I are also written in the queue data, D are written to memory.

The correct answer is:
An instruction and a data queue are used to regulate the execution of instructions by the CPU.

Question **9**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, b ,d
3. add f, e , a
4. add h, k, g
5. add m, a, b

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

○ a. Do not know the answer.

● b. Move instruction 4 before instruction 3. ✓

○ c. Move instruction 5 before instruction 3.

○ d. No optimisations are possible.

○ e. Move instructions 5 before instruction 4.

Your answer is correct.

The data hazards in this code arise due to instruction 3 (it depends on instruction 1).

Moving instruction 4 before instruction 3 will resolve the hazard as following the move instruction 3 will read data in cycle 5 and by this cycle instruction 1 will have stored its output.

The correct answer is:
Move instruction 4 before instruction 3.

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following is *not* a design decision made in the MIPS architecture to support pipelining?

Select one:

○ a. Operands are aligned hence no single data transfer instruction will require two memory accesses.

○ b. Instructions have the same format allowing the data to be fetched before the instruction is decoded.

○ c. Don't know/no answer

○ d. All instructions have the same length and are therefore easier to decode in a pipeline.

● e. Use of deep pipelines to maximise throughput. ✓

○ f. Memory operands only appear in loads and stores allowing the execute stage to calculate addresses.

The instruction pipelines in MIPS implementations are not especially deep, especially by modern standards.

The correct answer is: Use of deep pipelines to maximise throughput.

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