IN1006 Systems Architecture (PRD1 A 2022/23)

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Time taken	23 mins 2 secs
Grade	**6.70** out of 10.00 (**67**%)

Question **1**

Incorrect

Mark -0.10 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, c ,d
3. add f, e , b
4. add h, k, g
5. add m, k, w

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

a. Move instruction 5 before instruction 1.
b. Move instructions 4 and 5 before instruction 3.
c. No compiler optimisation is possible.
d. Do not know the answer.
e. Move instruction 4 before instruction 3.

✖ Move instruction 5 before instruction 3.

Your answer is incorrect.

Instruction 3 depends on instruction 2 (due to b). Instructions 4 and 5 can be moved before it in the program without affecting the overall program outcome. This move would make instruction 3 to load b in the 7th cycle in a pipeline execution (assuming that instruction 1 starts in cycle 1). In the 7th cycle however instruction 2 will have written b to memory (this would happen in cycle 5 of the pipeline). So the data hazard would no longer be present.

The correct answer is:
Move instructions 4 and 5 before instruction 3.

Question **2**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'control hazard'?

Select one:

- a. A gap in the pipeline where some or all of the stages are not processing an instruction.
- b. Don't know/no answer
- c. Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check. ✔
- d. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- e. Loading instructions into pipeline which try to access memory at the same stage.
- f. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Your answer is correct.

A control hazard occurs when an instruction I has been loaded to a pipeline although due to some condition check which is already being executed in the pipeline it turns out that I should not be executed.

The correct answer is: Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check.

Question **3**

Correct

Mark 1.00 out of 1.00

What does the acronym ILP stand for?

Select one:

- a. Integer Logic Parallelism
- b. Don't know/no answer
- c. Information Leak Prevention
- d. Instruction Level Parallelism ✔
- e. Integer Linear programming
- f. Inductive Logic programming

ILP stands for Instruction Level Parallelism in the context of systems architecture. See: http://en.wikipedia.org/wiki/Instruction_level_parallelism

The correct answer is: Instruction Level Parallelism

Question **4**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 5
- b. 3
- c. 1 ✔
- d. 4
- e. 2
- f. Don't know/no answer

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

Question **5**

Incorrect

Mark -0.10 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, b ,d
3. add f, e , a
4. add h, k, g
5. add m, a, b

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

- a. Move instructions 5 before instruction 4. ✖
- b. Move instruction 4 before instruction 3.
- c. Do not know the answer.
- d. No optimisations are possible.
- e. Move instruction 5 before instruction 3.

Your answer is incorrect.

The data hazards in this code arise due to instruction 3 (it depends on instruction 1).

Moving instruction 4 before instruction 3 will resolve the hazard as following the move instruction 3 will read data in cycle 5 and by this cycle instruction 1 will have stored its output.

The correct answer is:
Move instruction 4 before instruction 3.

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'structural hazard'?

Select one:

- a. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- b. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.
- c. Don't know/no answer
- d. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses. ✔
- e. A gap in the pipeline where some or all of the stages are not processing an instruction.
- f. Waiting for the next instruction to be fetched after a branch is taken.

A structural hazard occurs when hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

The correct answer is: Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'data hazard'?

Select one:

- a. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions. ✔
- b. Waiting for the next instruction to be fetched after a branch is taken.
- c. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- d. Don't know/no answer
- e. A gap in the pipeline where some or all of the stages are not processing an instruction.
- f. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

A data hazard occurs when an instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

The correct answer is: Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Question **8**

Correct

Mark 1.00 out of 1.00

Match the description for the correct MIPS notation for MIPS Pipeline.

Instruction fetch from memory	IF ✔
Instruction decode and register read	ID ✔
Access memory operand	MEM ✔
Execute operation or calculate address	EX ✔
Write result back to register	WB ✔

Your answer is correct.

The correct answer is: Instruction fetch from memory → IF,
Instruction decode and register read
→ ID,
Access memory operand
→ MEM,
Execute operation or calculate address
→ EX,
Write result back to register
→ WB

Question **9**

Incorrect

Mark -0.10 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add c, b ,d
3. add f, c ,a
4. add k, l, m
5. add h, e, g
6. add f, h, b

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

a. Move instruction 4 before instruction 3.
b. No optimisations are possible.
c. Move instruction 4 and 5 before instruction 3 and swap the order of their execution.
d. Do not know the answer.
e. Move instruction 4 and 5 before instruction 3. ✖

Your answer is incorrect.

The data hazards in this code arise due to instruction 3 (it depends on instructions 1 and 2) and instruction 6 (it depends on instruction 5).

Moving instruction 4 and 5 before instruction 3 and swapping the order of their execution would remove these hazards. This is because following these changes:

Instruction 3 would try to fetch data in the 6th cycle of the pipeline. In this cycle, instruction 2 will have completed the write to memory stage. Also instruction 6 which depends on instruction 5, would try to read data in cycle 7 by which instruction 5 will have written its output.

The correct answer is:
Move instruction 4 and 5 before instruction 3 and swap the order of their execution.

Question **10**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

add a, b, c

add c, b ,c

add f, c ,d

add h, e, f

add f, h, b

Select one:

- a. 4
- b. 2
- c. 3
- d. Don't know/no answer
- e. 5
- f. 1 ✔

Your answer is correct.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

◄ Quiz 6 _ Weekly Assessed Quiz 2022

Jump to...

Quiz navigation

1 2 3 4 6 7 8 9 10

Show one page at a time

Finish review