



IN1006 Systems Architecture (PRD1 A 2022/23)

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Started on	Thursday, 8 December 2022, 3:26 PM
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Time taken	24 mins 54 secs
Grade	7.90 out of 10.00 (79 %)
Question 1 Incorrect	
Mark -0.10 out of 1.00	

The reason for the implementation of the cache memory is?

Select one:

- a. All of the mentioned
- b. To increase the internal memory of the system
- oc. To mitigate the difference in speeds of operation of the processor and memory
- od. To reduce the memory access and cycle time

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Your answer is incorrect.

The correct answer is "to mitigate the difference in speeds of operation of the processor and memory". Cache will not increase the physical memory size or reduce the memory access and cycle time

The correct answer is: To mitigate the difference in speeds of operation of the processor and memory



Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address 000063FA₁₆ map?

Select one:

- a. Block 1
- b. Block 64
- oc. Block 799
- od. Block 573
- e. Don't know/no answer
- f. Block 1024

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits (1024 = 2^{10}), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

TAG (32nd to 16th) BLOCK (15th to 6th bit) OFFSET (5th to 1st bit)

The hexadecimal address 000063FA₁₆ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 111**1 1010

And if we convert 110 0011 111_{bin} to decimal, we get 799_{dec} So the given address will map to block 799 in cache.

The correct answer is: Block 799







Suppose the cache access time of a computer is 10ns and its main memory access time is 15 times slower. Assuming that the cache hit rate is 70%, what is the effective access time (EAT) for the processor to access an item in the cache?

Select one:

- a. 200ns
- b. 52ns for 90% of the times.
- c. 210ns for 30% of the times
- d. 52ns
- e. Don't know/no answer
- f. 10ns

Your answer is correct.

EAT = 0.7*10ns + (1-0.7)*150ns = 52ns

The correct answer is: 52ns

Question 4

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of temporal locality?

Select one:

- a. Items get placed in cache positions in the order that they enter.
- O b. Items get removed from the cache based on the order that they enter.
- o c. Items in memory tend to get used more than once when accessed.
- od. Don't know/no answer
- e. Items stored together in memory get used together.
- of. Items get written to memory locations in the order that the processor accesses the memory locations.

Temporal locality refers to the common feature of programs that items in memory tend to get used more than once when accessed.

The correct answer is: Items in memory tend to get used more than once when accessed.









Which of the following is t	he most accurate statement	relating to the term	virtual memory?
William of the following is t	, ic intost accurate statement	relating to the term	vii tuai iiitiiii y:

Select one:

- a. Don't know/no answer
- b. Allows secondary storage (e.g. hard disk) to play the role of main memory.The basic ide support extra suppor
 - The basic idea of VM is that the disk is used to support extra virtual pages of main memory

- oc. Allows the DRAM capacity to be increased.
- d. Allows secondary storage (e.g. hard disk) to play the role of the cache.
- e. Allows programmers to write sloppy code.
- f. Allows the cache hit rate to be increased.

Virtual memory allows secondary storage (e.g. hard disk) to play the role of main memory.

The correct answer is: Allows secondary storage (e.g. hard disk) to play the role of main memory.

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 5
- o b. 8
- oc. 16
- Od. Don't know/no answer
- e. 4
- 0 f. 3

The total size of the tag, block and offset fields is 16.

16 blocks of cache can be indexed with 4 bits $(32 = 2^4)$, so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits $(8=2^3)$; thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 4

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If a cache access requires one clock cycle and dealing with cache misses requires an additional five clock cycles, which of the following cache hit rates results in an effective access time of 2 clock cycles?

Select one:

- a. Don't know/no answer
- ob. 85%
- oc. 90%
- d. 80%
- e. 95%
- f. 70%

The effective access time is calculated by: EAT = h *access_hit_time + (1-h) access_miss_time where h is hit rate. In this case, access_hit_time = 1 clock cycle, access_miss_time = 1+5=6 clock cycles, and EAT = 2 clock cycles. So:

2 = h * 1 + (1-h) * 6 => -h+6h=6-2 => 5h = 4 > h = 4/5 or 80%

The correct answer is: 80%

Question 8

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *spatial locality?*

Select one:

- a. Don't know/no answer
- b. Items in memory tend to get used more than once when accessed.
- oc. Items get written to memory locations in the order that the processor accesses the memory locations.
- d. Items get placed in cache positions in the order that they enter.
- e. Items get removed from the cache based on the order that they enter.
- of. Items stored together in memory get used together.

Spatial locality refers to the common feature of programs that items stored together in memory get used together. The correct answer is: Items stored together in memory get used together.

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A 24-bit address generates an address space of _____ locations. (select a value below to fill in the blank)

Select one:

- a. 4096
- b. 16,777,216
- oc. 1024
- d. 4,294,967,296

Your answer is correct.

The number of addressable locations in the system is called an address space. The answer is 2 to the power 24 = 16,777,216.

The correct answer is: 16,777,216

2 =



Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Don't know/no answer
- ob. Block 58
- oc. Block 399
- d. Block 201
- e. Block 124
- f. Block 512

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits $(512 = 2^9)$, so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus, the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32nd to 16th) BLOCK (15th to 7th bit) OFFSET (6th to 1st bit)

The hexadecimal address 000063FA₁₆ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 11**11 1010

And if we convert 110001111_{bin} to decimal, we get 399_{dec} So the given address will map to block 399 in cache.

The correct answer is: Block 399

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