IN1006 Systems Architecture (PRD1 A 2022/23)

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Time taken	13 mins 8 secs
Grade	**8.90** out of 10.00 (**89**%)

Question **1**

Incorrect

Mark -0.10 out of 1.00

In what way are compilers usually used to prevent pipeline hazards?

Select one:

- a. Don't know/no answer
- b. Rearrange instructions such that an instruction that does not affect the decision is executed after the decision filling the bubble that would occur if the pipeline were to stall.
- c. Preventing data hazards by releasing the results before they are written to the registers.
- d. Rearranging the instructions to avoid data hazards where possible.
- e. Use of deep pipelines to maximise throughput. ✖
- f. A method to avoid control hazards by predicting what way a conditional branch instruction will execute in advance.

Compliers can be used to rearrange the instructions to avoid data hazards.

The correct answer is: Rearranging the instructions to avoid data hazards where possible.

Question **2**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,c
4. add h, e, d
5. add f, a, b

Select one:

- a. 1
- b. 3 ✔
- c. 4
- d. Don't know/no answer
- e. 2
- f. 5

Instructions 1, 2 and 3 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2 and 4 (i.e. d – the MIPS pipeline has two stages between execution and write to register). However 3, 4, 5 have no dependences. Therefore the largest size block of non-dependent instructions is 3.

The correct answer is: 3

Question **3**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. sub d, b ,c
3. add g, e ,d
4. add h, e, f
5. sub a, a, b

Select one:

- a. 2
- b. 5
- c. 1
- d. 3 ✔
- e. 4
- f. Don't know/no answer

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. Instructions 1 and 2 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2, 3 (i.e. d). However 3, 4, 5 have no dependences. Therefore the largest sized block of non-dependent instructions is 3. Mixing instruction types has no effect.

The correct answer is: 3

Question **4**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,b
4. add h, g, k
5. add f, a, h

Select one:

- a. 1
- b. 5
- c. 4
- d. 2
- e. 3 ✔
- f. Don't know/no answer

Your answer is correct.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. In the above block:

- Instructions 1, 2 and 3 have no dependency.
- There is a dependency between 4 and 3 (due to g).
- There is a dependency between 4 and 5 (due to h).

Therefore the largest size block of non-dependent instructions is 3.

The correct answer is: 3

Question **5**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 2
- b. 4
- c. 3
- d. 1 ✔
- e. Don't know/no answer
- f. 5

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following describes best the concept of "out-of-order" execution?

- a. Instructions are executed in two separate CPUs operating in parallel.
- b. Do not know the answer
- c. Instructions are executed in pipelines.
- d. An instruction and a data queue are used to regulate the execution of instructions by the CPU. ✔
- e. Instructions are loaded first to cache before brought to the CPU for execution.

Your answer is correct.

Instructions are not given to the CPU for execution immediately when they are due. They are placed in a queue and are moved from it to the CPU only when all the data that they need are available. Also the data D produced by an instruction I are placed in a queue and only when the data of all the instructions that were earlier than I are also written in the queue data, D are written to memory.

The correct answer is:
An instruction and a data queue are used to regulate the execution of instructions by the CPU.

Question **7**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,d
4. add h, e, f
5. add f, a, b

Select one:

- a. 3
- b. 1
- c. 4
- d. 2 ✔
- e. Don't know/no answer
- f. 5

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. In the above block,

- Instructions 1, 2, do not depend on each other.
- Instruction 3 depends on instruction 2 (due to d)
- There is a dependency between 4 and 5 (due to f).

Therefore the largest size block of non-dependent instructions is 2.

The correct answer is: 2

Question **8**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. sub d, b ,c
3. add g, e ,d
4. add h, e, f
5. sub n, f, b

Select one:

- a. 4 ✔
- b. 3
- c. 1
- d. 5
- e. Don't know/no answer
- f. 2

Your answer is correct.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. In the above program instructions 1, 2, 4 and 5 can be executed in parallel as they do not depend on data that any of them generates. Therefore 4 is the number of execution units.

The correct answer is: 4

Question **9**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

```
add a, b, c
add c, b ,c
add f, c ,d
add h, e, f
add f, h, b
```

Select one:

- a. 5
- b. 1 ✔
- c. Don't know/no answer
- d. 4
- e. 3
- f. 2

Your answer is correct.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

Question **10**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, b ,d
3. add f, e , a
4. add h, k, g
5. add m, a, b

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

- a. Move instruction 4 before instruction 3. ✔
- b. Move instruction 5 before instruction 3.
- c. Move instructions 5 before instruction 4.
- d. No optimisations are possible.
- e. Do not know the answer.

Your answer is correct.

The data hazards in this code arise due to instruction 3 (it depends on instruction 1).

Moving instruction 4 before instruction 3 will resolve the hazard as following the move instruction 3 will read data in cycle 5 and by this cycle instruction 1 will have stored its output.

The correct answer is:
Move instruction 4 before instruction 3.

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