IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	10.00 out of 10.00 (100%)

Question 1

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 128 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 24 , O= 4 and B = 4
- b. T= 16 , O= 8 and B = 8
- c. T= 28 , O= 2 and B = 2
- d. T= 8 , O= 16 and B = 8
- e. Don't know/no answer
- f. T= 20 , O= 5 and B = 7 ✔

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 128 blocks, it can be indexed with 7 bits (128 = 2^7), so the size of the block (B) field is 7 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 7 - 5 = 20.

The correct answer is: T= 20 , O= 5 and B = 7

Question 2

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 3
- b. 32
- c. 4
- d. 8 ✔
- e. 16
- f. Don't know/no answer

Your answer is correct.

The total size of the tag, block and offset fields is 16.

$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 8

Question 3

Correct

Mark 1.00 out of 1.00

Which of the following flip-flops is most often used to construct SRAM?

Select one:

- a. RS flip-flip
- b. D flip-flop ✔
- c. Don't know/no answer
- d. J flip-flip
- e. SR flip-flop
- f. Clocked RS flip-flip

A D flip-flip is the form of flip-flop used in SRAM as one (D) input specifies what is to be written.

The correct answer is: D flip-flop

Question 4

Correct

Mark 1.00 out of 1.00

Suppose the cache access time is 10ns, main memory access time is 200ns and the cache hit rate is 90%. What is the EAT for the processor to access an item in the cache?

Select one:

- a. 210ns
- b. Don't know/no answer
- c. 10ns
- d. 29ns ✔
- e. 10ns for 90% of the times.
- f. 200ns

EAT = 0.9*10ns + (1-0.9)*200ns = 29ns

The correct answer is: 29ns

Question 5

Correct

Mark 1.00 out of 1.00

Which of the following is the most accurate statement relating to the term *virtual memory*?

Select one:

- a. Allows the DRAM capacity to be increased.
- b. Don't know/no answer
- c. Allows secondary storage (e.g. hard disk) to play the role of the cache.
- d. Allows secondary storage (e.g. hard disk) to play the role of main memory. ✔ The basic idea of VM is that the disk is used to support extra virtual pages of main memory
- e. Allows programmers to write sloppy code.
- f. Allows the cache hit rate to be increased.

Virtual memory allows secondary storage (e.g. hard disk) to play the role of main memory.

The correct answer is: Allows secondary storage (e.g. hard disk) to play the role of main memory.

Question 6

Correct

Mark 1.00 out of 1.00

Which of the following is the correct ordering of the following memory types in *decreasing* order of speed.

Select one:

- a. Hard disk drive, flash memory, DRAM, SRAM.
- b. Don't know/no answer
- c. flash memory, SRAM, DRAM, hard disk drive.
- d. Hard disk drive, flash memory, SRAM, DRAM.
- e. SRAM, DRAM, flash memory, hard disk drive. ✔
- f. SRAM, flash memory, DRAM, hard disk drive.

SRAM is the fastest type of memory, followed by DRAM, flash and hard disks.

The correct answer is: SRAM, DRAM, flash memory, hard disk drive.

Question 7

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 5
- b. Don't know/no answer
- c. 4 ✔
- d. 3
- e. 16
- f. 8

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits ($32 = 2^4$), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits ($8=2^3$); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 4

Question 8

Correct

Mark 1.00 out of 1.00

Which type of memory is built with capacitors that slowly leak their charge hence they must be refreshed every few milliseconds to prevent data loss?

Select one:

- a. SRAM
- b. Cache
- c. DRAM ✔
- d. Registers

Your answer is correct.

The correct answer is: DRAM

Question 9

Correct

Mark 1.00 out of 1.00

Suppose the cache access time of a computer is 10ns and its main memory access time is 15 times slower. Assuming that the cache hit rate is 70%, what is the effective access time (EAT) for the processor to access an item in the cache?

Select one:

- a. 10ns
- b. 200ns
- c. 52ns for 90% of the times.
- d. 52ns ✔
- e. Don't know/no answer
- f. 210ns for 30% of the times

Your answer is correct.

EAT = 0.7*10ns + (1-0.7)*150ns = 52ns

The correct answer is: 52ns

Question 10

Correct

Mark 1.00 out of 1.00

A 24-bit address generates an address space of _____ locations.
(select a value below to fill in the blank)

Select one:

- a. 16,777,216 ✔
- b. 1024
- c. 4,294,967,296
- d. 4096

Your answer is correct.

The number of addressable locations in the system is called an address space. The answer is 2 to the power 24 = 16,777,216.

The correct answer is: 16,777,216

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