

# IN1006 Systems Architecture (PRD1 A 2022/23)

[Home](#) | [My Moodle](#) | [IN1006 PRD1 A 2022-23](#) | [COURSEWORK 1: Weekly Assessed Quiz](#) | [Quiz 6 Weekly Assessed Quiz 2022](#)

**Started on** Thursday, 8 December 2022, 4:45 PM

**State** Finished

**Completed on** Thursday, 8 December 2022, 5:03 PM

**Time taken** 17 mins 58 secs

**Grade** 10.00 out of 10.00 (100%)

## Question 1

Correct

Mark 1.00 out of 1.00

Which of the following is the correct sequence of steps undertaken when a cache miss occurs?

Select one:

- ☐ a. Don't know/no answer
- ☐ b. Stall processor, request data item from lower level of hierarchy, activate memory controller, load data item into cache, resume processor.
- ☐ c. Activate memory controller, request data item from lower level of hierarchy, stall processor, load data item into cache, resume processor.
- ☐ d. Activate memory controller, stall processor, request data item from lower level of hierarchy, load data item into cache, resume processor.
- ☒ e. Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor. ✓
- ☐ f. Stall processor, request data item from lower level of hierarchy, load data item into cache, activate memory controller, resume processor.

The correct sequence of steps is: stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct answer is: Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

Which of the following *best* describes why a memory hierarchy is needed?

Select one:

- ☐ a. SRAM is cheaper than DRAM per unit of memory.
- ☐ b. DRAM is cheaper than SRAM per unit of memory.
- ☐ c. Processor speeds have increased faster than SRAM speeds.
- ☒ d. Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs. ✓
- ☐ e. Don't know/no answer
- ☐ f. It is useful to be able to exceed physical memory limits.

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

### Question 3

Correct

Mark 1.00 out of 1.00

Which of the following statements about the different types of memory that can be found in a computer is correct?

- ☐ a. A computer cannot operate without virtual memory.
- ☒ b. A computer can operate without a cache and secondary memory. ✓
- ☐ c. A computer must always have a full memory hierarchy with L1 cache, L2 cache, RAM and secondary memory.
- ☐ d. A computer can operate without a RAM.
- ☐ e. A computer can operate without a ROM.

Your answer is correct.

The correct answer is:

A computer can operate without a cache and secondary memory.

Which of the following is the best description of the concept of *sequential locality*?

Select one:

- ☒ a. Instructions tend to be accessed sequentially. ✓
- ☐ b. Items stored together in memory get used together.
- ☐ c. Items in memory tend to get used more than once when accessed.
- ☐ d. Items get placed in cache lines in the order that they enter.
- ☐ e. Don't know/no answer
- ☐ f. Items get removed from the cache based on the order that they enter.

Sequential locality refers to the common feature of programs that instructions tend to be accessed sequentially.

The correct answer is: Instructions tend to be accessed sequentially.

Question **5**

Correct

Mark 1.00 out of 1.00

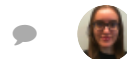
Which of the following is the best description of the concept of *spatial locality*?

Select one:

- ☐ a. Don't know/no answer
- ☐ b. Items get placed in cache positions in the order that they enter.
- ☐ c. Items get written to memory locations in the order that the processor accesses the memory locations.
- ☐ d. Items get removed from the cache based on the order that they enter.
- ☐ e. Items in memory tend to get used more than once when accessed.
- ☒ f. Items stored together in memory get used together. ✓

Spatial locality refers to the common feature of programs that items stored together in memory get used together

The correct answer is: Items stored together in memory get used together.



Mark 1.00 out of 1.00

Which of the following is the most accurate statement relating to the term *virtual memory*?

Select one:

- ☐ a. Allows programmers to write sloppy code.
- ☐ b. Allows secondary storage (e.g. hard disk) to play the role of the cache.
- ☐ c. Don't know/no answer
- ☐ d. Allows the cache hit rate to be increased.
- ☐ e. Allows the DRAM capacity to be increased.
- ☒ f. Allows secondary storage (e.g. hard disk) to play the role of main memory. ✓ The basic idea of VM is that the disk is used to support extra virtual pages of main memory

Virtual memory allows secondary storage (e.g. hard disk) to play the role of main memory.

The correct answer is: Allows secondary storage (e.g. hard disk) to play the role of main memory.

### Question 7

Correct

Mark 1.00 out of 1.00

Suppose the cache access time is 10ns, main memory access time is 200ns and the cache hit rate is 90%. What is the EAT for the processor to access an item in the cache?

Select one:

- ☐ a. 10ns for 90% of the times.
- ☐ b. 10ns
- ☒ c. 29ns ✓
- ☐ d. Don't know/no answer
- ☐ e. 200ns
- ☐ f. 210ns

$$\text{EAT} = 0.9 \times 10\text{ns} + (1 - 0.9) \times 200\text{ns} = 29\text{ns}$$

The correct answer is: 29ns



Mark 1.00 out of 1.00

Assume a computer having a cache whose block size is 1024 bytes. Which of the following programs would lead the most effective use of the sequential locality?

Select one:

- ☐ a. A program that reads 2000 data points from a file and prints them to the computer terminal.
- ☐ b. A program with 50 instructions that reads and transforms data in a file which can grow dynamically.
- ☐ c. Do know the answer.
- ☒ d. A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points. ✓
- ☐ e. A program with 900 instructions that processes an array with 300 data points.
- ☐ f. A program with that computes the sum of 9999 numbers stored in a file.

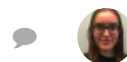
Sequential locality refers to the common feature of programs that instructions and data tend to be accessed sequentially.

As the block size of the computer is 1024 bytes only the program with the 800 instructions processing the array of 200 data points would be possible to fit in one block and thus execute as many times as required without the need to transfer further data and/or instructions from the main memory to the cache. The existence of a loop in this program would not affect sequential locality either since the jump from the last to the first instruction of the loop in the program would not cause any transfers to and from the main memory because all instructions of the program can fit in the cache and would be loaded at the start of the program's execution.

All other options given may lead to data/instructions transfers between cache and the main memory thus violating sequential locality.

The correct answer is: A program with 800 instructions executed within a loop that can be executed several times processing an array with 200 data points.





Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- ☐ a. Don't know/no answer
- ☐ b. 4
- ☒ c. 3
- ☐ d. 16
- ☐ e. 5
- ☐ f. 8



The total size of the tag, block and offset fields is 16.

16 blocks of cache can be indexed with 4 bits ( $16 = 2^4$ ), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits ( $8 = 2^3$ ); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is:  $16 - 4 - 3 = 9$ .

The correct answer is: 3

#### Question 10

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 64 blocks where each block contains 16 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- ☐ a. T= 24 , O= 4 and B = 4
- ☒ b. T= 22 , O= 4 and B = 6
- ☐ c. T= 28 , O= 2 and B = 2
- ☐ d. Don't know/no answer
- ☐ e. T= 8 , O= 16 and B = 8
- ☐ f. T= 16 , O= 8 and B = 8



As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them ( $4,294,967,296 = 2^{32}$ ). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 64 blocks, it can be indexed with 6 bits ( $64 = 2^6$ ). So the size of the block field (B) is 6.

As each block has 16 bytes, it can be indexed with 4 bits ( $16 = 2^4$ ). So the size of the offset field (O) is 4.

Thus, the tag (T) field is:  $TBO - B - O = 32 - 6 - 4 = 22$ .

The correct answer is: T= 22 , O= 4 and B = 6