IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 32 D flip-flops.
- b. 64 D flip-flops ✔
- c. 64 RS flip-flips
- d. 32 D flip-flops and 32 RS flip-flops
- e. 32 D flip-flops and 16 RS flip-flops.
- f. Don't know/no answer

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

Mark 1.00 out of 1.00

Which of the following is the correct sequence of steps undertaken when a cache miss occurs?

Select one:

- a. Activate memory controller, stall processor, request data item from lower level of hierarchy, load data item into cache, resume processor.
- b. Stall processor, request data item from lower level of hierarchy, load data item into cache, activate memory controller, resume processor.
- c. Activate memory controller, request data item from lower level of hierarchy, stall processor, load data item into cache, resume processor.
- d. Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor. ✔
- e. Stall processor, request data item from lower level of hierarchy, activate memory controller, load data item into cache, resume processor.
- f. Don't know/no answer

The correct sequence of steps is: stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct answer is: Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

Question **3**

Correct

Mark 1.00 out of 1.00

A 24-bit address generates an address space of _____ locations.
(select a value below to fill in the blank)

Select one:

- a. 4096
- b. 16,777,216 ✔
- c. 1024
- d. 4,294,967,296

Your answer is correct.

The number of addressable locations in the system is called an address space. The answer is 2 to the power 24 = 16,777,216.

The correct answer is: 16,777,216

Mark 1.00 out of 1.00

Which of the following is the most accurate statement relating to the term *virtual memory*?

Select one:

- a. Allows secondary storage (e.g. hard disk) to play the role of main memory. ✔ The basic idea of VM is that the disk is used to support extra virtual pages of main memory
- b. Allows the cache hit rate to be increased.
- c. Allows secondary storage (e.g. hard disk) to play the role of the cache.
- d. Allows the DRAM capacity to be increased.
- e. Allows programmers to write sloppy code.
- f. Don't know/no answer

Virtual memory allows secondary storage (e.g. hard disk) to play the role of main memory.

The correct answer is: Allows secondary storage (e.g. hard disk) to play the role of main memory.

Question **5**

Correct

Mark 1.00 out of 1.00

The reason for the implementation of the cache memory is?

Select one:

- a. To mitigate the difference in speeds of operation of the processor and memory ✔
- b. All of the mentioned
- c. To increase the internal memory of the system
- d. To reduce the memory access and cycle time

Your answer is correct.

The correct answer is "to mitigate the difference in speeds of operation of the processor and memory". Cache will not increase the physical memory size or reduce the memory access and cycle time

The correct answer is: To mitigate the difference in speeds of operation of the processor and memory

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Block 1
- b. Block 64
- c. Block 1024
- d. Block 799 ✔
- e. Block 573
- f. Don't know/no answer

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits ($1024 = 2^{10}$), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits ($32 = 2^5$) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

TAG (32nd to 16th) BLOCK (15th to 6th bit) OFFSET (5th to 1st bit)

The hexadecimal address $000063FA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 111**1 1010

And if we convert $110\ 0011\ 111_{bin}$ to decimal, we get 799_{dec} So the given address will map to block 799 in cache.

The correct answer is: Block 799

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000053AA_{16}$ map?

Select one:

- a. Block 201
- b. Block 124
- c. Don't know/no answer
- d. Block 334 ✔
- e. Block 512
- f. Block 58

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32^{nd} to 16^{th}) BLOCK (15^{th} to 7^{th} bit) OFFSET (6^{th} to 1^{st} bit)

The hexadecimal address $000053AA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0101 0011 1010 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**101 0011 10**10 1010

And if we convert 101001110_{bin} to decimal, we get 334_{dec} So the given address will map to block 334 in cache.

The correct answer is: Block 334

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 16 blocks where each block contains 16 bytes. Determine the size of the offset field in the memory addresses used by this computer.

Select one:

- a. Don't know/no answer
- b. 5
- c. 32
- d. 16
- e. 3
- f. 4 ✔

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset fields is 32.

As the cache gas 16 blocks, it can be indexed with 4 bits (16 = 2^4), so the size of the block field is 4 bits.

As each block has 16 bytes, we need 4 bits for the offset field to access each byte in the block (16=2^4) bytes .

Finally, the tag field is: 32 - 4 - 4 = 24.

The correct answer is: 4

Question **9**

Correct

Mark 1.00 out of 1.00

Which of the following flip-flops is most often used to construct SRAM?

Select one:

- a. RS flip-flip
- b. J flip-flip
- c. D flip-flop ✔
- d. SR flip-flop
- e. Clocked RS flip-flip
- f. Don't know/no answer

A D flip-flip is the form of flip-flop used in SRAM as one (D) input specifies what is to be written.

The correct answer is: D flip-flop

Mark 1.00 out of 1.00

Which of the following *best* describes why a memory hierarchy is needed?

Select one:

- a. Processor speeds have increased faster than SRAM speeds.
- b. SRAM is cheaper than DRAM per unit of memory.
- c. It is useful to be able to exceed physical memory limits.
- d. DRAM is cheaper than SRAM per unit of memory.
- e. Don't know/no answer
- f. Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs. ✔

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

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