IN1006 Systems Architecture (PRD1 A 2022/23)

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State	Finished
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Time taken	10 mins 54 secs
Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 3 ✔
- b. 16
- c. 4
- d. 5
- e. 8
- f. Don't know/no answer

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 3

Question **2**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000053AA_{16}$ map?

Select one:

- a. Don't know/no answer
- b. Block 124
- c. Block 201
- d. Block 58
- e. Block 334 ✔
- f. Block 512

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

TAG (32^{nd} to 16^{th}) BLOCK (15^{th} to 7^{th} bit) OFFSET (6^{th} to 1^{st} bit)

The hexadecimal address $000053AA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0101 0011 1010 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**101 0011 10**10 1010

And if we convert 101001110_{bin} to decimal, we get 334_{dec} So the given address will map to block 334 in cache.

The correct answer is: Block 334

Question **3**

Correct

Mark 1.00 out of 1.00

Which of the following is the most accurate statement relating to the term *virtual memory*?

Select one:

- a. Allows programmers to write sloppy code.
- b. Don't know/no answer
- c. Allows secondary storage (e.g. hard disk) to play the role of the cache.
- d. Allows the DRAM capacity to be increased.
- e. Allows the cache hit rate to be increased.
- f. Allows secondary storage (e.g. hard disk) to play the role of main memory. ✔ The basic idea of VM is that the disk is used to support extra virtual pages of main memory

Virtual memory allows secondary storage (e.g. hard disk) to play the role of main memory.

The correct answer is: Allows secondary storage (e.g. hard disk) to play the role of main memory.

Question **4**

Correct

Mark 1.00 out of 1.00

Which of the following is a pair of non-volatile memories?

Select one:

- a. DRAM and Flash
- b. DRAM and SRAM
- c. ROM and Flash ✔
- d. SRAM and EEPROM
- e. EPROM and DRAM

The volatile memories in the question are SRAM, VRAM and DRAM, The only option that does not contain any of them is the answer.

The correct answer is: ROM and Flash

Question **5**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 32 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 28 , O= 2 and B = 2
- b. T= 24 , O= 4 and B = 4
- c. Don't know/no answer
- d. T= 22 , O= 5 and B = 5 ✔
- e. T= 8 , O= 16 and B = 8
- f. T= 16 , O= 8 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 32 blocks, it can be indexed with 5 bits (32 = 2^5), so the size of the block (B) field is 5 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 5 - 5 = 22.

The correct answer is: T= 22 , O= 5 and B = 5

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 4
- b. 16
- c. 3
- d. 8 ✔
- e. Don't know/no answer
- f. 32

Your answer is correct.

The total size of the tag, block and offset fields is 16.

32 = 2^5 blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has 8=2^3 bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 8

Question **7**

Correct

Mark 1.00 out of 1.00

Which type of memory is built with capacitors that slowly leak their charge hence they must be refreshed every few milliseconds to prevent data loss?

Select one:

- a. DRAM ✔
- b. Registers
- c. Cache
- d. SRAM

Your answer is correct.

The correct answer is: DRAM

Question **8**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 64 blocks where each block contains 16 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 24 , O= 4 and B = 4
- b. Don't know/no answer
- c. T= 28 , O= 2 and B = 2
- d. T= 8 , O= 16 and B = 8
- e. T= 16 , O= 8 and B = 8
- f. T= 22 , O= 4 and B = 6 ✔

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 64 blocks, it can be indexed with 6 bits (64 = 2^6). So the size of the block field (B) is 6.

As each block has 16 bytes, it can be indexed with 4 bits (16 = 2^4). So the size of the offset field (B) is 4.

Thus , the tag (T) field is: TBO - B - O = 32 - 6 - 4 = 22.

The correct answer is: T= 22 , O= 4 and B = 6

Question **9**

Correct

Mark 1.00 out of 1.00

Which of the following statements about ROM is correct?

- a. ROM is a type of L2 cache memory.
- b. ROM is needed to support the mapping of cache memory addresses to main memory addresses.
- c. ROM stores the program that boots a computer. ✔
- d. ROM stores the operating system of a computer.
- e. ROM is a type of L1 cache memory.

Your answer is correct.

ROM stores the program that boots a computer.

The correct answer is:
ROM stores the program that boots a computer.

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 32 D flip-flops and 32 RS flip-flops
- b. 64 RS flip-flips
- c. 32 D flip-flops.
- d. Don't know/no answer
- e. 32 D flip-flops and 16 RS flip-flops.
- f. 64 D flip-flops ✔

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

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