IN1006 Systems Architecture (PRD1 A 2022/23)

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Time taken	25 mins 1 sec
Grade	8.80 out of 10.00 (88%)

Question 1

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *temporal locality*?

Select one:

- a. Items stored together in memory get used together.
- b. Items get removed from the cache based on the order that they enter.
- c. Items get written to memory locations in the order that the processor accesses the memory locations.
- d. Items get placed in cache positions in the order that they enter.
- e. Don't know/no answer
- f. Items in memory tend to get used more than once when accessed. ✔

Temporal locality refers to the common feature of programs that items in memory tend to get used more than once when accessed.

The correct answer is: Items in memory tend to get used more than once when accessed.

Question 2

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 16
- b. 5
- c. 3 ✔
- d. Don't know/no answer
- e. 4
- f. 8

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 3

Question 3

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 128 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 20 , O= 5 and B = 7 ✔
- b. T= 28 , O= 2 and B = 2
- c. Don't know/no answer
- d. T= 24 , O= 4 and B = 4
- e. T= 16 , O= 8 and B = 8
- f. T= 8 , O= 16 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 128 blocks, it can be indexed with 7 bits (128 = 2^7), so the size of the block (B) field is 7 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 7 - 5 = 20.

The correct answer is: T= 20 , O= 5 and B = 7

Question 4

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 16
- b. 32
- c. 4
- d. 8 ✔
- e. Don't know/no answer
- f. 3

Your answer is correct.

The total size of the tag, block and offset fields is 16.

32 = 2^5 blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has 8=2^3 bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 8

Question 5

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 16 blocks where each block contains 16 bytes. Determine the size of the tag field in the memory addresses used by this computer.

Select one:

- a. 3
- b. 16
- c. 32
- d. Don't know/no answer
- e. 24 ✔
- f. 5

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset fields is 32.

As the cache gas 16 blocks, it can be indexed with 4 bits (16 = 2^4), so the size of the block field is 4 bits.

As each block has 16 bytes, we need 4 bits for the offset field to access each byte in the block (16=2^4) bytes .

Finally, the tag field is: 32 - 4 - 4 = 24.

The correct answer is: 24

Question 6

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 8
- b. 5
- c. 3
- d. 4 ✔
- e. 16
- f. Don't know/no answer

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 4

Question 7

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 8
- b. 5
- c. Don't know/no answer
- d. 16
- e. 9 ✔
- f. 4

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 9

Question 8

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Block 799 ✔
- b. Block 1
- c. Block 64
- d. Block 573
- e. Don't know/no answer
- f. Block 1024

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits ($1024 = 2^{10}$), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits ($32 = 2^5$) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

TAG (32nd to 16th) BLOCK (15th to 6th bit) OFFSET (5th to 1st bit)

The hexadecimal address $000063FA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0110 0011 1111 1010

And if we convert $110\ 0011\ 111_{bin}$ to decimal, we get 799_{dec} So the given address will map to block 799 in cache.

The correct answer is: Block 799

Question 9

Incorrect

Mark -0.20 out of 1.00

Which of the following flip-flops is most often used to construct SRAM?

Select one:

- a. J flip-flip
- b. Don't know/no answer
- c. RS flip-flip
- d. Clocked RS flip-flip
- e. SR flip-flop ✖
- f. D flip-flop

A D flip-flip is the form of flip-flop used in SRAM as one (D) input specifies what is to be written.

The correct answer is: D flip-flop

Question 10

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 64 RS flip-flips
- b. Don't know/no answer
- c. 32 D flip-flops and 32 RS flip-flops
- d. 64 D flip-flops ✔
- e. 32 D flip-flops and 16 RS flip-flops.
- f. 32 D flip-flops.

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

◄ Quiz 5 _ Weekly Assessed Quiz 2022

Jump to...

Quiz 7 _ Weekly Assessed Quiz 2022 ►

Quiz navigation

1 2 3 4 5 6 7 8 9 10

Show one page at a time

Finish review