IN1006 Systems Architecture (PRD1 A 2022/23)

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State	Finished
Completed on	Thursday, 8 December 2022, 5:25 PM
Time taken	21 mins 43 secs
Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 32 D flip-flops and 16 RS flip-flops.
- b. Don't know/no answer
- c. 32 D flip-flops and 32 RS flip-flops
- d. 32 D flip-flops.
- e. 64 D flip-flops ✔
- f. 64 RS flip-flips

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

Question **2**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 16
- b. Don't know/no answer
- c. 32
- d. 4
- e. 3
- f. 8 ✔

Your answer is correct.

The total size of the tag, block and offset fields is 16.

32 = 2^5 blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has 8=2^3 bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 8

Question **3**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Select one:

- a. 8
- b. 9 ✔
- c. 16
- d. 4
- e. Don't know/no answer
- f. 5

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits (32 = 2^4), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits (8=2^3); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 9

Question **4**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 5
- b. 16
- c. Don't know/no answer
- d. 8
- e. 3 ✔
- f. 4

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits ($32 = 2^4$), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits ($8=2^3$); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 3

Question **5**

Correct

Mark 1.00 out of 1.00

Which of the following is the correct sequence of steps undertaken when a cache miss occurs?

Select one:

- a. Don't know/no answer
- b. Activate memory controller, request data item from lower level of hierarchy, stall processor, load data item into cache, resume processor.
- c. Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor. ✔
- d. Activate memory controller, stall processor, request data item from lower level of hierarchy, load data item into cache, resume processor.
- e. Stall processor, request data item from lower level of hierarchy, activate memory controller, load data item into cache, resume processor.
- f. Stall processor, request data item from lower level of hierarchy, load data item into cache, activate memory controller, resume processor.

The correct sequence of steps is: stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct answer is: Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

Question **6**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 8
- b. 5
- c. 32
- d. 3 ✔
- e. Don't know/no answer
- f. 16

The total size of the tag, block and offset fields is 16.
$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 3

Question **7**

Correct

Mark 1.00 out of 1.00

The reason for the implementation of the cache memory is?

Select one:

- a. To mitigate the difference in speeds of operation of the processor and memory ✔
- b. To reduce the memory access and cycle time
- c. To increase the internal memory of the system
- d. All of the mentioned

Your answer is correct.

The correct answer is "to mitigate the difference in speeds of operation of the processor and memory". Cache will not increase the physical memory size or reduce the memory access and cycle time

The correct answer is: To mitigate the difference in speeds of operation of the processor and memory

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following statements about ROM is correct?

- a. ROM stores the operating system of a computer.
- b. ROM is needed to support the mapping of cache memory addresses to main memory addresses.
- c. ROM is a type of L2 cache memory.
- d. ROM stores the program that boots a computer. ✔
- e. ROM is a type of L1 cache memory.

Your answer is correct.

ROM stores the program that boots a computer.

The correct answer is:
ROM stores the program that boots a computer.

Question **9**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *temporal locality*?

Select one:

- a. Items get removed from the cache based on the order that they enter.
- b. Don't know/no answer
- c. Items get placed in cache positions in the order that they enter.
- d. Items stored together in memory get used together.
- e. Items in memory tend to get used more than once when accessed. ✔
- f. Items get written to memory locations in the order that the processor accesses the memory locations.

Temporal locality refers to the common feature of programs that items in memory tend to get used more than once when accessed.

The correct answer is: Items in memory tend to get used more than once when accessed.

Question **10**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 16 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 4 ✔
- b. Don't know/no answer
- c. 5
- d. 8
- e. 3
- f. 16

The total size of the tag, block and offset fields is 16.
16 blocks of cache can be indexed with 4 bits ($32 = 2^4$), so block needs 4 bits.

Each block has 8 bytes so it can be indexed with 3 bits ($8=2^3$); thus 3 bits are needed for the offset to determine the address of each byte within a block.

Finally, the tag field is: 16 - 4 - 3 = 9.

The correct answer is: 4

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