# IN1006 Systems Architecture (PRD1 A 2022/23)



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| **Started on** | Thursday, 8 December 2022, 6:00 PM |
| **State** | Finished |
| **Completed on** | Thursday, 8 December 2022, 6:25 PM |
| **Time taken** | 25 mins |
| **Grade** | **8.90** out of 10.00 (**89**%) |

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the following is a pair of non-volatile memories?

Select one:

- a. DRAM and Flash
- b. DRAM and SRAM
- c. SRAM and EEPROM
- d. EPROM and DRAM
- e. ROM and Flash ✔

The volatile memories in the question are SRAM, VRAM and DRAM, The only option that does not contain any of them is the answer.

The correct answer is: ROM and Flash

Question **2**

Correct

Mark 1.00 out of 1.00

Which of the following statements about the different types of memory that can be found in a computer is correct?

- a. A computer cannot operate without virtual memory.
- b. A computer can operate without a ROM.
- c. A computer can operate without a cache and secondary memory. ✔
- d. A computer must always have a full memory hierarchy with L1 cache, L2 cache, RAM and secondary memory.
- e. A computer can operate without a RAM.

Your answer is correct.

The correct answer is:
A computer can operate without a cache and secondary memory.

Question **3**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *temporal locality*?

Select one:

- a. Items get placed in cache positions in the order that they enter.
- b. Items get written to memory locations in the order that the processor accesses the memory locations.
- c. Items in memory tend to get used more than once when accessed. ✔
- d. Don't know/no answer
- e. Items stored together in memory get used together.
- f. Items get removed from the cache based on the order that they enter.

Temporal locality refers to the common feature of programs that items in memory tend to get used more than once when accessed.

The correct answer is: Items in memory tend to get used more than once when accessed.

Question **4**

Correct

Mark 1.00 out of 1.00

Suppose the cache access time is 10ns, main memory access time is 200ns and the cache hit rate is 90%. What is the EAT for the processor to access an item in the cache?

Select one:

- a. 10ns for 90% of the times.
- b. 200ns
- c. 10ns
- d. 29ns ✔
- e. Don't know/no answer
- f. 210ns

EAT = 0.9*10ns + (1-0.9)*200ns = 29ns

The correct answer is: 29ns

Question **5**

Correct

Mark 1.00 out of 1.00

Which of the following is the correct sequence of steps undertaken when a cache miss occurs?

Select one:

- a. Stall processor, request data item from lower level of hierarchy, load data item into cache, activate memory controller, resume processor.
- b. Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor. ✔
- c. Stall processor, request data item from lower level of hierarchy, activate memory controller, load data item into cache, resume processor.
- d. Don't know/no answer
- e. Activate memory controller, request data item from lower level of hierarchy, stall processor, load data item into cache, resume processor.
- f. Activate memory controller, stall processor, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct sequence of steps is: stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

The correct answer is: Stall processor, activate memory controller, request data item from lower level of hierarchy, load data item into cache, resume processor.

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following flip-flops is most often used to construct SRAM?

Select one:

- a. D flip-flop ✔
- b. J flip-flip
- c. Don't know/no answer
- d. SR flip-flop
- e. RS flip-flip
- f. Clocked RS flip-flip

A D flip-flip is the form of flip-flop used in SRAM as one (D) input specifies what is to be written.

The correct answer is: D flip-flop

Question **7**

Incorrect

Mark -0.10 out of 1.00

Suppose the cache access time of a computer is 10ns and its main memory access time is 15 times slower. Assuming that the cache hit rate is 70%, what is the effective access time (EAT) for the processor to access an item in the cache?

Select one:

- a. 10ns
- b. 200ns
- c. 210ns for 30% of the times
- d. Don't know/no answer
- e. 52ns
- f. 52ns for 90% of the times. ✖

Your answer is incorrect.

EAT = 0.7*10ns + (1-0.7)*150ns = 52ns

The correct answer is: 52ns

Question **8**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of $2^{32}$ bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Don't know/no answer
- b. Block 1
- c. Block 573
- d. Block 799 ✔
- e. Block 64
- f. Block 1024

As the computer has a memory with $2^{32}$ bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits ($1024 = 2^{10}$), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits ($32 = 2^5$) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

**TAG (32nd to 16th) BLOCK (15th to 6th bit) OFFSET (5th to 1st bit)**

The hexadecimal address $000063FA_{16}$ corresponds to the binary address:

**0000 0000 0000 0000 0110 0011 1111 1010**

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 111**1 1010

And if we convert $110\ 0011\ 111_{bin}$ to decimal, we get $799_{dec}$ So the given address will map to block 799 in cache.

The correct answer is: Block 799

Question **9**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of $2^{32}$ bytes and a direct mapped cache of 512 blocks each of which containing 64 bytes. To which cache block the main memory address $000053AA_{16}$ map?

Select one:

- a. Block 334 ✔
- b. Block 58
- c. Block 201
- d. Block 124
- e. Don't know/no answer
- f. Block 512

As the computer has a memory with $2^{32}$ bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 512 blocks, it can be indexed with 9 bits ($512 = 2^9$), so the size of the block (B) field is 9 bits.

As each block has 64 bytes, so it can be indexed with 64 bits ($64 = 2^6$) or, equivalently, the offset (O) field must be 6 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 9 - 6 = 17.

Consequently the memory address format will be

**TAG ($32^{nd}$ to $16^{th}$) BLOCK ($15^{th}$ to $7^{th}$ bit) OFFSET ($6^{th}$ to $1^{st}$ bit)**

The hexadecimal address $000053AA_{16}$ corresponds to the binary address:

**0000 0000 0000 0000 0101 0011 1010 1010**

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**101 0011 10**10 1010

And if we convert $101001110_{bin}$ to decimal, we get $334_{dec}$ So the given address will map to block 334 in cache.

The correct answer is: Block 334

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following *best* describes why a memory hierarchy is needed?

Select one:

- a. Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs. ✔
- b. SRAM is cheaper than DRAM per unit of memory.
- c. Don't know/no answer
- d. DRAM is cheaper than SRAM per unit of memory.
- e. Processor speeds have increased faster than SRAM speeds.
- f. It is useful to be able to exceed physical memory limits.

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

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