IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	10.00 out of 10.00 (100%)

Question 1

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'stall'?

Select one:

- a. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- b. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- c. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.
- d. Waiting for the next instruction to be fetched after a branch is taken. ✔
- e. A gap in the pipeline where some or all of the stages are not processing an instruction.
- f. Don't know/no answer

A stall occurs in response to a control hazard. It involves waiting for the next instruction to be fetched after a branch is taken.

The correct answer is: Waiting for the next instruction to be fetched after a branch is taken.

Question 2

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. add d2, b2 ,c2
3. add d3, b3 ,c3
4. add d4, b4, c4
5. add d5, c5, b5

Which of the four architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

- a. MISD
- b. MIMD and MISD
- c. MIMD
- d. Do not know the answer
- e. SIMD ✔
- f. SISD

Your answer is correct.

Instructions 1-5 above are the same (add) and are executed upon different data. Thus, SIMD is the most suitable architecture.

The correct answer is: SIMD

Question 3

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below?

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 5
- b. 1 ✔
- c. 4
- d. 2
- e. 3
- f. Don't know/no answer

All instructions have some dependency with another.

The correct answer is: 1

Question 4

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. sub d, b ,c
3. add g, e ,d
4. add h, e, f
5. sub a, a, b

Select one:

- a. 3 ✔
- b. 4
- c. Don't know/no answer
- d. 5
- e. 2
- f. 1

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. Instructions 1 and 2 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2, 3 (i.e. d). However 3, 4, 5 have no dependences. Therefore the largest sized block of non-dependent instructions is 3. Mixing instruction types has no effect.

The correct answer is: 3

Question 5

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'control hazard'?

Select one:

- a. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- b. A gap in the pipeline where some or all of the stages are not processing an instruction.
- c. Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check. ✔
- d. Loading instructions into pipeline which try to access memory at the same stage.
- e. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.
- f. Don't know/no answer

Your answer is correct.

A control hazard occurs when an instruction I has been loaded to a pipeline although due to some condition check which is already being executed in the pipeline it turns out that I should not be executed.

The correct answer is: Executing an instruction in the pipeline whose execution depends upon a yet unknown condition check.

Question 6

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. lw $t1, 0($t0)
2. lw $t2, 1($t0)
3. add $t3, $t1, $t2
4. sw $t3, 0($t1)
5. lw $t4, 2($t0)
6. add $t5, $t1, $t4
7. sw $t5, 1($t1)
8. lw $t6, 3($t0)
9. add $t5, $t1, $t6
10. sw $t5, 2($t1)

Which of the following would offer the maximum protection against data hazards in this code without affecting the results of its execution, if a 5-stage pipeline is assumed?

- a. Move instruction 5 and instruction 8 before instruction 3. ✔
- b. Move instruction 5 and instruction 7 before instruction 3.
- c. Move instructions 3 and 4 after instruction 5.
- d. Move instructions 3 and 6 after instruction 10.
- e. Move instruction 5 before instruction 3.

Your answer is correct.

Data hazards in this code extract arise due to loading data immediately before the computations that use them as will make computations stall whilst waiting loading instructions to complete their execution.

Such hazards can be removed by moving instruction 5 before instruction 3 (this will avoid the hazard between instructions 2 and 3 and the hazard between instructions 5 and 6), and instruction 8 before instruction 3 (this will avoid the hazard between instructions 8 and 9).

The correct answer is:
Move instruction 5 and instruction 8 before instruction 3.

Question 7

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a ‘structural hazard’?

Select one:

- a. A gap in the pipeline where some or all of the stages are not processing an instruction.
- b. Don't know/no answer
- c. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- d. Waiting for the next instruction to be fetched after a branch is taken.
- e. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.
- f. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses. ✔

A structural hazard occurs when hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

The correct answer is: Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

Question 8

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below?

1. add a, b, c
2. sub d, b ,c
3. add g, e ,d
4. add h, e, f
5. sub a, a, b

Select one:

- a. 1
- b. 4
- c. 3 ✔
- d. Don't know/no answer
- e. 5
- f. 2

Instructions 1 and 2 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2, 3 (i.e. d). However 3, 4, 5 have no dependences. Therefore the largest size block of non-dependent instructions is 3. Mixing instruction types has no effect.

The correct answer is: 3

Question 9

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

```
add a, b, c
add c, b ,c
add f, c ,d
add h, e, f
add f, h, b
```

Select one:

- a. Don't know/no answer
- b. 3
- c. 1 ✔
- d. 5
- e. 2
- f. 4

Your answer is correct.

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. All instructions have some dependency with another.

The correct answer is: 1

Question 10

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add a, b, c
2. add b, b ,d
3. add f, e , a
4. add h, k, g
5. add m, a, b

Which of the following compiler optimisations could avoid data hazards in this code assuming a 4 stage pipeline (i.e., 1. fetch instruction; 2. Decode and load data; 3. Execute instruction; 4. Write to memory) with no forwarding?

- a. Move instruction 4 before instruction 3. ✔
- b. Do not know the answer.
- c. Move instructions 5 before instruction 4.
- d. No optimisations are possible.
- e. Move instruction 5 before instruction 3.

Your answer is correct.

The data hazards in this code arise due to instruction 3 (it depends on instruction 1).

Moving instruction 4 before instruction 3 will resolve the hazard as following the move instruction 3 will read data in cycle 5 and by this cycle instruction 1 will have stored its output.

The correct answer is:
Move instruction 4 before instruction 3.

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