IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	**10.00** out of 10.00 (**100**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Which of the following *best* describes why a memory hierarchy is needed?

Select one:

- a. SRAM is cheaper than DRAM per unit of memory.
- b. Don't know/no answer
- c. Processor speeds have increased faster than SRAM speeds.
- d. DRAM is cheaper than SRAM per unit of memory.
- e. Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs. ✔
- f. It is useful to be able to exceed physical memory limits.

The need for a memory hierarchy is driven by the increasing gap between the speed of the processor and the speed of main memory (though it has other useful applications, e.g. in allowing physical memory) and the different technologies of memory.

The correct answer is: Processor speeds have increased faster than memory speeds and there are different technologies of memory with different speeds and costs.

Question **2**

Correct

Mark 1.00 out of 1.00

Which of the following best describes a cache memory in *Harvard Architecture*?

Select one:

- a. An arrangement where the data and instruction caches are separated. ✔
- b. An arrangement where data and instructions appear in the same cache.
- c. A cache where the assignment of data items (blocks) to cache lines is determined by the last n-bits of the data item's address.
- d. A cache where the last n-bits of a block's address denotes which grouping of cache lines are used.
- e. Don't know/no answer
- f. A cache where each data item can be assigned to any block as needed.

The Harvard cache architecture refers to an arrangement where the data and instructions are split into separate caches.

The correct answer is: An arrangement where the data and instruction caches are separated.

Question **3**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of the concept of *sequential locality?*

Select one:

- a. Items stored together in memory get used together.
- b. Instructions tend to be accessed sequentially. ✔
- c. Don't know/no answer
- d. Items get placed in cache lines in the order that they enter.
- e. Items in memory tend to get used more than once when accessed.
- f. Items get removed from the cache based on the order that they enter.

Sequential locality refers to the common feature of programs that instructions tend to be accessed sequentially.

The correct answer is: Instructions tend to be accessed sequentially.

Question **4**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 32 blocks where each block contains 32 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 22 , O= 5 and B = 5 ✔
- b. T= 16 , O= 8 and B = 8
- c. Don't know/no answer
- d. T= 28 , O= 2 and B = 2
- e. T= 24 , O= 4 and B = 4
- f. T= 8 , O= 16 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 32 blocks, it can be indexed with 5 bits (32 = 2^5), so the size of the block (B) field is 5 bits.

As each block has 32 bytes, so it can be indexed with 5 bits (32 = 2^5) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 5 - 5 = 22.

The correct answer is: T= 22 , O= 5 and B = 5

Question **5**

Correct

Mark 1.00 out of 1.00

The reason for the implementation of the cache memory is?

Select one:

- a. To mitigate the difference in speeds of operation of the processor and memory ✔
- b. To reduce the memory access and cycle time
- c. All of the mentioned
- d. To increase the internal memory of the system

Your answer is correct.

The correct answer is "to mitigate the difference in speeds of operation of the processor and memory". Cache will not increase the physical memory size or reduce the memory access and cycle time

The correct answer is: To mitigate the difference in speeds of operation of the processor and memory

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following is the correct ordering of the following memory types in *decreasing* order of speed.

Select one:

- a. SRAM, flash memory, DRAM, hard disk drive.
- b. Hard disk drive, flash memory, DRAM, SRAM.
- c. Don't know/no answer
- d. SRAM, DRAM, flash memory, hard disk drive. ✔
- e. Hard disk drive, flash memory, SRAM, DRAM.
- f. flash memory, SRAM, DRAM, hard disk drive.

SRAM is the fastest type of memory, followed by DRAM, flash and hard disks.

The correct answer is: SRAM, DRAM, flash memory, hard disk drive.

Question **7**

Correct

Mark 1.00 out of 1.00

Suppose the cache access time of a computer is 10ns and its main memory access time is 15 times slower. Assuming that the cache hit rate is 70%, what is the effective access time (EAT) for the processor to access an item in the cache?

Select one:

- a. 200ns
- b. 52ns for 90% of the times.
- c. 52ns ✔
- d. 210ns for 30% of the times
- e. Don't know/no answer
- f. 10ns

Your answer is correct.

EAT = 0.7*10ns + (1-0.7)*150ns = 52ns

The correct answer is: 52ns

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 64 D flip-flops ✔
- b. 32 D flip-flops and 16 RS flip-flops.
- c. 64 RS flip-flips
- d. 32 D flip-flops.
- e. 32 D flip-flops and 32 RS flip-flops
- f. Don't know/no answer

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

Question **9**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Select one:

- a. 8
- b. Don't know/no answer
- c. 16
- d. 32
- e. 3 ✔
- f. 5

The total size of the tag, block and offset fields is 16.
$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 3

Question **10**

Correct

Mark 1.00 out of 1.00

Assume a computer having a main memory of 2^{32} bytes and a direct mapped cache of 1024 blocks each of which containing 32 bytes. To which cache block the main memory address $000063FA_{16}$ map?

Select one:

- a. Block 1
- b. Block 64
- c. Block 799 ✔
- d. Block 1024
- e. Don't know/no answer
- f. Block 573

As the computer has a memory with 2^{32} bytes, it will need 32 bits to identify the addresses of all of them. Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 1024 blocks, it can be indexed with 10 bits ($1024 = 2^{10}$), so the size of the block (B) field is 10 bits.

As each block has 32 bytes, so it can be indexed with 5 bits ($32 = 2^5$) or, equivalently, the offset (O) field must be 5 bits long.

Thus , the tag (T) field is: TBO - B - O = 32 - 10 - 5 = 17.

Consequently the memory address format will be

TAG (32^{nd} to 16^{th}) BLOCK (15^{th} to 6^{th} bit) OFFSET (5^{th} to 1^{st} bit)

The hexadecimal address $000063FA_{16}$ corresponds to the binary address:

0000 0000 0000 0000 0110 0011 1111 1010

So the block part in this address consists of the bold bits below:

0000 0000 0000 0000 0**110 0011 111**1 1010

And if we convert 110 0011 111_{bin} to decimal, we get 799_{dec} So the given address will map to block 799 in cache.

The correct answer is: Block 799

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