IN1006 Systems Architecture (PRD1 A 2022/23)

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Time taken	22 mins 39 secs
Grade	**8.90** out of 10.00 (**89**%)

Question **1**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below?

1. add a, b, c
2. sub d, b ,c
3. add g, e ,d
4. add h, e, f
5. sub a, a, b

Select one:

- a. 1
- b. 5
- c. 2
- d. 4
- e. 3 ✔
- f. Don't know/no answer

Instructions 1 and 2 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2, 3 (i.e. d). However 3, 4, 5 have no dependences. Therefore the largest size block of non-dependent instructions is 3. Mixing instruction types has no effect.

The correct answer is: 3

Question **2**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below?

1. add a, b, c
2. add c, b ,c
3. add f, c ,d
4. add h, e, f
5. add f, h, b

Select one:

- a. 2
- b. 3
- c. 5
- d. Don't know/no answer
- e. 4
- f. 1 ✔

All instructions have some dependency with another.

The correct answer is: 1

Question **3**

Incorrect

Mark -0.10 out of 1.00

Consider the following MIPS code:

```
1. lw  $t1, 0($t0)
2. lw  $t2, 1($t0)
3. add  $t3, $t1, $t2
4. sw  $t3, 0($t1)
5. lw  $t4, 2($t0)
6. add  $t5, $t1, $t4
7. sw  $t5, 1($t1)
8. lw  $t6, 3($t0)
9. add  $t5, $t1, $t6
10. sw  $t5, 2($t1)
```

Which of the following would offer the maximum protection against data hazards in this code without affecting the results of its execution, if a 5-stage pipeline is assumed?

a. Move instruction 5 and instruction 8 before instruction 3.
b. Move instruction 5 and instruction 7 before instruction 3.
c. Move instructions 3 and 6 after instruction 10. ✖
d. Move instructions 3 and 4 after instruction 5.
e. Move instruction 5 before instruction 3.

Your answer is incorrect.

Data hazards in this code extract arise due to loading data immediately before the computations that use them as will make computations stall whilst waiting loading instructions to complete their execution.

Such hazards can be removed by moving instruction 5 before instruction 3 (this will avoid the hazard between instructions 2 and 3 and the hazard between instructions 5 and 6), and instruction 8 before instruction 3 (this will avoid the hazard between instructions 8 and 9).

The correct answer is:
Move instruction 5 and instruction 8 before instruction 3.

Question **4**

Correct

Mark 1.00 out of 1.00

How many superscalar execution units could be used for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,d
4. add h, e, f
5. add f, a, b

Select one:

- a. Don't know/no answer
- b. 4
- c. 3
- d. 5
- e. 1
- f. 2 ✔

The number of execution units that can be used is limited to the largest sized block of non-dependent instructions. In the above block,

- Instructions 1, 2, do not depend on each other.
- Instruction 3 depends on instruction 2 (due to d)
- There is a dependency between 4 and 5 (due to f).

Therefore the largest size block of non-dependent instructions is 2.

The correct answer is: 2

Question **5**

Correct

Mark 1.00 out of 1.00

Consider the following MIPS code:

1. add d1, b1, c1
2. add d2, b2 ,c2
3. add d3, b3 ,c3
4. add d4, b4, c4
5. add d5, c5, b5

Which of the four architectures in the Flynn taxonomy would be best suited for executing the above code?

Select one:

- a. Do not know the answer
- b. MISD
- c. SISD
- d. MIMD and MISD
- e. MIMD
- f. SIMD ✔

Your answer is correct.

Instructions 1-5 above are the same (add) and are executed upon different data. Thus, SIMD is the most suitable architecture.

The correct answer is: SIMD

Question **6**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'data hazard'?

Select one:

- a. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- b. Waiting for the next instruction to be fetched after a branch is taken.
- c. A gap in the pipeline where some or all of the stages are not processing an instruction.
- d. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- e. Don't know/no answer
- f. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions. ✔

A data hazard occurs when an instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

The correct answer is: Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'stall'?

Select one:

- a. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.
- b. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- c. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.
- d. Waiting for the next instruction to be fetched after a branch is taken. ✔
- e. Don't know/no answer
- f. A gap in the pipeline where some or all of the stages are not processing an instruction.

A stall occurs in response to a control hazard. It involves waiting for the next instruction to be fetched after a branch is taken.

The correct answer is: Waiting for the next instruction to be fetched after a branch is taken.

Question **8**

Correct

Mark 1.00 out of 1.00

What is the maximum number of instructions that can be executed simultaneously for the MIPS pseudo-code below? Assume no register forwarding.

1. add a, b, c
2. add d, b ,c
3. add g, e ,c
4. add h, e, d
5. add f, a, b

Select one:

- a. 2
- b. Don't know/no answer
- c. 1
- d. 4
- e. 3 ✔
- f. 5

Instructions 1, 2 and 3 can be executed at the same time (they can share inputs as they have not changed). There is a dependency between 2 and 4 (i.e. d – the MIPS pipeline has two stages between execution and write to register). However 3, 4, 5 have no dependences. Therefore the largest size block of non-dependent instructions is 3.

The correct answer is: 3

Question **9**

Correct

Mark 1.00 out of 1.00

In what way are compilers usually used to prevent pipeline hazards?

Select one:

- a. Preventing data hazards by releasing the results before they are written to the registers.
- b. Don't know/no answer
- c. Use of deep pipelines to maximise throughput.
- d. Rearrange instructions such that an instruction that does not affect the decision is executed after the decision filling the bubble that would occur if the pipeline were to stall.
- e. A method to avoid control hazards by predicting what way a conditional branch instruction will execute in advance.
- f. Rearranging the instructions to avoid data hazards where possible. ✔

Compliers can be used to rearrange the instructions to avoid data hazards.

The correct answer is: Rearranging the instructions to avoid data hazards where possible.

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following is the best description of a 'structural hazard'?

Select one:

- a. Loading instructions into pipeline before the result of a decision is known, e.g. loading instructions after a branch
- b. A gap in the pipeline where some or all of the stages are not processing an instruction.
- c. Don't know/no answer
- d. Waiting for the next instruction to be fetched after a branch is taken.
- e. Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses. ✔
- f. Instruction depends upon the results of a previous instruction still in the pipeline, e.g. compound math expressions.

A structural hazard occurs when hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

The correct answer is: Hardware cannot support a combination of instructions in the same clock cycle, e.g. two simultaneous memory accesses.

◄ Quiz 6 _ Weekly Assessed Quiz 2022

Jump to...

Quiz navigation

1 2 3 4 5 6 7 9 10

Show one page at a time

Finish review