IN1006 Systems Architecture (PRD1 A 2022/23)

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Grade	**7.70** out of 10.00 (**77**%)

Question **1**

Incorrect

Mark -0.20 out of 1.00

Which of the following is a pair of non-volatile memories?

Select one:

- a. SRAM and EEPROM ✖
- b. ROM and Flash
- c. DRAM and SRAM
- d. EPROM and DRAM
- e. DRAM and Flash

The volatile memories in the question are SRAM, VRAM and DRAM, The only option that does not contain any of them is the answer.

The correct answer is: ROM and Flash

Question **2**

Correct

Mark 1.00 out of 1.00

What is a bit of SRAM constructed from?

Select one:

- a. Don't know/no answer
- b. Six transistors ✔
- c. One transistor and one capacitor
- d. Four transistors.
- e. Two capacitors and a floating-gate transistor.
- f. Three transistors and a floating-gate transistor.

A bit of SRAM is constructed from 6 transistors.

The correct answer is: Six transistors

Question **3**

Correct

Mark 1.00 out of 1.00

Suppose the cache access time is 10ns, main memory access time is 200ns and the cache hit rate is 90%. What is the EAT for the processor to access an item in the cache?

Select one:

- a. 29ns ✔
- b. 10ns for 90% of the times.
- c. 210ns
- d. Don't know/no answer
- e. 200ns
- f. 10ns

EAT = 0.9*10ns + (1-0.9)*200ns = 29ns

The correct answer is: 29ns

Question **4**

Correct

Mark 1.00 out of 1.00

Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Select one:

- a. 32
- b. Don't know/no answer
- c. 8
- d. 3
- e. 16
- f. 5 ✔

The total size of the tag, block and offset fields is 16.
$32 = 2^5$ blocks of cache can be indexed with 5 bits, so block is 5 bits.

Since each block has $8=2^3$ bytes we need 3 bits for the offset to access each byte in the block.

Finally, the tag field is: 16 - 5 - 3 = 8.

The correct answer is: 5

Question **5**

Incorrect

Mark -0.10 out of 1.00

Suppose we have a byte-addressable computer which has a memory of 4,294,967,296 addresses, a cache with 64 blocks where each block contains 16 bytes. What is the size of the block (B), offset (O) and the tag (T) fields in the memory addresses used by this computer.

Select one:

- a. T= 28 , O= 2 and B = 2
- b. T= 24 , O= 4 and B = 4 ✖
- c. Don't know/no answer
- d. T= 16 , O= 8 and B = 8
- e. T= 22 , O= 4 and B = 6
- f. T= 8 , O= 16 and B = 8

As the computer has a memory with 4,294,967,296 bytes, it will need 32 bits to identify the addresses of all of them (4,294,967,296 = 2^{32}). Thus, the total size of the tag, block and offset (TBO) fields is 32.

As the cache has 64 blocks, it can be indexed with 6 bits (64 = 2^6). So the size of the block field (B) is 6.

As each block has 16 bytes, it can be indexed with 4 bits (16 = 2^4). So the size of the offset field (B) is 4.

Thus , the tag (T) field is: TBO - B - O = 32 - 6 - 4 = 22.

The correct answer is: T= 22 , O= 4 and B = 6

Question **6**

Correct

Mark 1.00 out of 1.00

If a cache access requires one clock cycle and dealing with cache misses requires an additional five clock cycles, which of the following cache hit rates results in an effective access time of 2 clock cycles?

Select one:

- a. 85%
- b. 80% ✔
- c. 95%
- d. 90%
- e. Don't know/no answer
- f. 70%

The effective access time is calculated by: EAT = h *access_hit_time + (1-h) access_miss_time
where h is hit rate. In this case, access_hit_time = 1 clock cycle, access_miss_time = 1+5=6 clock cycles, and EAT = 2 clock cycles. So:

2 = h * 1 + (1-h) * 6 => -h+6h=6-2 => 5h = 4 > h = 4/5 or 80%

The correct answer is: 80%

Question **7**

Correct

Mark 1.00 out of 1.00

Which of the following best describes a *Harvard Architecture* cache?

Select one:

- a. An arrangement where the data and instruction caches are separated. ✔ This is the defining characteristic of a Harvard or split cache
- b. A cache where each data item can be assigned to any block as needed.
- c. A cache where the assignment of data items (blocks) to cache lines is determined by the last n-bits of the data item's address.
- d. An arrangement where data and instructions appear in the same cache.
- e. A cache where the last n-bits of a block's address denotes which grouping of cache lines are used.
- f. Don't know/no answer

The Harvard cache architecture refers to an arrangement where the data and instruction caches are separated.

The correct answer is: An arrangement where the data and instruction caches are separated.

Question **8**

Correct

Mark 1.00 out of 1.00

Which of the following is the correct ordering of the following memory types in *decreasing* order of speed.

Select one:

- a. Hard disk drive, flash memory, SRAM, DRAM.
- b. Don't know/no answer
- c. SRAM, flash memory, DRAM, hard disk drive.
- d. flash memory, SRAM, DRAM, hard disk drive.
- e. Hard disk drive, flash memory, DRAM, SRAM.
- f. SRAM, DRAM, flash memory, hard disk drive. ✔

SRAM is the fastest type of memory, followed by DRAM, flash and hard disks.

The correct answer is: SRAM, DRAM, flash memory, hard disk drive.

Question **9**

Correct

Mark 1.00 out of 1.00

Which of the following statements about ROM is correct?

- a. ROM is needed to support the mapping of cache memory addresses to main memory addresses.
- b. ROM is a type of L2 cache memory.
- c. ROM is a type of L1 cache memory.
- d. ROM stores the operating system of a computer.
- e. ROM stores the program that boots a computer. ✔

Your answer is correct.

ROM stores the program that boots a computer.

The correct answer is:
ROM stores the program that boots a computer.

Question **10**

Correct

Mark 1.00 out of 1.00

Which of the following best describes the composition of a 64-bit register.

Select one:

- a. 64 D flip-flops ✔
- b. 32 D flip-flops.
- c. Don't know/no answer
- d. 32 D flip-flops and 32 RS flip-flops
- e. 32 D flip-flops and 16 RS flip-flops.
- f. 64 RS flip-flips

A n-bit register is built from n-D flip-flips connected by a bus.

The correct answer is: 64 D flip-flops

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