Big thanks to Colin Kidder (https://github.com/collin80) for the following explanation of the STGAP1AS SPI gate driver traffic on the M3 rear drive unit :

Everything to and from the gate driver chip is an 8 bit value followed by an 8 bit CRC. This makes all transactions 16 bit chunks. Additionally, there must be 6 chips and they're all daisy chained. So, you constantly see 6 duplicate transactions all in a row. That causes all six chips to get their own copy of the transaction. Sometimes they are the same - just sending the same thing 6 times. Sometimes they are NOT the same. Sometimes the low side and high side are configured differently so be careful there.

The first thing it does is send 6 copies of 0xD0 32 (reset status registers).
Wait of about 87us.
0x2A DA (Start Configuration) 6 times
Wait 90us
0x8C A1 (write to register CFG1) 6 times
Wait 18us
0xAA 3D sets CFG1 to AA which means
- enable CRC on all commands
- don't enable VDD undervoltage monitoring
- [BAR]SD pin does reset status registers
- Diag2 pin works as input
- Dead time set to 800ns
- Input deglitch time set to 500ns
Wait 18us
0x9D D6 (write CFG2) six times
wait 31us
0x0D 03 which sets CFG2 to 0x0D which means:
- sense threshold 100mv
- desaturation current trigger at 500uA
- desat voltage threshold at 8 volts
Wait 68us
0x9E DF (write CFG3)
Wait 27us
0x60 38 which basically turns off 2 level turn off.
- It technically sets 2 level turn off to 13V
- but then sets the time to disabled
Wait 27us
0x9F D8 00 0C (Write CFG4 or NOP) Every other chip gets write CFG4 and the other gets NOP (no operation)
34us
0x16 68 00 0C (Set CFG4 to 0x16 on odd chips, NOP on even) This means:
- OVLO disabled (disable voltage monitoring on VH and VL)
- But, oddly enough, set OVLO to be latching
- Negative supply UVLO set to -3V
- Positive supply OVLO set to 12V
Wait 1/4 second
0x00 0C 9F D8 (NOP / Write CFG4) three times. So, now the other chips get CFG4 write
21us
0x00 0C 12 74 (NOP, set CFG4 to 0x12)
- OVLO disabled

- Latched
- Neg supply monitoring disabled.
- Pos supply 12V OVLO
Wait 34us
0x99 CA (CFG5 Write) all six the same
Wait 68uS
0x0A 42 (all six the same) Means:
- 2LTO mode always active (except it seems to have been disabled above)
- Miller clamp feature disabled
- Desat comparator enabled
- SENSE comparator disabled
Wait 24us
0x85 9E (Write DiagCfg1) - Sent to all chips as well
Wait 27us
0x7A BE (Write 0x7A to DiagCfg1) - Enabling something here causes that event to force DIAG1 pin low
- SPI Comm Fault Enabled
- VDD power supply fault enabled
- Undervolt fault enabled
- Overvolt fault enabled
- Desat and sense faults enabled
- ASC feedback DISABLED
- Thermal shutdown enabled
- Thermal warning DISABLED.
Wait 38us
0x86 97 (Write DiagCfg2) - To all chips
Wait 73us
0x00 E0 (write 00 to DiagCfg2) - Disable everything
Wait 27us
0x3A AA (Global reset) - To all chips
Wait 85us