Thanks to Colin Kidder for the following :

2.4MHz SPI

Unlock code: 1:0xAB; 2:0xEF; 3:0x56; 4:0x12
Lock code: 1: 0xDF; 2:0x34; 3:0xBE; 4:0xCA

You must unlock to change/read protected registers but that data only takes effect when you re-lock the register.

Transactions are 16 bit.
15th bit = CMD, Read = 0, write = 1
14-9 = Address for read/write (MOSI) Nothing for MISO (all zeros)
8-1 = 8 data bits for writing / all zeros on MOSI when reading / 8 read bits from MISO when reading
0 = Parity bit - set so that # of 1's is even across all 16 bits

For reads and writes we send the address to read/write. The reply from the chip has these as status flags that are always zero.

0x8756 = 1 000011 10101011 0 (Write, PROTCFG, 0xAB - First unlock byte)
0x87DE = 1 000011 11101111 0 (Write, PROTCFG, 0xEF - Second unlock byte)
0x86AD = 1 000011 01010110 1 (Write, PROTCFG, 0x56 - Third unlock byte, parity)
0x8625 = 1 000011 00010010 1 (Write, PROTCFG, 0x12 - Last unlock byte, parity)

Sent 0x0C00 = 0b0 000110 00000000 0 = (Read, WDCFG0)
Received 0x80C8 = 1 000000 01100100 0 (Replying, 0x64 - watchdog error threshold = 6, window watchdog disabled, functional watchdog enabled, external WDI input as WWD trigger, watchdog cycle time = 0.1ms)

Send 0x0E01 = 0 000111 00000000 1 = (Read, WDCFG1)
Received 0x81ED = 1 000000 11110110 1 = (Reply, 0xF6 - Top three not used, watchdog enabled while sleep, functional watchdog error of 6 causes reset)

0x87BE = 1 000011 11011111 0 (Write, PROTCFG, 0xDF - First lock byte)
0x8668 = 1 000011 00110100 0 (Write, PROTCFG, 0x34 - Second lock byte)
0x877D = 1 000011 10111110 1 (Write, PROTCFG, 0xBE - Third lock byte, parity)
0x8795 = 1 000011 11001010 1 (Write, PROTCFG, 0xCA - Fourth lock byte, parity)

So, this first set of transactions unlocks the protected registers, reads
two of them (watchdog config), then locks the registers again.

I wish I could have gotten farther but that should at least get people started. That should explain how to look at the data bytes in Saleae Logic and figure out what they mean. Since I decoded the unlock/lock sequences you can just ignore those while decoding / skip over them as they'll be that same thing all the time. The juicy goodness is the operations in between.

This was the beginning of the cold start log BTW. That's where decoding should start - from the beginning.

I did a little more. Here's the continuation. Well, all my notes so far. YMMV about all this. This goes all the way to the end of the cold start file but a lot of it is yet not decoded.

<unlock>
0x8E3C = 1 000111 00011110 0 (Write, WDCFG1, 0x1E - Request WD function in sleep, WD error threshold 15)
0x8DDE = 1 000110 11101111 0 (Write, WDCFG0, 0xEF - Window WD threshold 15, Window WD enable, Functional WD enable, WWD trigged by SPI write to WWDSCMD, 1ms tick period)
0x8A01 = 1 000101 00000000 1 (Write, SYSPCFG1, 0x00 - No delay in state transition, err pin monitoring off in sleep, err pin monitoring disabled fully, err pin monitor recovery disabled, err pin monitor recovery time 1ms)
0x9009 = 1 001000 00000100 1 (Write, FWDCFG, 0x04 - functional watchdog heartbeat timer period 250 cycles)
0x9201 = 1 001001 00000000 1 (Write, WWDCFG0, 0x00 - window watchdog closed window time 50 cycles)
0x9402 = 1 001010 00000001 0 (Write, WWDCFG1, 0x01 - window watchdog open window time 100 WD cycles)
<lock>

Send 0x2E00 = 0 010111 00000000 0 (Read WWDSCMD)
Receive 0x8001 = 1 000000 00000000 1 (Reply 0x00 - Trigger status = 0)

0xAE02 = 1 010111 00000001 0 (Write WWDSCMD, 0x01 - Write 1 to TRIG - Supposed to write inverse of Trigger status we just read)

Send 0x5401 = 0 101010 00000000 1 (Read FWDSTATO)
Receive 0x8061 = 1 000000 00110000 1 (reply 0x30 - FWD response message is wrong, response counter = 3, question = 0 - All are defaults upon reset)

0xB1FF = 1 000000 11111111 1 (Write DEVCFG0, 0xFF - Wake timer enabled in sleep/standby 10ms, 1600us transition delay to sleep)

0xB01F = 1 011000 00001111 1 (Write FWDRSP, 0x0F - Write functional watchdog response here)

0xB1E1 = 1 011000 11110000 1 (Write FWDRSP, 0xF0 - Write second response. No idea what this means)

0xB200 = 1 011001 00000000 0 (Write FWDRSPSYNC, 0x00 - Write last FWD heartbeat sync response here to restart heartbeat)

0xABD5 = 1 010101 11101010 1 (Write DEVCTRL, 0xEA - Tracker QT2 enabled, tracker QT1 enabled, QC0 enabled, QVR enabled, Go to NORMAL mode)

0xAC2B = 1 010110 00010101 1 (Write DEVCTRLN, 0x15 - Inverted bit pattern from above)

Send 0x2E00
Receive 0x8103

0xAE01

0x5401

Send 0x3801
Receive 0x8010

Send 0x4001
Receive 0x8001

Send 0x4200
Receive 0x8001

Send 0x4400
Receive 0x8002

Send 0x4601
Receive 0x8001

0xC000
0xC201
0xC402
0xC600
0xB811

Send 0x3801
Receive 0x8002

Send 0x3A00
Receive 0x8004

0xBA04
0xB803

Send 0x3801
Receive 0x8001

Send 0x2E00
Receive 0x8001

0xAE02
0xB002
0xB1E2
0xB01C
0xB3FD

Send 0x2E00
Receive 0x8103

0xAE01

Send 0x5401
Receive 0x80E5

Send 0x2E00
Receive 0x8001

0xAE02

0xB1D2
0xB032
0xB1CC
0xB22D

Send 0x2E00
Receive 0x8103

0xAE01

Send 0x5401
Receive 0x80EA