

Cato Yuan Wen

 +1 650 451 8009  cyw6944@nyu.edu  <https://catoywen.github.io/portfolio/> (not finished)

Education

New York University	2021.09 – Today
<ul style="list-style-type: none">• Major: Electrical and Computer Engineering• Minor: Financial Engineering• GPA: 3.919	
Shanghai High School International Division	2017.09 – 2021.05
<ul style="list-style-type: none">• International Baccalaureate Program 43/45• Computer Science High Level 7/7• Math Application & Approaches High Level 7/7• Computer Science Extended Essay 3/3	

Relevant Coursework

Very Large Scale Integration (NYU)	A
<ul style="list-style-type: none">• Used Cadence Virtuoso EDA Suite to design and simulate circuit designs• Learned about basic semiconductor physics, CMOS fabrication, combinational logic circuit design, transistor sizing, and more	
Circuits (NYU)	A
<ul style="list-style-type: none">• Used oscilloscopes, digital multimeters, waveform generators, Arduino in experiments• Learned the calculation and design of BJT, MOSFET, small signal, and operational amplifier circuits	
Advanced Linear Algebra and Complex Variables (NYU)	A-
<ul style="list-style-type: none">• Learned about complex integration, Cauchy Riemann Equations, Cauchy Goursat, Gram Schmidt process, QR decomposition, matrix diagonalization, LU decomposition, and SVD decomposition• Can complete linear regression using vector projects and compress images using SVD decomposition	
Very Large Scale Integration (Coursera)	honor
<ul style="list-style-type: none">• learned about various digital logic techniques such as Shannon expansion, network repair, checking satisfiability, multilevel logic synthesis, and ASIC placement	

Work Experience

Synopsys - Technical Intern	2022.06 – 2022.08
<ul style="list-style-type: none">• Wrote simple scripts to process and format data. Also used simple statistical models to analyze the placement of clock sinks in clock tree synthesis	
Analogic - Intern	2022.01 – 2022.02
<ul style="list-style-type: none">• Translated over 300 pages of FPGA documentation from Chinese to English, helped prepare powerpoint presentations, and took notes during meetings	

Past Projects/Papers

International Baccalaureate Extended Essay
<ul style="list-style-type: none">• Analyzed various methods to reduce inference time for FPGA based CNN accelerators. Methods include early exits, pruning, and the tiling algorithm
International Artificial Intelligence Fair
<ul style="list-style-type: none">• Developed neural network with two peers to predict bus delay for Toronto. Acquired and preprocessed data such as weather conditions, holidays, and traffic accidents

Technical Skills

<ul style="list-style-type: none">• Languages (comfortable): English, Chinese, Python, C++, Verilog• Languages (beginner): Java, React, Javascript, HTML, CSS• Libraries: Numpy, Pandas, CV2, Sklearn, Tensorflow, Dlib, Pickle, Selenium, Scrapy, Tkinter• Misc: Cadence Virtuoso
