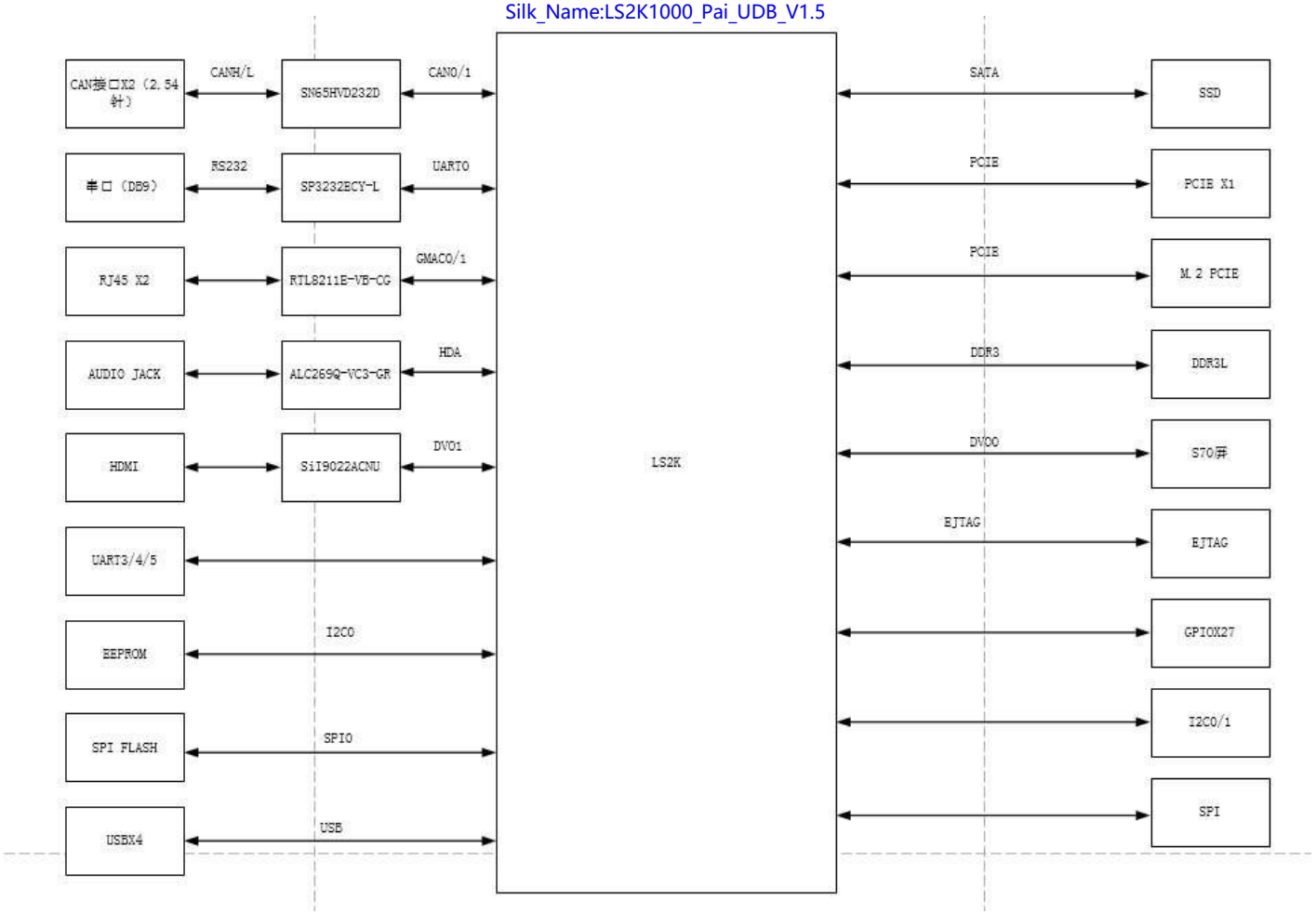
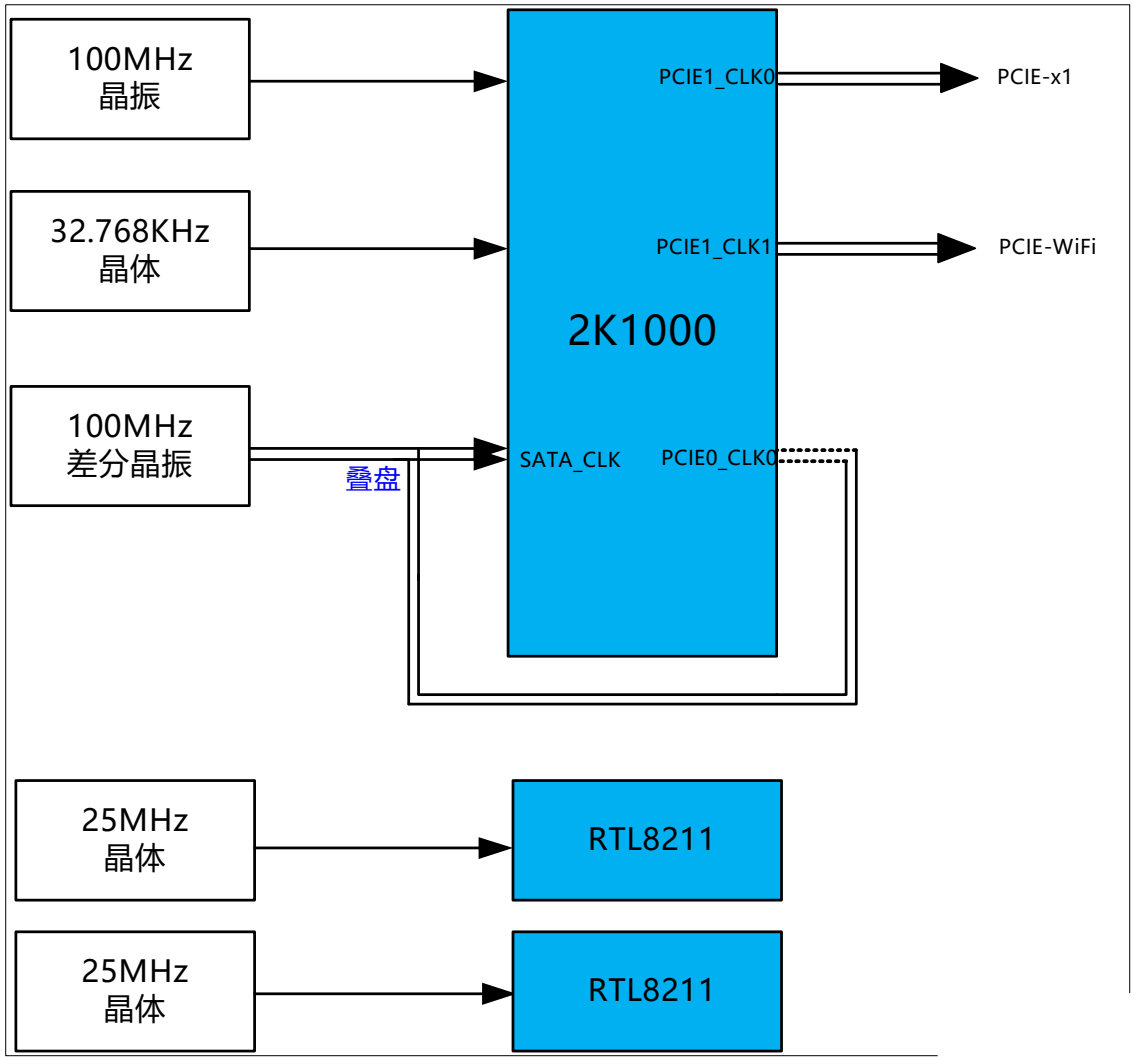
2K1000 Pai SYSTEM BLOCK

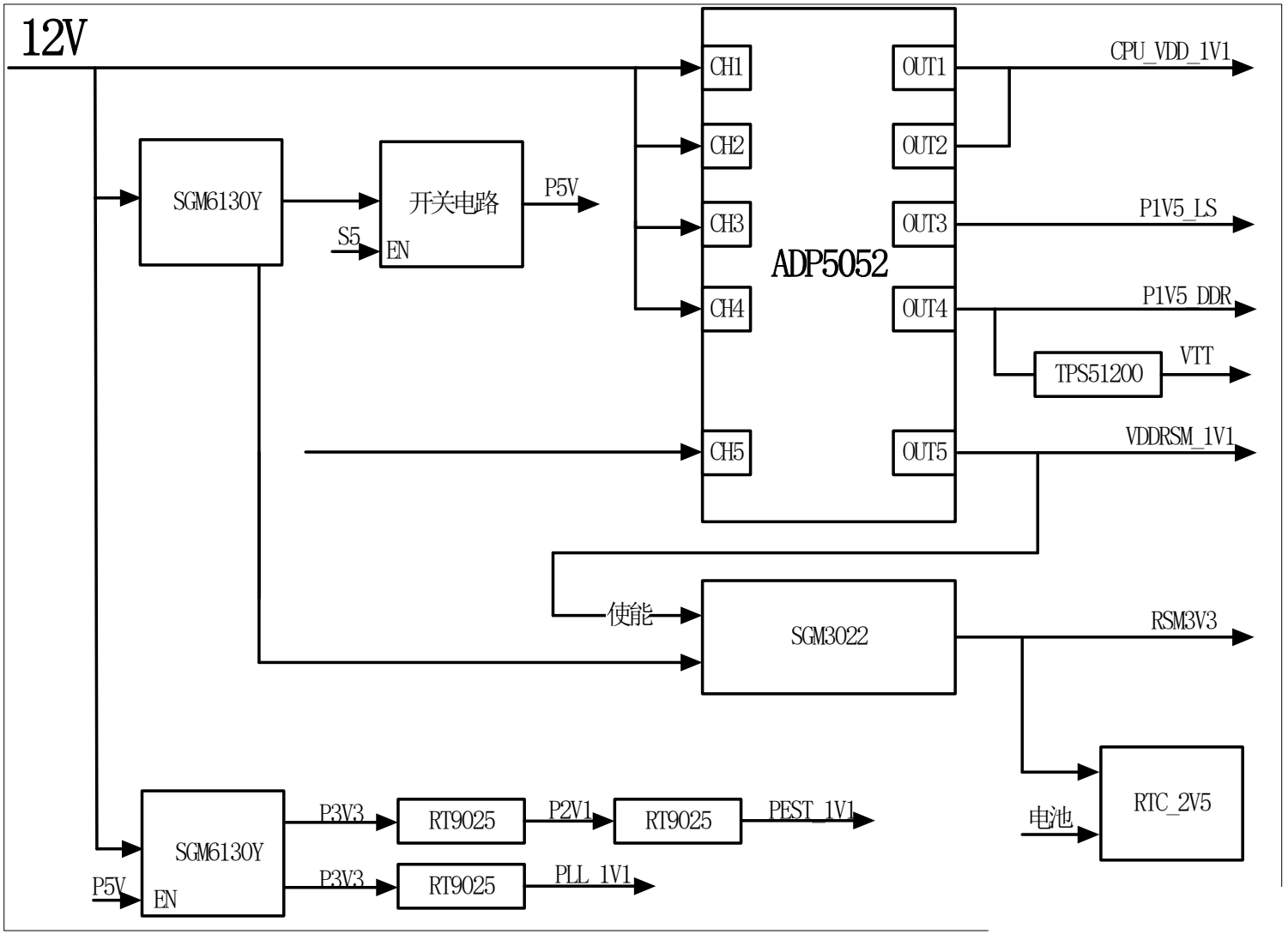
技术微信：14749330677
Silk_Name:LS2K1000_Pai_UDB_V1.5



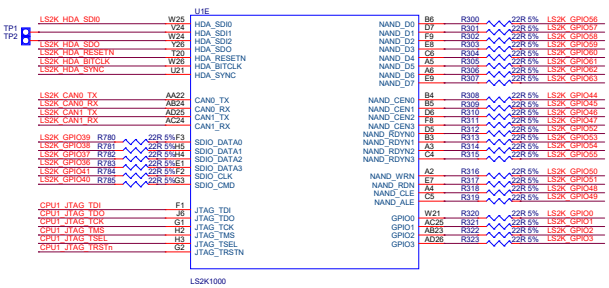
CLOCK BLOCK

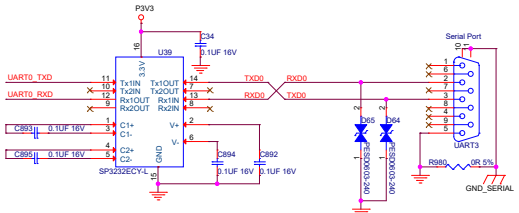

100MHz
晶振
32.768KHz
晶体
100MHz
差分晶振
叠盘
PCIE1_CLK0
PCIE1_CLK1
2K1000
SATA_CLK
PCIE0_CLK0
PCIE-x1
PCIE-WiFi
25MHz
晶体
25MHz
晶体
RTL8211
RTL8211

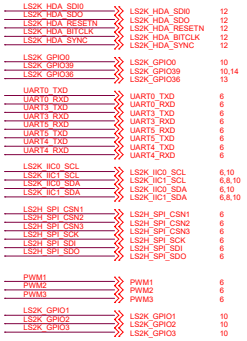
POWER BLOCK

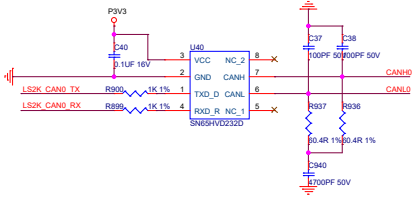

12V
CH1
CH2
CH3
CH4
CH5
OUT1
OUT2
OUT3
OUT4
OUT5
ADP5052
CPU_VDD_1V1
P1V5_LS
P1V5_DDR
VTT
TPS51200
VDDRSM_1V1
SGM6130Y
开关电路
P5V
S5
EN
使能
SGM3022
RSM3V3
RTC_2V5
电池
SGM6130Y
P5V
EN
P3V3
RT9025
P2V1
RT9025
PEST_1V1
P3V3
RT9025
PLL_1V1

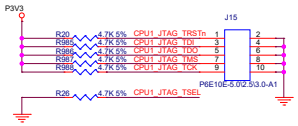
龙 芯 派-2K1000-Q

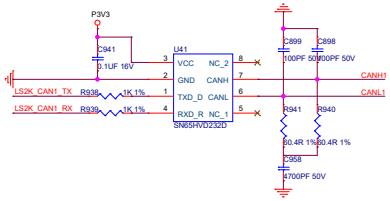

U1E
LS2K1000
LS2K_HDA_SDI0
LS2K_HDA_SDO
LS2K_HDA_RESETN
LS2K_HDA_BITCLK
LS2K_HDA_SYNC
LS2K_CAN0_TX
LS2K_CAN0_RX
LS2K_CAN1_TX
LS2K_CAN1_RX
LS2K_GPIO39
LS2K_GPIO38
LS2K_GPIO37
LS2K_GPIO36
LS2K_GPIO41
LS2K_GPIO40
CPU1_JTAG_TDI
CPU1_JTAG_TDO
CPU1_JTAG_TCK
CPU1_JTAG_TMS
CPU1_JTAG_TSEL
CPU1_JTAG_TRSTn
NAND_D0
NAND_D1
NAND_D2
NAND_D3
NAND_D4
NAND_D5
NAND_D6
NAND_D7
NAND_CEN0
NAND_CEN1
NAND_CEN2
NAND_CEN3
NAND_RDYN0
NAND_RDYN1
NAND_RDYN2
NAND_RDYN3
NAND_WRN
NAND_RDN
NAND_CLE
NAND_ALE
GPIO0
GPIO1
GPIO2
GPIO3
LS2K_GPIO56
LS2K_GPIO57
LS2K_GPIO58
LS2K_GPIO59
LS2K_GPIO60
LS2K_GPIO61
LS2K_GPIO62
LS2K_GPIO63
LS2K_GPIO44
LS2K_GPIO45
LS2K_GPIO46
LS2K_GPIO47
LS2K_GPIO52
LS2K_GPIO53
LS2K_GPIO54
LS2K_GPIO55
LS2K_GPIO50
LS2K_GPIO51
LS2K_GPIO48
LS2K_GPIO49
LS2K_GPIO0
LS2K_GPIO1
LS2K_GPIO2
LS2K_GPIO3

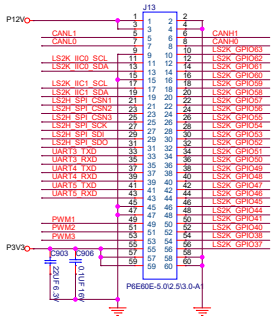

P3V3
U39
SP3232ECY-L
UART0_TXD
UART0_RXD
TXD0
RXD0
Serial Port
UART3
GND_SERIAL
D65
D64
R986
0R 5%

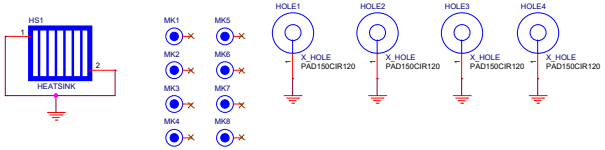

LS2K_HDA_SDI0
LS2K_HDA_SDO
LS2K_HDA_RESETN
LS2K_HDA_BITCLK
LS2K_HDA_SYNC
LS2K_GPIO0
LS2K_GPIO39
LS2K_GPIO36
UART0_TXD
UART0_RXD
UART3_TXD
UART3_RXD
UART5_TXD
UART5_RXD
UART4_TXD
UART4_RXD
LS2K_IIC0_SCL
LS2K_IIC1_SCL
LS2K_IIC0_SDA
LS2K_IIC1_SDA
LS2H_SPI_CSN1
LS2H_SPI_CSN2
LS2H_SPI_CSN3
LS2H_SPI_SCK
LS2H_SPI_SDI
LS2H_SPI_SDO
PWM1
PWM2
PWM3
LS2K_GPIO1
LS2K_GPIO2
LS2K_GPIO3

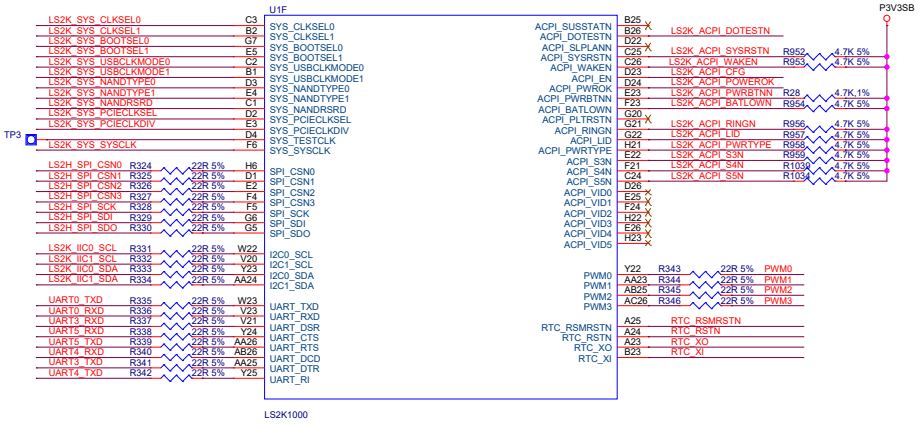

P3V3
U40
SN65HVD232D
LS2K_CAN0_TX
LS2K_CAN0_RX
CANH0
CANL0
R900
R899
R937
R936
C940
4700PF 50V

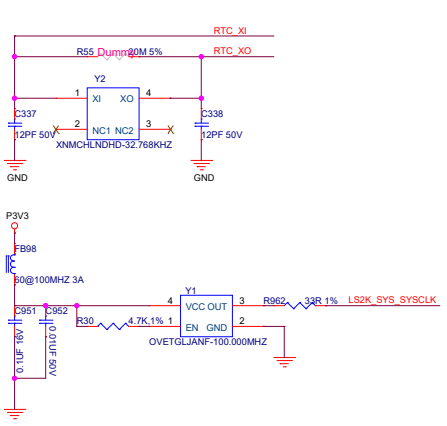

P3V3
J15
P6E10E-5.0\2.5\3.0-A1
CPU1_JTAG_TRSTn
CPU1_JTAG_TDI
CPU1_JTAG_TDO
CPU1_JTAG_TMS
CPU1_JTAG_TCK
CPU1_JTAG_TSEL

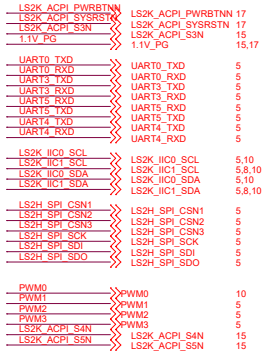

P3V3
U41
SN65HVD232D
LS2K_CAN1_TX
LS2K_CAN1_RX
CANH1
CANL1
R938
R939
R941
R940
C958
4700PF 50V


P12V
J13
P6E60E-5.0\2.5\3.0-A
CANL1
CANH1
CANL0
CANH0
LS2K_IIC0_SCL
LS2K_IIC0_SDA
LS2K_IIC1_SCL
LS2K_IIC1_SDA
LS2H_SPI_CSN1
LS2H_SPI_CSN2
LS2H_SPI_CSN3
LS2H_SPI_SCK
LS2H_SPI_SDI
LS2H_SPI_SDO
UART3_TXD
UART3_RXD
UART4_TXD
UART4_RXD
UART5_TXD
UART5_RXD
PWM1
PWM2
PWM3
P3V3

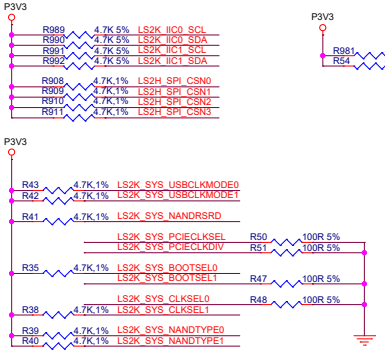

HS1
HEATSINK
MK1
MK2
MK3
MK4
MK5
MK6
MK7
MK8
HOLE1
HOLE2
HOLE3
HOLE4
X_HOLE
PAD150CIR120

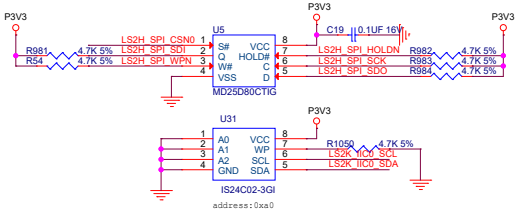


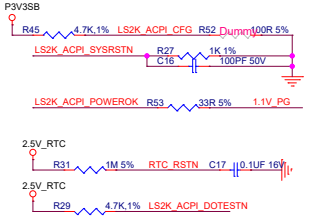


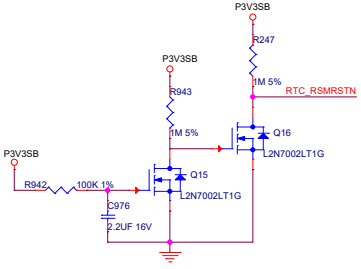


SYS_CLKSEL[1:0]	I	PLL 时钟配置输入 00=低频模式 01=高频模式 10=软件模式(DFT) 11=bypass 模式
SYS_BOOTSEL[1:0]	I	启动选择输入 00=LIO 01=SPI(DFT) 10=SDIO 11=NAND

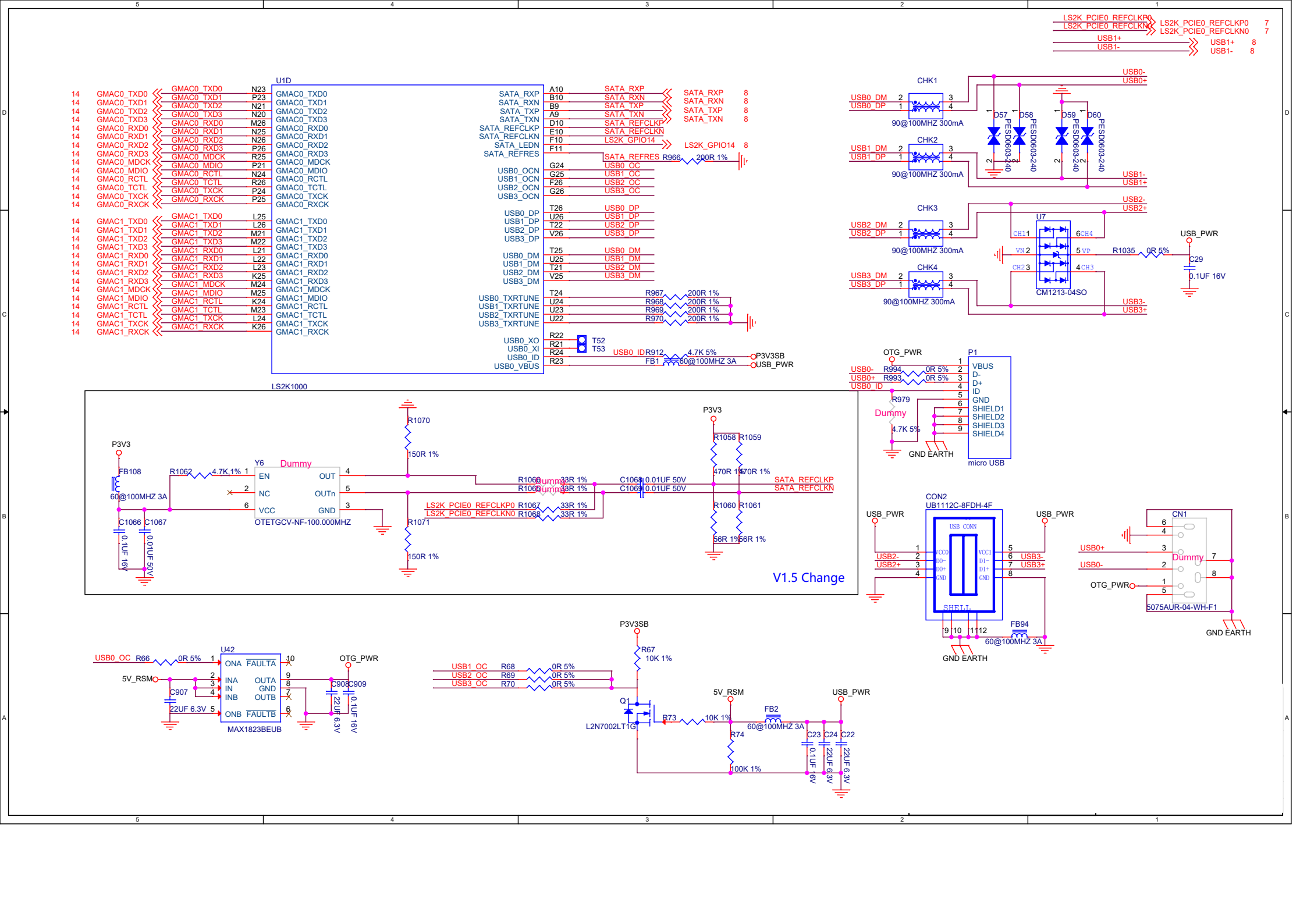


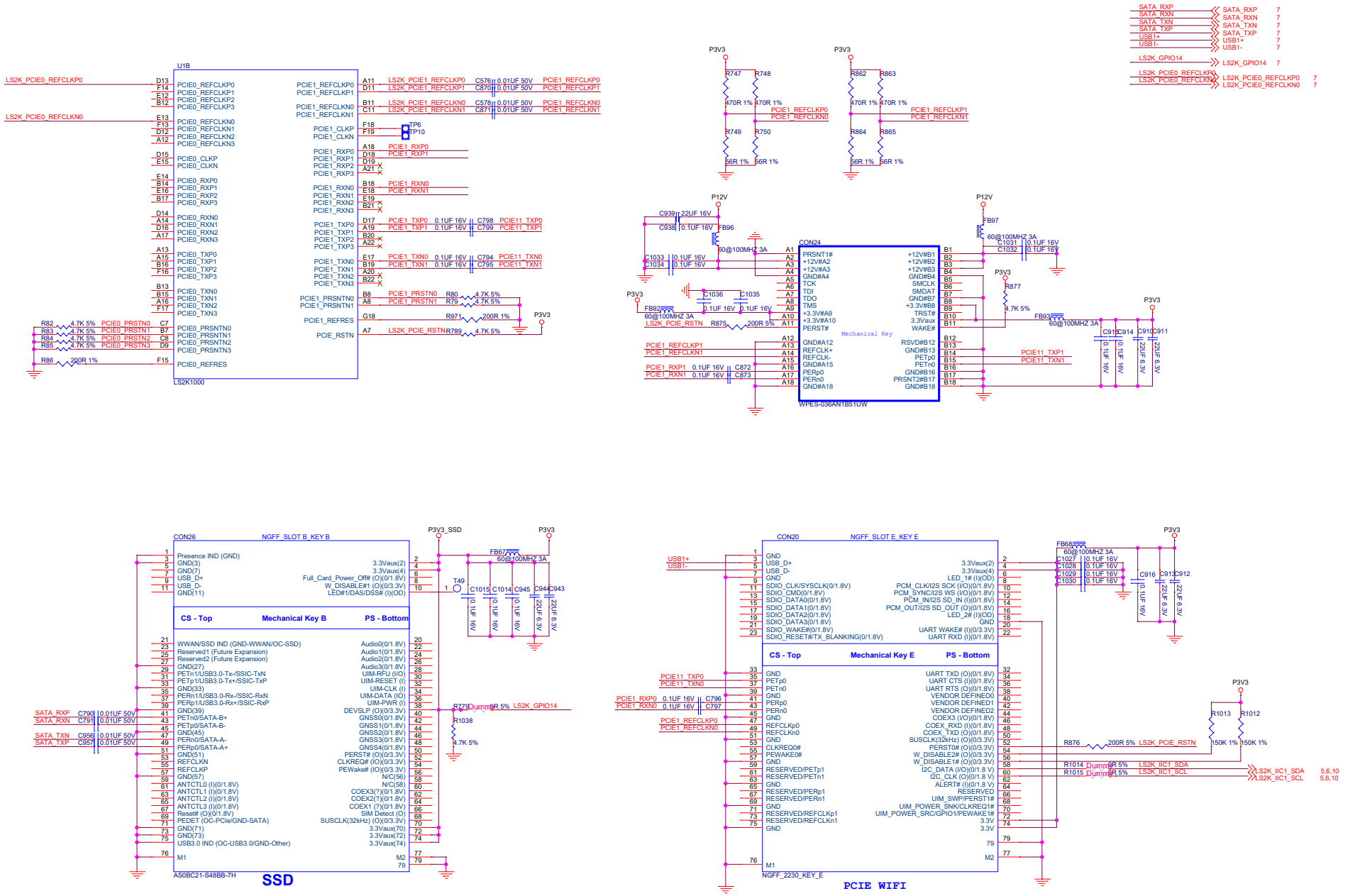


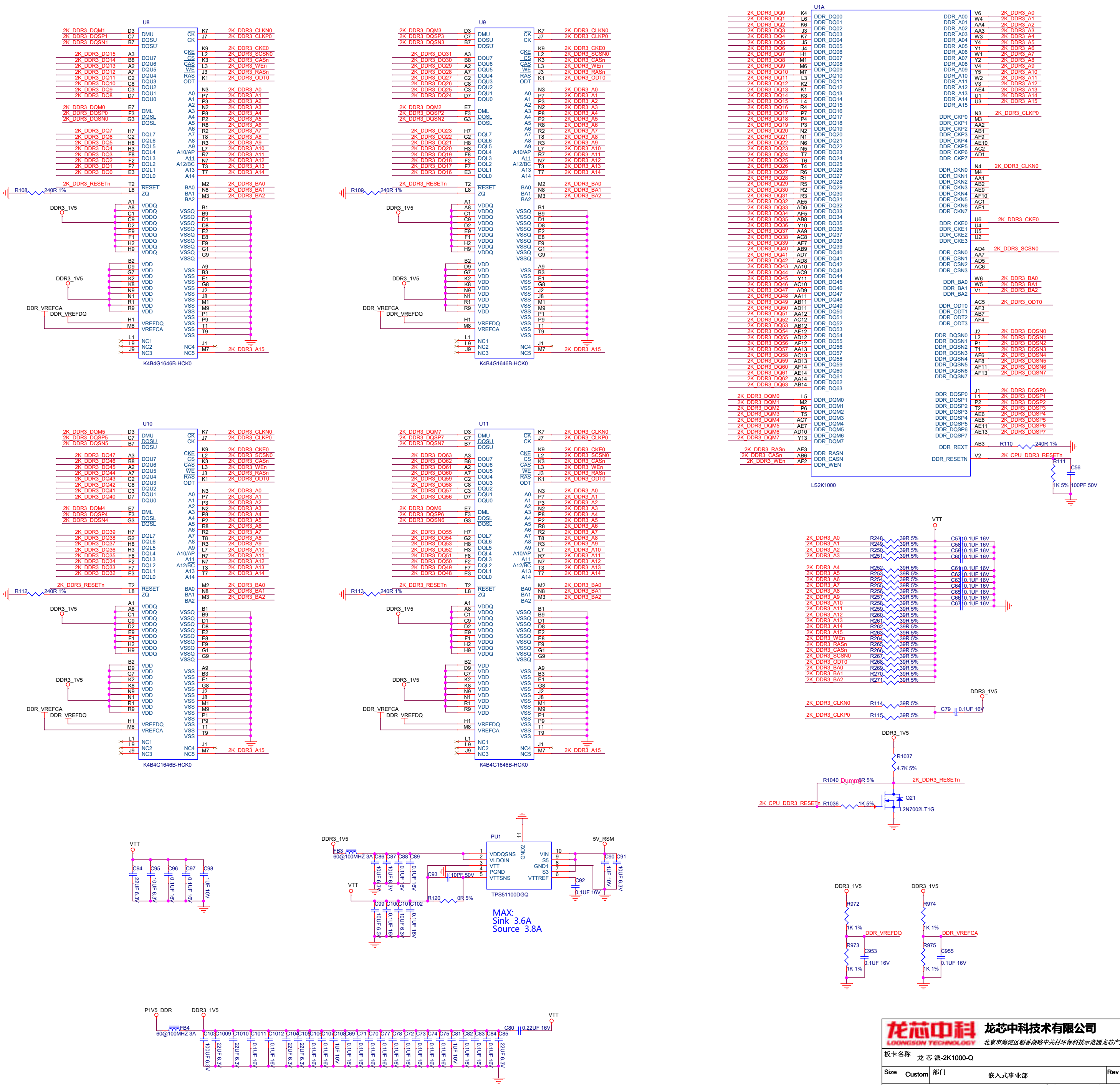




SYS_USBCLKMODE[1:0]	I	USB 时钟输入配置输入 00=保留 01=保留 10=one 12MHz clock input 11=use sysclk(DFT)
SYS_PCIECLKSEL	I	PCIE 参考时钟选择输入 {SYS_PCIECLKSEL, SYS_PCIECLKDIV}: 00=内部 100MHz 时钟 01=保留 10=外部 100MHz 时钟 11=外部 200MHz 时钟
SYS_PCIECLKDIV	I	PCIE 参考时钟选择输入 {SYS_PCIECLKSEL, SYS_PCIECLKDIV}: 00=内部 100MHz 时钟 01=保留 10=外部 100MHz 时钟 11=外部 200MHz 时钟
SYS_NANDRSRD	I	NAND ECC 功能使能输入, 1=enable 0=disable(DFT)


LS2K_PCIE0_REFCLKP0
LS2K_PCIE0_REFCLKN0
USB1+
USB1-
U1D
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_MDCK
GMAC0_MDIO
GMAC0_RCTL
GMAC0_TCTL
GMAC0_TXCK
GMAC0_RXCK
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_MDCK
GMAC1_MDIO
GMAC1_RCTL
GMAC1_TCTL
GMAC1_TXCK
GMAC1_RXCK
SATA_RXP
SATA_RXN
SATA_TXP
SATA_TXN
SATA_REFCLKP
SATA_REFCLKN
SATA_LEDN
SATA_REFRES
LS2K_GPIO14
R966 200R 1%
USB0_OCN
USB1_OCN
USB2_OCN
USB3_OCN
USB0_OC
USB1_OC
USB2_OC
USB3_OC
USB0_DP
USB1_DP
USB2_DP
USB3_DP
USB0_DM
USB1_DM
USB2_DM
USB3_DM
USB0_TXRTUNE
USB1_TXRTUNE
USB2_TXRTUNE
USB3_TXRTUNE
R967 200R 1%
R968 200R 1%
R969 200R 1%
R970 200R 1%
USB0_XO
USB0_XI
USB0_ID
USB0_VBUS
T52
T53
R912 4.7K 5%
FB1 60@100MHZ 3A
P3V3SB
USB_PWR
CHK1
CHK2
CHK3
CHK4
90@100MHZ 300mA
D57 PESD0603-240
D58 PESD0603-240
D59 PESD0603-240
D60 PESD0603-240
U7
CM1213-04SO
R1035 0R 5%
C29 0.1UF 16V
LS2K1000
P3V3
FB108 60@100MHZ 3A
R1062 4.7K,1%
Y6 Dummy
OTETGCV-NF-100.000MHZ
C1066 0.1UF 16V
C1067 0.01UF 50V
R1070 150R 1%
R1071 150R 1%
R1065 Dummy 33R 1%
R1066 Dummy 33R 1%
R1067 33R 1%
R1068 33R 1%
C1068 0.01UF 50V
C1069 0.01UF 50V
R1058 470R 1%
R1059 470R 1%
R1060 56R 1%
R1061 56R 1%
SATA_REFCLKP
SATA_REFCLKN
V1.5 Change
OTG_PWR
P1
micro USB
R994 0R 5%
R993 0R 5%
R979 Dummy 4.7K 5%
GND EARTH
CON2
UB1112C-8FDH-4F
FB94 60@100MHZ 3A
CN1
5075AUR-04-WH-F1
U42
MAX1823BEUB
R66 0R 5%
5V_RSM
C907 22UF 6.3V
C908 22UF 6.3V
C909 0.1UF 16V
R68 0R 5%
R69 0R 5%
R70 0R 5%
R67 10K 1%
Q1
L2N7002LT1G
R73 10K 1%
R74 100K 1%
FB2 60@100MHZ 3A
C23 0.1UF 6V
C24 22UF 6.3V
C22 22UF 6.3V

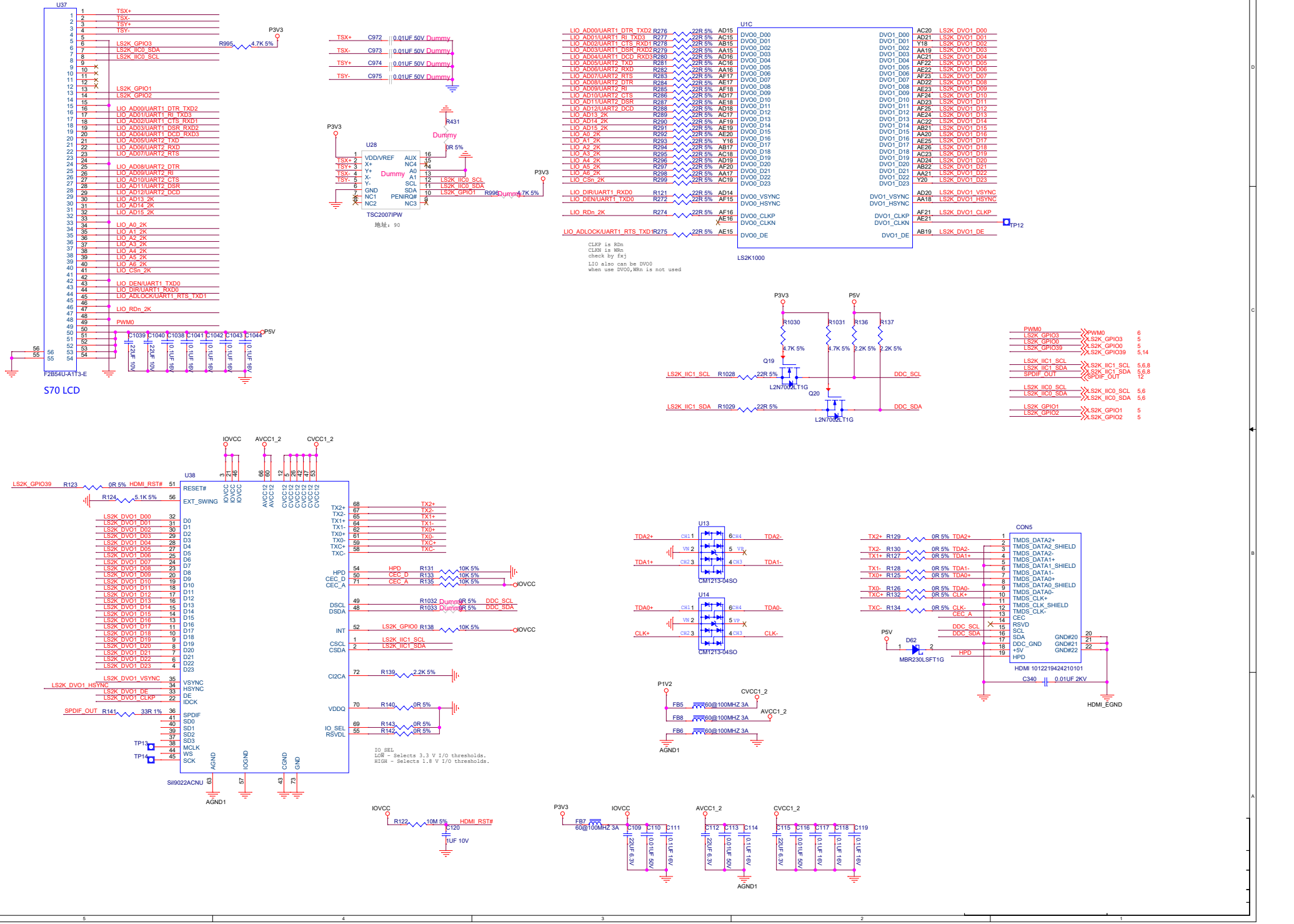

U1B
LS2K1000
CON26
NGFF_SLOT B_KEY B
CS - Top
Mechanical Key B
PS - Bottom
AS0BC21-S48BB-7H
SSD
CON24
WPES-036AN1B51UW
CON20
NGFF_SLOT E_KEY E
CS - Top
Mechanical Key E
PS - Bottom
NGFF_2230_KEY_E
PCIE WIFI

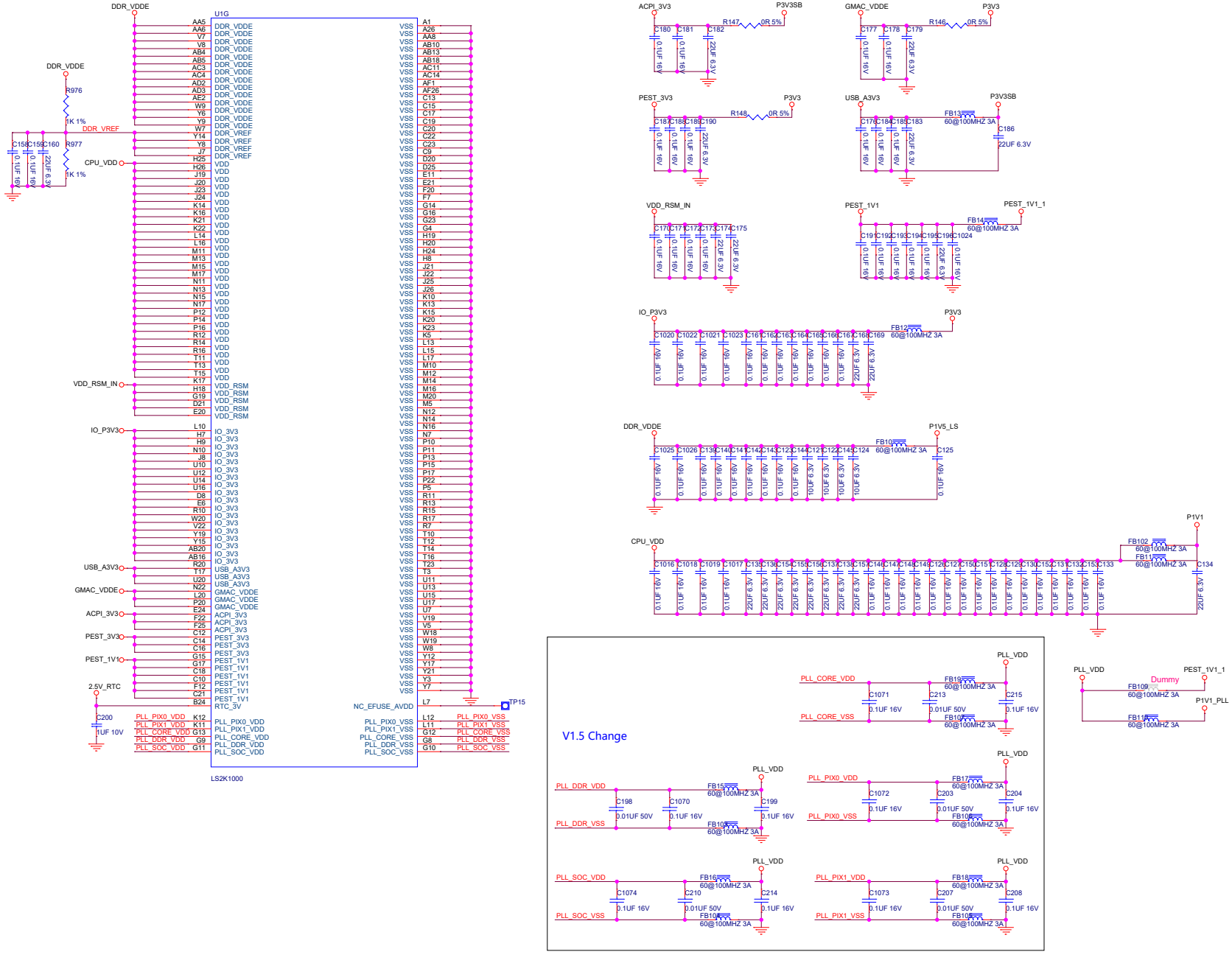


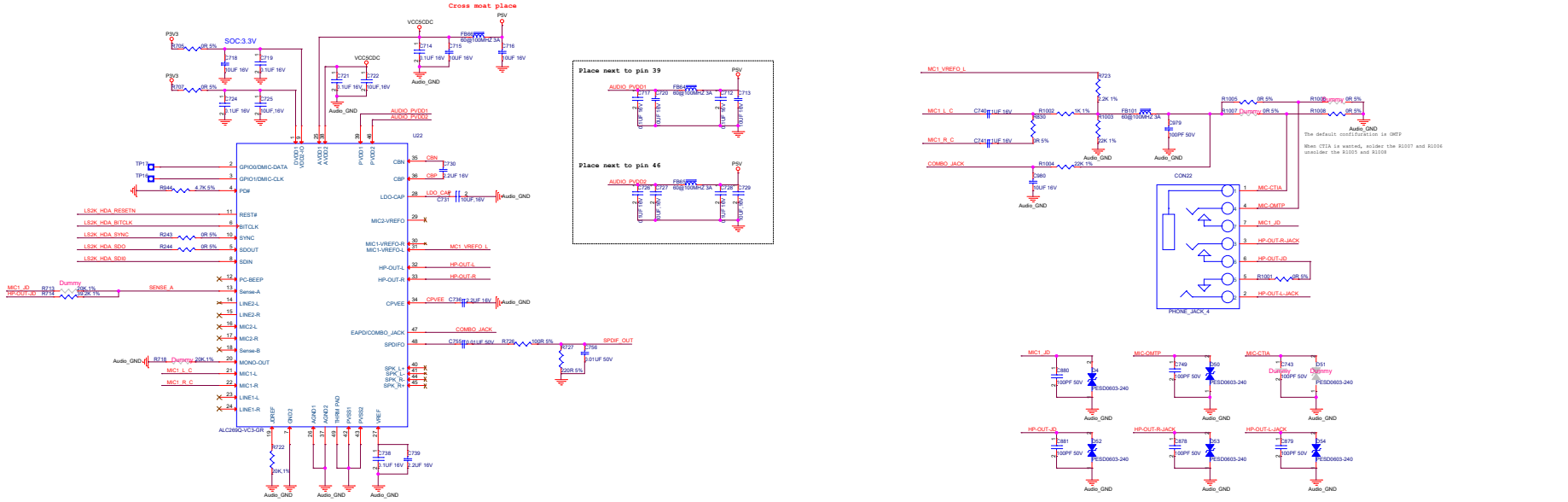
龙芯中科技术有限公司

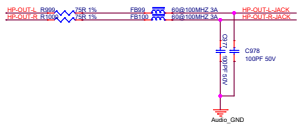
北京市海淀区稻香湖路中关村环保科技示范园龙芯产业园

板卡名称	龙 芯 派-2K1000-Q		
Size Custom	部门 嵌入式事业部		Rev V1.5
Date: Tuesday, April 13, 2021		Sheet 9 of 18	
Drawn By 郭峰		Checked By 田社校	

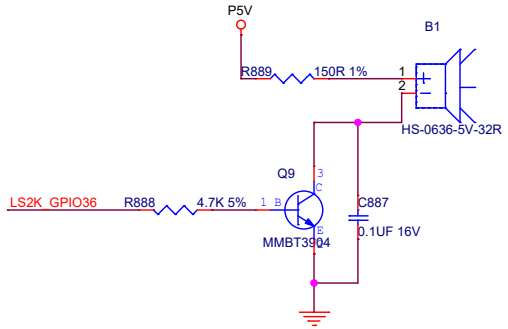

U37
F2B54U-A113-E
S70 LCD
U1C
LS2K1000
U28
TSC2007IPW
地址：90
U38
Sil9022ACNU
U13
U14
CM1213-04SO
CON5
HDMI 1012219424210101
MBR230LSFT1G
P3V3
P5V
P1V2
IOVCC
AVCC1_2
CVCC1_2
AGND1
HDMI_EGND
CLKP is RDn
CLKN is WRn
check by fxj
LIO also can be DVO0
when use DVO0,WRn is not used
IO_SEL
LOW - Selects 3.3 V I/O thresholds.
HIGH - Selects 1.8 V I/O thresholds.

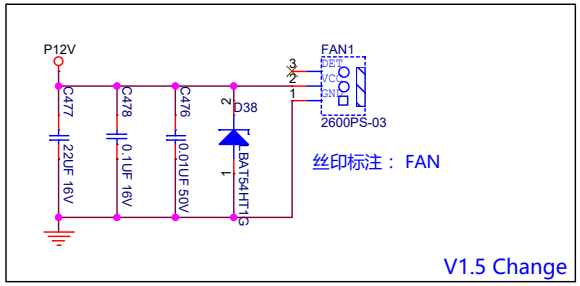

U1G
LS2K1000
DDR_VDDE
DDR_VREF
CPU_VDD
VDD_RSM_IN
IO_P3V3
USB_A3V3
GMAC_VDDE
ACPI_3V3
PEST_3V3
PEST_1V1
2.5V_RTC
NC_EFUSE_AVDD
TP15
R976
R977
1K 1%
C200
1UF 10V
PLL_PIX0_VDD
PLL_PIX1_VDD
PLL_CORE_VDD
PLL_DDR_VDD
PLL_SOC_VDD
PLL_PIX0_VSS
PLL_PIX1_VSS
PLL_CORE_VSS
PLL_DDR_VSS
PLL_SOC_VSS
ACPI_3V3
P3V3SB
GMAC_VDDE
P3V3
PEST_3V3
USB_A3V3
VDD_RSM_IN
PEST_1V1
PEST_1V1_1
IO_P3V3
DDR_VDDE
P1V5_LS
CPU_VDD
P1V1
R147
R146
R148
0R 5%
FB13
FB14
FB12
FB10
FB102
FB101
60@100MHZ 3A
C186
22UF 6.3V
C1024
C125
C134
V1.5 Change
PLL_VDD
PLL_CORE_VDD
PLL_CORE_VSS
PLL_DDR_VDD
PLL_DDR_VSS
PLL_PIX0_VDD
PLL_PIX0_VSS
PLL_SOC_VDD
PLL_SOC_VSS
PLL_PIX1_VDD
PLL_PIX1_VSS
FB15
FB16
FB17
FB18
FB19
FB109
FB110
FB111
Dummy
P1V1_PLL
0.01UF 50V
0.1UF 16V
0.1UF 6.3V
22UF 6.3V
10UF 6.3V





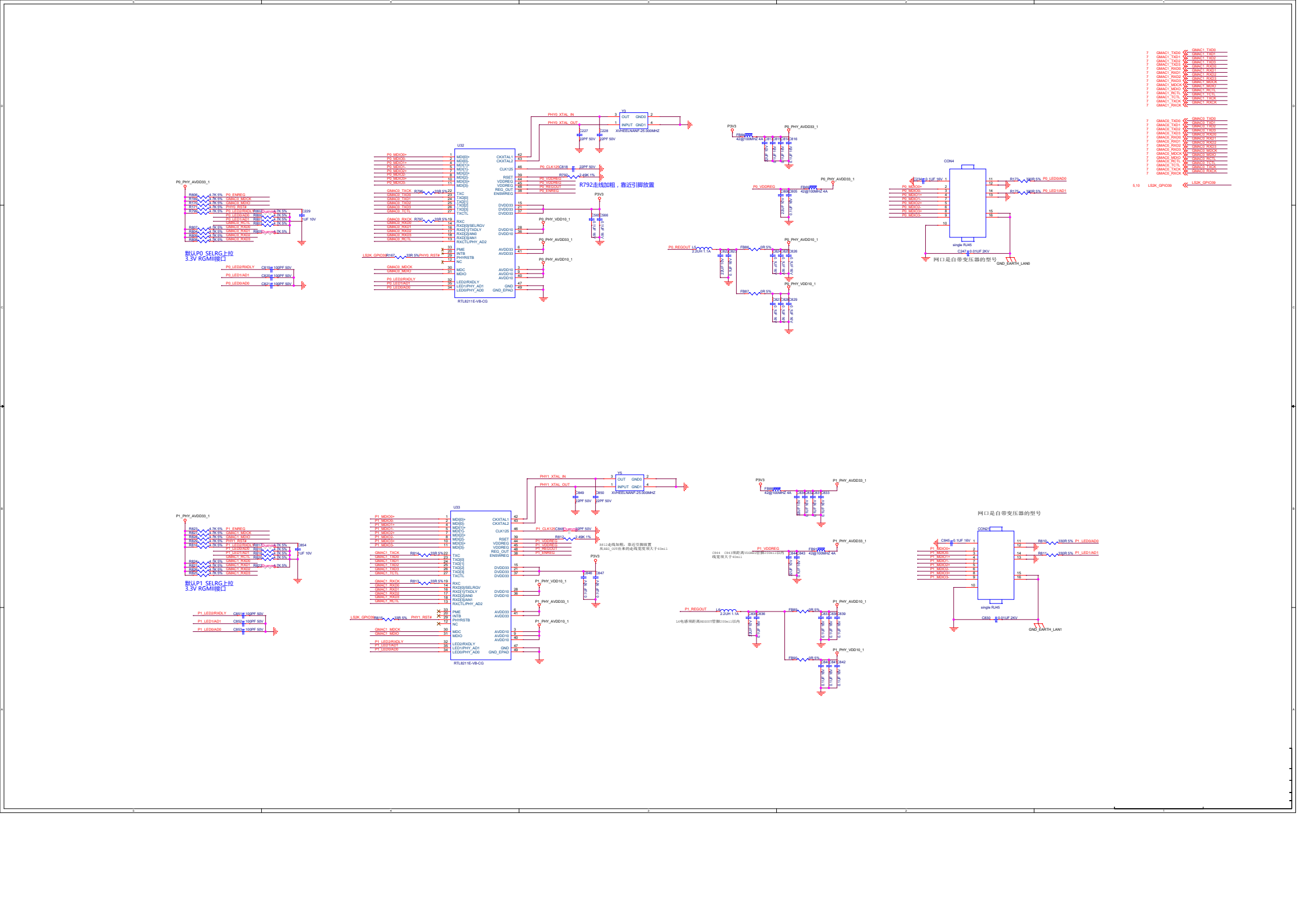
Change the ALC269's outout to HPOUT
Change the MIC's circuit
Dummy the MIC_JD's resistor
Change the HPOUT_JD's resistor to 39.2K

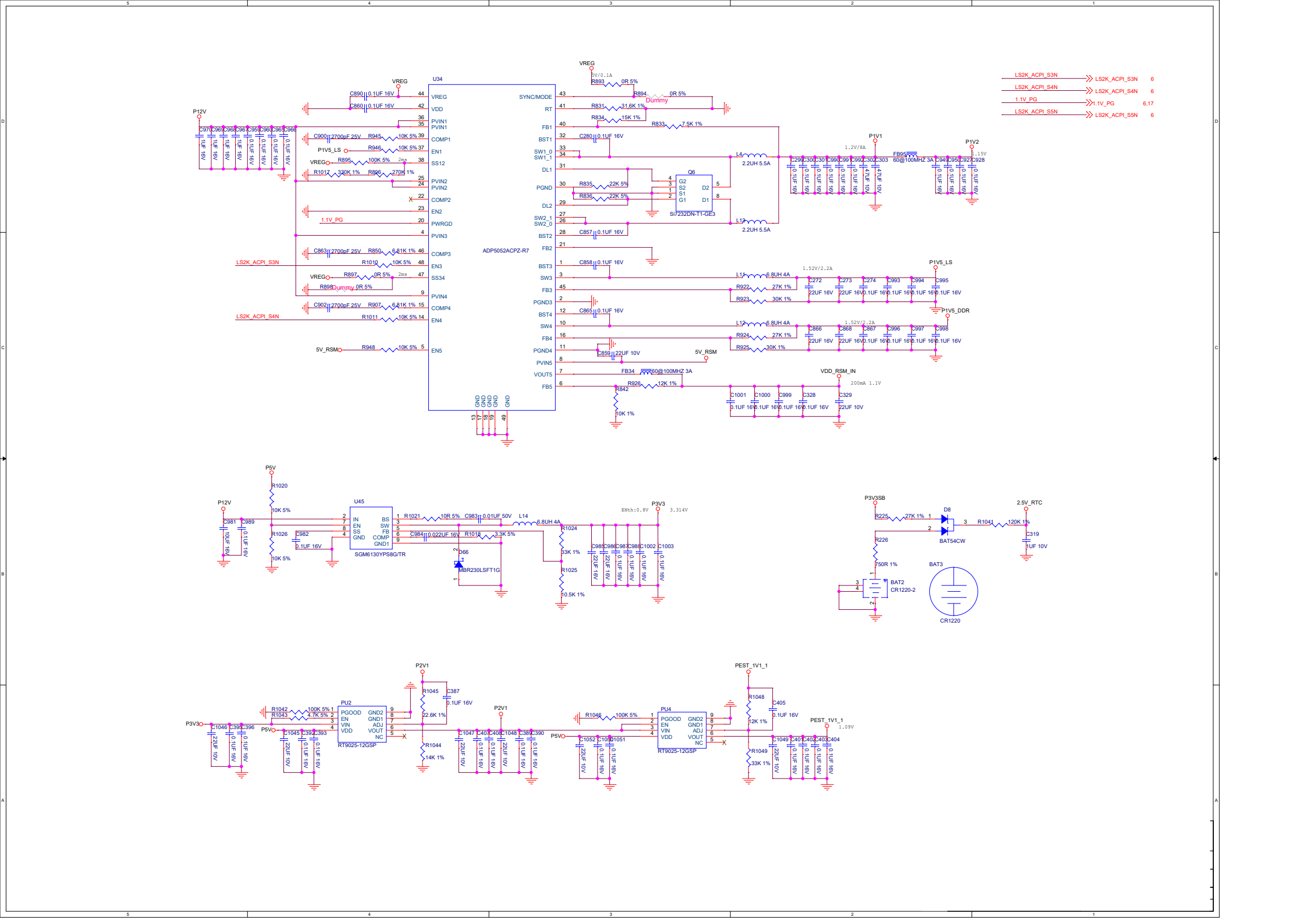


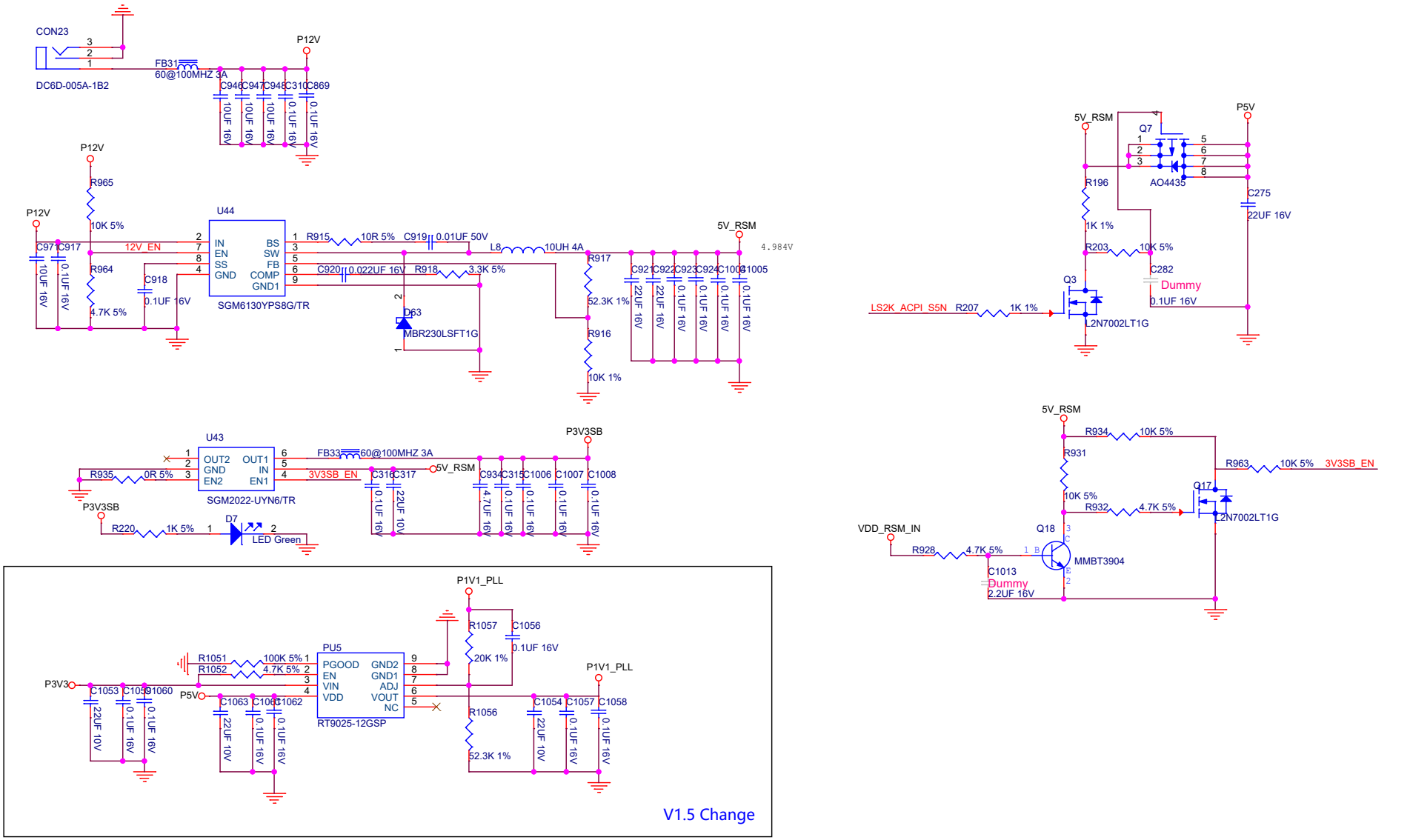


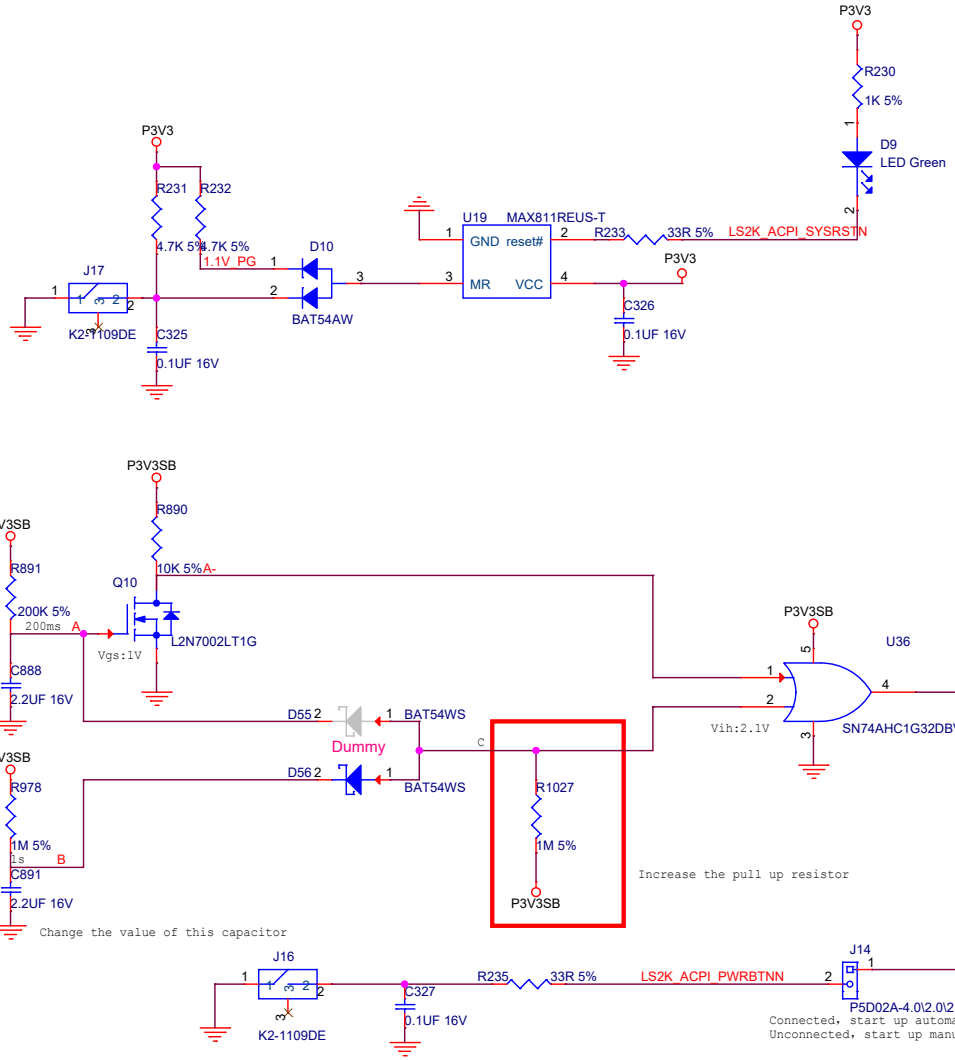
LS2K_GPIO36

LS2K_GPIO36 5


默认P0_SELRG上拉
3.3V RGMII接口
U32
RTL8211E-VB-CG
R792走线加粗，靠近引脚放置
网口是自带变压器的型号
默认P1_SELRG上拉
3.3V RGMII接口
U33
RTL8211E-VB-CG
网口是自带变压器的型号

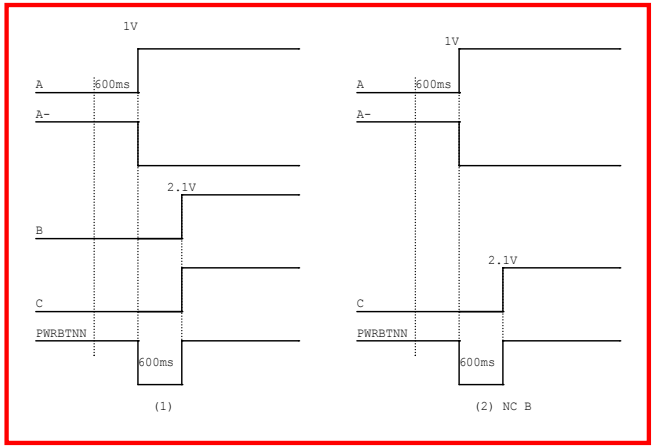

U34
ADP5052ACPZ-R7
VREG
P12V
LS2K_ACPI_S3N
LS2K_ACPI_S4N
5V_RSM
1.1V_PG
P1V5_LS
P1V5_DDR
P1V1
P1V2
VDD_RSM_IN
Q6
Si7232DN-T1-GE3
U45
SGM6130YPS8G/TR
D66
MBR230LSFT1G
P3V3
P5V
D8
BAT54CW
BAT2
CR1220-2
BAT3
CR1220
2.5V_RTC
PU2
RT9025-12GSP
PU4
P2V1
PEST_1V1_1


LS2K_ACPI_S5N
LS2K_ACPI_S5N 15
CON23
DC6D-005A-1B2
FB31
60@100MHZ 3A
P12V
C946 10UF 16V
C947 10UF 16V
C948 10UF 16V
C310 0.1UF 16V
C869 0.1UF 16V
R965 10K 5%
U44
SGM6130YPS8G/TR
IN
EN
SS
GND
BS
SW
FB
COMP
GND1
12V_EN
C97 10UF 16V
C917 0.1UF 16V
R964 4.7K 5%
C918 0.1UF 16V
R915 10R 5%
C919 0.01UF 50V
L8 10UH 4A
C920 0.022UF 16V
R918 3.3K 5%
D63
MBR230LSFT1G
R917 52.3K 1%
R916 10K 1%
5V_RSM
4.984V
C921 22UF 16V
C922 22UF 16V
C923 0.1UF 16V
C924 0.1UF 16V
C1004 0.1UF 16V
C1005 0.1UF 16V
U43
SGM2022-UYN6/TR
OUT2
GND
EN2
OUT1
IN
EN1
R935 0R 5%
FB33 60@100MHZ 3A
3V3SB_EN
C316 0.1UF 16V
C317 22UF 10V
P3V3SB
C934 4.7UF 16V
C315 0.1UF 16V
C1006 0.1UF 16V
C1007 0.1UF 16V
C1008 0.1UF 16V
R220 1K 5%
D7
LED Green
P1V1_PLL
PU5
RT9025-12GSP
PGOOD
EN
VIN
VDD
GND2
GND1
ADJ
VOUT
NC
R1051 100K 5%
R1052 4.7K 5%
P3V3
P5V
C1053 22UF 10V
C1059 0.1UF 16V
C1060 0.1UF 16V
C1063 22UF 10V
C1061 0.1UF 16V
C1062 0.1UF 16V
R1057 20K 1%
C1056 0.1UF 16V
R1056 52.3K 1%
C1054 22UF 10V
C1057 0.1UF 16V
C1058 0.1UF 16V
V1.5 Change
5V_RSM
Q7
AO4435
P5V
R196 1K 1%
R203 10K 5%
C275 22UF 16V
C282 Dummy 0.1UF 16V
Q3
L2N7002LT1G
LS2K_ACPI_S5N R207 1K 1%
R934 10K 5%
R931 10K 5%
R963 10K 5% 3V3SB_EN
Q17
L2N7002LT1G
R932 4.7K 5%
VDD_RSM_IN
R928 4.7K 5%
Q18
MMBT3904
C1013 Dummy 2.2UF 16V



LS2K_ACPI_SYSRSTN
1.1V_PG
LS2K_ACPI_PWRBTNN

LS2K_ACPI_SYSRSTN 6
1.1V_PG 6,15
LS2K_ACPI_PWRBTNN 6



Change history

1.del F1 20170812
2.LCD change 3.3V to 5V
3. Delete the SD card
4.Change the EJTAG pin to the standard one
5. Change the OTG USB connector to the micro one
6. Change the HDMI connector to the standard one
7. Change the AUDIO Codec IC, and change the audio jack from two to one and delet its delay circuit
8. Increase the Beeper circuit and the power on start up circuit
9. Change the PHY chip and the internet connector to the standard one
10.CHange the 2.0,1.0,1.25pin to 2.54pin
11.Delete the touch IC ZT2083, and change the touch mode to 1-wire mode;
12.Increase the M.2 SATA, M.2 PCIE, and PCIE X1
13.The power scheme is changed,.Using the PMU of ADP5052 and the RT9018B-25GQW
   to generate the used voltage,delete the former used power IC
14.Change the power entry port from micro USB to the 5V adapter port
15.Increase one RS232 connector
16.Delete the wifi module
17.The PCB size is changed into 120mm*120mm
18.Increase the EEPROM.
19.Increase the heatsink package and 8 mark points
20.Connect the USB1 to PCIE WIFI connector
21. Delete the resistors of 15K on the USB circuit
22.Changed the 40pin into a 54pin one

2018.10.23
1.Change the value of R942,and increase the capicator of C976
2.Change U5 from W25X40BVSNIG to MD25D80CTIG
3.Change the order of SATA_TXP and SATA_TXN to the right order

5.Change the ALC 269's output pin to audiojack,and modify the mic circuit
6.Change the resistors that are conneted to the EN pins of ADP 5052
7.R225 is changed from 100K to 100R
8.Change the channel 1 andchannel 2 to parallel mode of ADP5052
9.P3V3 is generated by other circuit, the chip is SGM6130
10.Increase the pull up resistors to the W_DISABLE signals of PCIE WIFI

11.Increase the pull up resistor to the auto startup resistor
12.Change the ADP5052's inductance's footprint to small ones.

2019.06.18

1、R31改为1M
2、增加R1028/R1029\R1031\R1030\Q19\Q20\C1013
3、RTCRSMRSTN上拉改为P3V3SB
4、USB处的供电源该为5VRSM
5、增加P3V3_SSD处的滤波电容
6、I2C1的信号接到HDMI接口处的I2C总线上，增加电平转换电路
7、去电U13、U14两个TVS管5脚上的电源
8、S5信号控制P5V的通断，S3信号控制DDR电源的使能。

2019.12.31　V1.4版本
1、新增PEST1V1_1的电源产生电路，该部分电路用于给2K的PEST1V1和PLL部分供电
2、修改给CPU_VDD供电的磁珠，同时该位置增加1个磁珠

2020.06.10　V1.5版本
1、新增PLL1V1_1的电源产生电路,该部分电路用于给2K的PLL部分供电(16页)
2、新增SATA 100M差分外部参考晶振（选焊,解决SATA概率性找不到问题）7页
3、修改多路电源的使能电阻，阻值10K，解决概率性不能上电问题（15页）
4、选焊掉C282防止上电5V有瞬间通电现象（16页）