MEC4126F: Integrated Embedded Systems

Prac 7
08 May 2025

Total marks: 51

Instructions to students

1. This template file contains space for the answers to the written questions of Prac 7.
2. Ensure that you copy-paste your answers inside the space allocated for each question.
3. Provide your numerical answers to **TWO (2)** significant decimal points, unless stated otherwise.

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Plagiarism Declaration

By demonstrating and submitting this practical I agree that:

- I know that plagiarism is a serious form of academic dishonesty.
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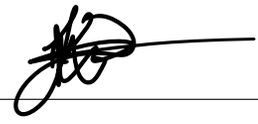
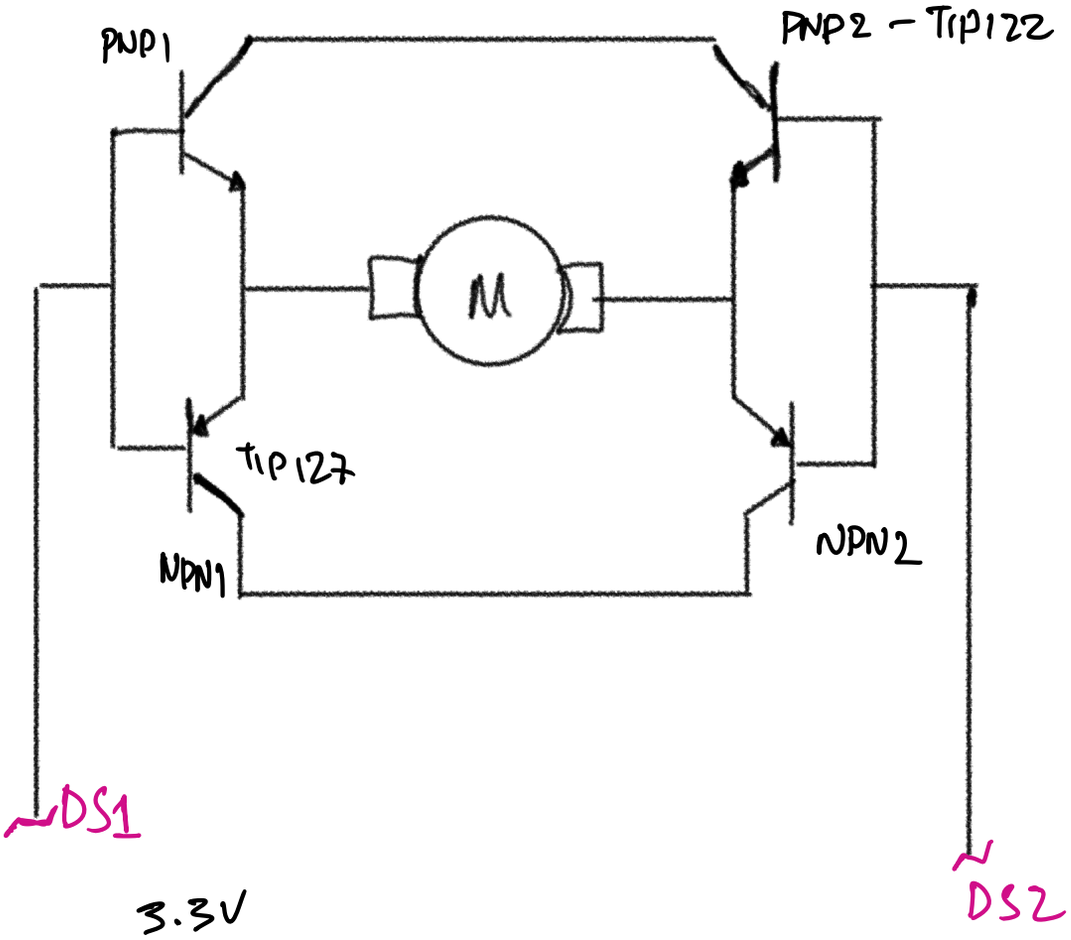
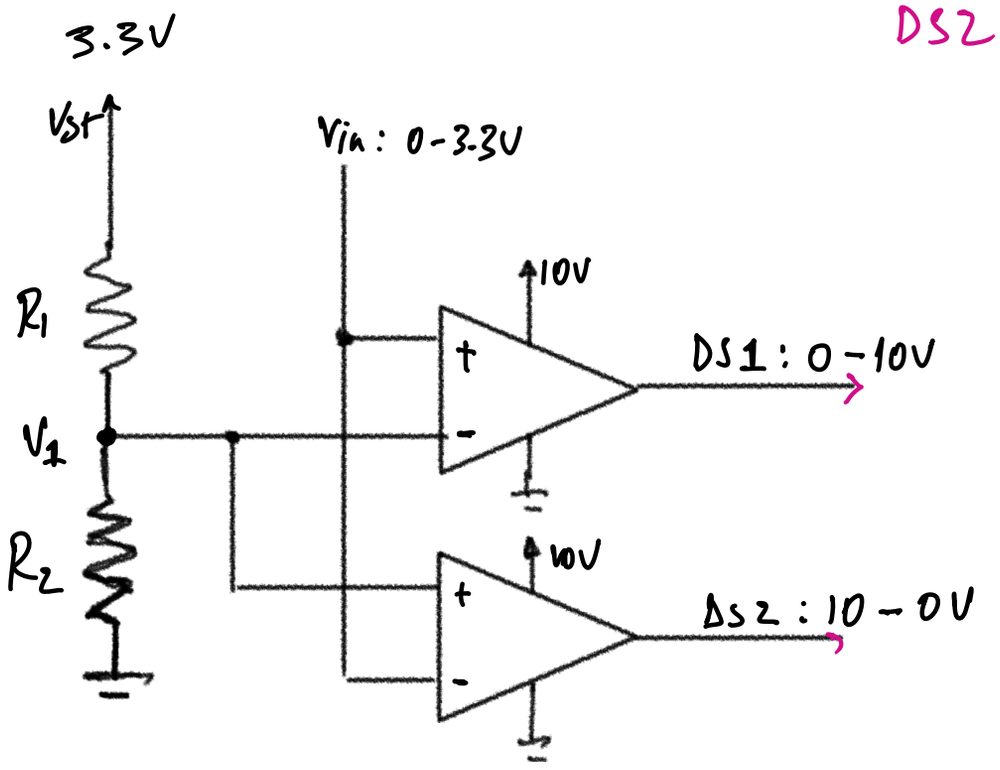
- I have not and shall not allow others to plagiarise my work.
- I have not used an AI language model to generate the code or answers submitted here.

Name: Justice Motaung Signature: 

Question 1 (6 marks)

Circuit Diagram





set $V_1 = 1.65V$

Question 1 (6 marks)

$V_{in} = 0V$

$V_+ < V_- \;:\; DS1 = 0V$

$V_+ > V_- \quad DS2 = 10V$

$V_{in} = 3.3V$

$V_+ > V_- \;:\; DS1 = 10V$

$V_+ < V_- \;:\; DS2 = 0V$

$i_1 = i_2 \Rightarrow R = \frac{V}{I}$ (ohm's) - series

$$\frac{V_{s+} - V_1}{R_1} = \frac{V_1 - GND}{R_2}$$

$$\therefore \frac{V_{s+} - V_1}{V_1} = \frac{R_1}{R_2}$$

$$\therefore \frac{R_1}{R_2} = 1 \Rightarrow \text{Choose } R_2 = 1.5k\Omega$$

$$\therefore R_1 = R_2 = 1.5k\Omega$$

Question 2 (3 marks)

Output Voltages	$V_{in} = 3.3V$ ($V_{in} > V_{ref}$)	$V_{in} = 0V$ ($V_{in} < V_{ref}$)
V_{out1}	+10V (High)	0V
V_{out2}	0V (low)	10V

Question 3 (3 marks)

DS1	DS2	PNP1	PNP2	NPN1	NPN2	V across motor
10V	0V	On	Off	Off	On	10 − 1.4 = 8.6V
0V	10V	Off	On	On	Off	−(10 − 1.4) =

Question 4 (14 marks)

Question 5 (6 marks)

Kp increases the rise time & reduces steady-state error magnitude but when too high increases overshoot and potential oscillation.

Ki eliminates the residual steady state error, error elimination faster with higher Ki value. Although it can cause overshoot and slow settling. Excessive integral action results in oscillations.

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Question 6 (10 marks)

Question 5

- Sampling time
  - * a smaller sampling time will results in more accurate discrete approximation, higher control bandwith but at the cost of CPU load and noise sensitivity
  - * A larger sampling time means CPU overhead will be reduced, but response will be slower, some data could be missed (aliasing) and degraded stability margins.