PSoC® Creator™
Project Datasheet for Keyboard

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Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5 device. For details on all the systems listed above, please refer to the PSoC 5 Technical Reference Manual .

Figure 1. CY8C58LP Device Family Block Diagram

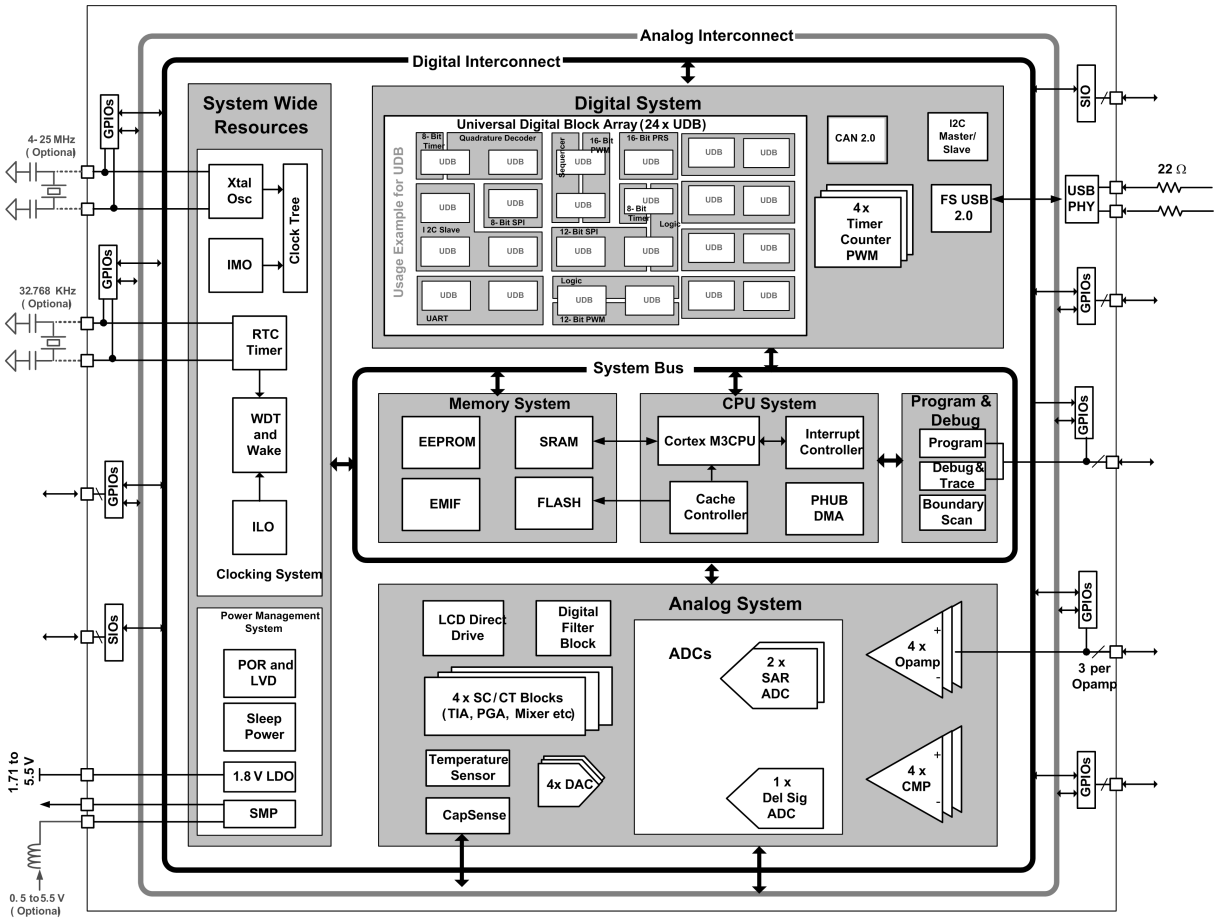


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5888LTI-LP097
Package Name	68-QFN
Architecture	PSoC 5
Family	CY8C58LP
CPU speed (MHz)	80
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E161069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

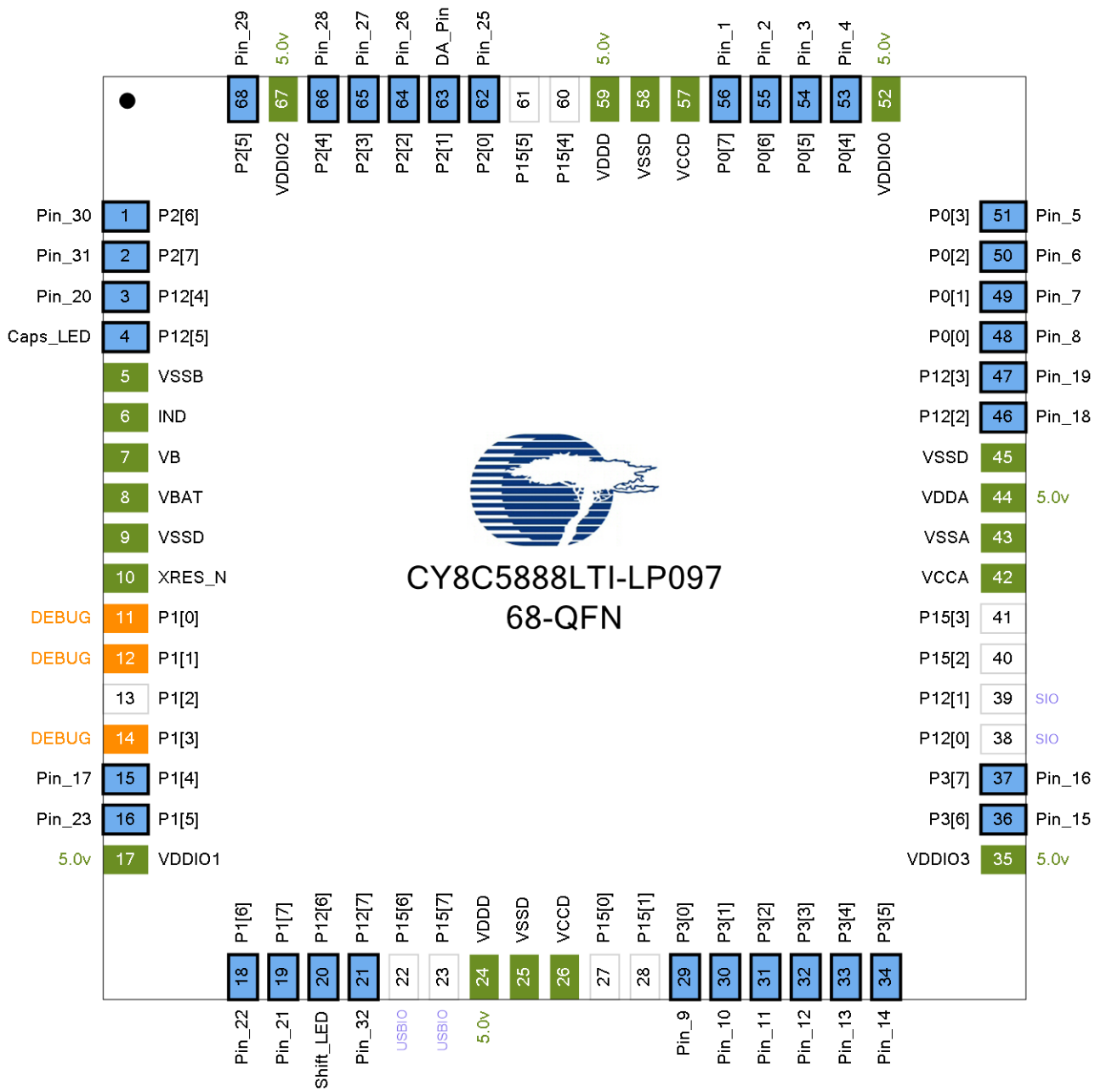
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	0	8	8	0.00 %
Analog Clocks	0	4	4	0.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	0	32	32	0.00 %
IO	37	11	48	77.08 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	0	192	192	0.00 %
Unique P-terms	0	384	384	0.00 %
Total P-terms	0			
Datapath Cells	0	24	24	0.00 %
Status Cells	0	24	24	0.00 %
Control Cells	0	24	24	0.00 %
Opamp	0	4	4	0.00 %
Comparator	0	4	4	0.00 %
Delta-Sigma ADC	0	1	1	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	2	2	0.00 %
Analog (SC/CT) Blocks	0	4	4	0.00 %
DAC				
VIDAC	0	4	4	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[6]	Pin_30	Software Output	Strong drive	HiZ Analog Unb
2	P2[7]	Pin_31	Software Output	Strong drive	HiZ Analog Unb
3	P12[4]	Pin_20	Software Input	Res pull down	HiZ Analog Unb
4	P12[5]	Caps_LED	Software Output	Strong drive	HiZ Analog Unb
5	VSSB	VSSB	Dedicated		
6	IND	IND	Dedicated		
7	VB	VB	Dedicated		
8	VBAT	VBAT	Dedicated		
9	VSSD	VSSD	Power		
10	XRES_N	XRES_N	Dedicated		
11	P1[0]	Debug:SWD_IO	Reserved		
12	P1[1]	Debug:SWD_CK	Reserved		
13	P1[2]	GPIO [unused]			HiZ Analog Unb
14	P1[3]	Debug:SWV	Reserved		
15	P1[4]	Pin_17	Software Input	Res pull down	HiZ Analog Unb
16	P1[5]	Pin_23	Software Input	Res pull down	HiZ Analog Unb
17	VDDIO1	VDDIO1	Power		
18	P1[6]	Pin_22	Software Input	Res pull down	HiZ Analog Unb
19	P1[7]	Pin_21	Software Input	Res pull down	HiZ Analog Unb
20	P12[6]	Shift_LED	Software Output	Strong drive	HiZ Analog Unb
21	P12[7]	Pin_32	Software Output	Strong drive	HiZ Analog Unb
22	P15[6]	USB IO [unused]			HiZ Analog Unb
23	P15[7]	USB IO [unused]			HiZ Analog Unb
24	VDDD	VDDD	Power		
25	VSSD	VSSD	Power		
26	VCCD	VCCD	Power		
27	P15[0]	GPIO [unused]			HiZ Analog Unb
28	P15[1]	GPIO [unused]			HiZ Analog Unb
29	P3[0]	Pin_9	Software Input	Res pull down	HiZ Analog Unb
30	P3[1]	Pin_10	Software Input	Res pull down	HiZ Analog Unb
31	P3[2]	Pin_11	Software Input	Res pull down	HiZ Analog Unb
32	P3[3]	Pin_12	Software Input	Res pull down	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
33	P3[4]	Pin_13	Software Input	Res pull down	HiZ Analog Unb
34	P3[5]	Pin_14	Software Input	Res pull down	HiZ Analog Unb
35	VDDIO3	VDDIO3	Power		
36	P3[6]	Pin_15	Software Input	Res pull down	HiZ Analog Unb
37	P3[7]	Pin_16	Software Input	Res pull down	HiZ Analog Unb
38	P12[0]	SIO [unused]			HiZ Analog Unb
39	P12[1]	SIO [unused]			HiZ Analog Unb
40	P15[2]	GPIO [unused]			HiZ Analog Unb
41	P15[3]	GPIO [unused]			HiZ Analog Unb
42	VCCA	VCCA	Power		
43	VSSA	VSSA	Power		
44	VDDA	VDDA	Power		
45	VSSD	VSSD	Power		
46	P12[2]	Pin_18	Software Input	Res pull down	HiZ Analog Unb
47	P12[3]	Pin_19	Software Input	Res pull down	HiZ Analog Unb
48	P0[0]	Pin_8	Software Input	Res pull down	HiZ Analog Unb
49	P0[1]	Pin_7	Software Input	Res pull down	HiZ Analog Unb
50	P0[2]	Pin_6	Software Input	Res pull down	HiZ Analog Unb
51	P0[3]	Pin_5	Software Input	Res pull down	HiZ Analog Unb
52	VDDIO0	VDDIO0	Power		
53	P0[4]	Pin_4	Software Input	Res pull down	HiZ Analog Unb
54	P0[5]	Pin_3	Software Input	Res pull down	HiZ Analog Unb
55	P0[6]	Pin_2	Software Input	Res pull down	HiZ Analog Unb
56	P0[7]	Pin_1	Software Input	Res pull down	HiZ Analog Unb
57	VCCD	VCCD	Power		
58	VSSD	VSSD	Power		
59	VDDD	VDDD	Power		
60	P15[4]	GPIO [unused]			HiZ Analog Unb
61	P15[5]	GPIO [unused]			HiZ Analog Unb
62	P2[0]	Pin_25	Software Output	Strong drive	HiZ Analog Unb
63	P2[1]	DA_Pin	Software Output	Strong drive	HiZ Analog Unb
64	P2[2]	Pin_26	Software Output	Strong drive	HiZ Analog Unb
65	P2[3]	Pin_27	Software Output	Strong drive	HiZ Analog Unb
66	P2[4]	Pin_28	Software Output	Strong drive	HiZ Analog Unb
67	VDDIO2	VDDIO2	Power		
68	P2[5]	Pin_29	Software Output	Strong drive	HiZ Analog Unb

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Res pull down = Resistive pull down

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	48	Pin_8	Software Input	Res pull down	HiZ Analog Unb
P0[1]	49	Pin_7	Software Input	Res pull down	HiZ Analog Unb
P0[2]	50	Pin_6	Software Input	Res pull down	HiZ Analog Unb
P0[3]	51	Pin_5	Software Input	Res pull down	HiZ Analog Unb
P0[4]	53	Pin_4	Software Input	Res pull down	HiZ Analog Unb
P0[5]	54	Pin_3	Software Input	Res pull down	HiZ Analog Unb
P0[6]	55	Pin_2	Software Input	Res pull down	HiZ Analog Unb
P0[7]	56	Pin_1	Software Input	Res pull down	HiZ Analog Unb
P1[0]	11	Debug:SWD_IO	Reserved		
P1[1]	12	Debug:SWD_CK	Reserved		
P1[2]	13	GPIO [unused]			HiZ Analog Unb
P1[3]	14	Debug:SWV	Reserved		
P1[4]	15	Pin_17	Software Input	Res pull down	HiZ Analog Unb
P1[5]	16	Pin_23	Software Input	Res pull down	HiZ Analog Unb
P1[6]	18	Pin_22	Software Input	Res pull down	HiZ Analog Unb
P1[7]	19	Pin_21	Software Input	Res pull down	HiZ Analog Unb
P12[0]	38	SIO [unused]			HiZ Analog Unb
P12[1]	39	SIO [unused]			HiZ Analog Unb
P12[2]	46	Pin_18	Software Input	Res pull down	HiZ Analog Unb
P12[3]	47	Pin_19	Software Input	Res pull down	HiZ Analog Unb
P12[4]	3	Pin_20	Software Input	Res pull down	HiZ Analog Unb
P12[5]	4	Caps_LED	Software Output	Strong drive	HiZ Analog Unb
P12[6]	20	Shift_LED	Software Output	Strong drive	HiZ Analog Unb
P12[7]	21	Pin_32	Software Output	Strong drive	HiZ Analog Unb
P15[0]	27	GPIO [unused]			HiZ Analog Unb
P15[1]	28	GPIO [unused]			HiZ Analog Unb
P15[2]	40	GPIO [unused]			HiZ Analog Unb
P15[3]	41	GPIO [unused]			HiZ Analog Unb
P15[4]	60	GPIO [unused]			HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P15[5]	61	GPIO [unused]			HiZ Analog Unb
P15[6]	22	USB IO [unused]			HiZ Analog Unb
P15[7]	23	USB IO [unused]			HiZ Analog Unb
P2[0]	62	Pin_25	Software Output	Strong drive	HiZ Analog Unb
P2[1]	63	DA_Pin	Software Output	Strong drive	HiZ Analog Unb
P2[2]	64	Pin_26	Software Output	Strong drive	HiZ Analog Unb
P2[3]	65	Pin_27	Software Output	Strong drive	HiZ Analog Unb
P2[4]	66	Pin_28	Software Output	Strong drive	HiZ Analog Unb
P2[5]	68	Pin_29	Software Output	Strong drive	HiZ Analog Unb
P2[6]	1	Pin_30	Software Output	Strong drive	HiZ Analog Unb
P2[7]	2	Pin_31	Software Output	Strong drive	HiZ Analog Unb
P3[0]	29	Pin_9	Software Input	Res pull down	HiZ Analog Unb
P3[1]	30	Pin_10	Software Input	Res pull down	HiZ Analog Unb
P3[2]	31	Pin_11	Software Input	Res pull down	HiZ Analog Unb
P3[3]	32	Pin_12	Software Input	Res pull down	HiZ Analog Unb
P3[4]	33	Pin_13	Software Input	Res pull down	HiZ Analog Unb
P3[5]	34	Pin_14	Software Input	Res pull down	HiZ Analog Unb
P3[6]	36	Pin_15	Software Input	Res pull down	HiZ Analog Unb
P3[7]	37	Pin_16	Software Input	Res pull down	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- Res pull down = Resistive pull down
- HiZ Analog Unb = Hi-Z Analog Unbuffered

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
Caps_LED	P12[5]	Software Output	HiZ Analog Unb
DA_Pin	P2[1]	Software Output	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P15[4]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
Pin_1	P0[7]	Software Input	HiZ Analog Unb
Pin_10	P3[1]	Software Input	HiZ Analog Unb
Pin_11	P3[2]	Software Input	HiZ Analog Unb
Pin_12	P3[3]	Software Input	HiZ Analog Unb
Pin_13	P3[4]	Software Input	HiZ Analog Unb
Pin_14	P3[5]	Software Input	HiZ Analog Unb
Pin_15	P3[6]	Software Input	HiZ Analog Unb
Pin_16	P3[7]	Software Input	HiZ Analog Unb
Pin_17	P1[4]	Software Input	HiZ Analog Unb
Pin_18	P12[2]	Software Input	HiZ Analog Unb
Pin_19	P12[3]	Software Input	HiZ Analog Unb
Pin_2	P0[6]	Software Input	HiZ Analog Unb
Pin_20	P12[4]	Software Input	HiZ Analog Unb
Pin_21	P1[7]	Software Input	HiZ Analog Unb
Pin_22	P1[6]	Software Input	HiZ Analog Unb
Pin_23	P1[5]	Software Input	HiZ Analog Unb
Pin_25	P2[0]	Software Output	HiZ Analog Unb

Name	Port	Type	Reset State
Pin_26	P2[2]	Software Output	HiZ Analog Unb
Pin_27	P2[3]	Software Output	HiZ Analog Unb
Pin_28	P2[4]	Software Output	HiZ Analog Unb
Pin_29	P2[5]	Software Output	HiZ Analog Unb
Pin_3	P0[5]	Software Input	HiZ Analog Unb
Pin_30	P2[6]	Software Output	HiZ Analog Unb
Pin_31	P2[7]	Software Output	HiZ Analog Unb
Pin_32	P12[7]	Software Output	HiZ Analog Unb
Pin_4	P0[4]	Software Input	HiZ Analog Unb
Pin_5	P0[3]	Software Input	HiZ Analog Unb
Pin_6	P0[2]	Software Input	HiZ Analog Unb
Pin_7	P0[1]	Software Input	HiZ Analog Unb
Pin_8	P0[0]	Software Input	HiZ Analog Unb
Pin_9	P3[0]	Software Input	HiZ Analog Unb
Shift_LED	P12[6]	Software Output	HiZ Analog Unb
SIO [unused]	P12[1]		HiZ Analog Unb
SIO [unused]	P12[0]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

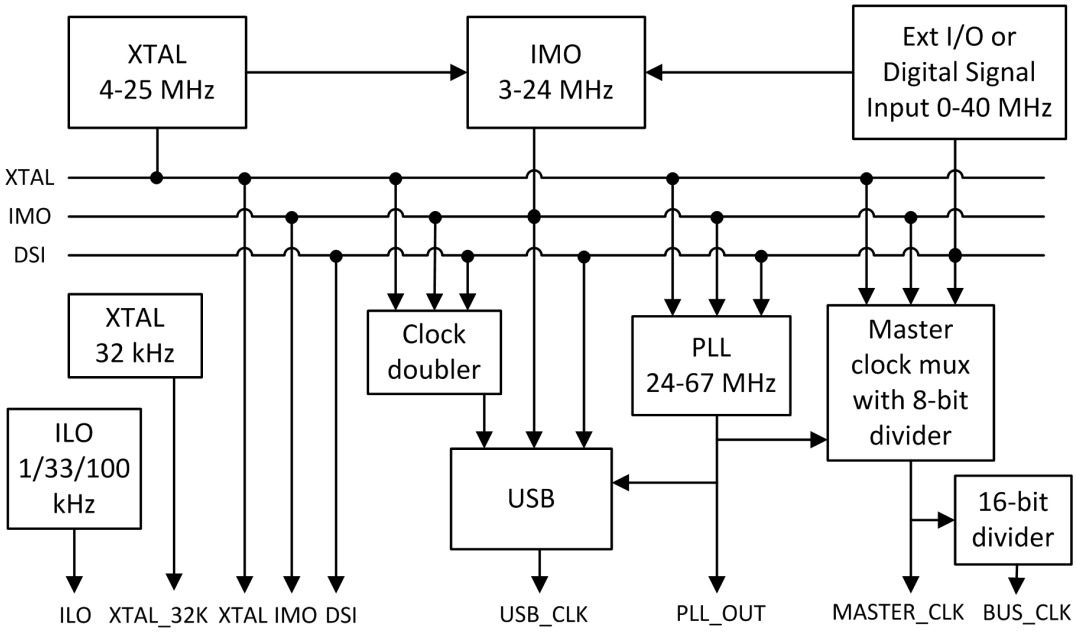
Name	Value
Variable VDDA	False
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains no interrupt components.

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 10 lists the Flash protection settings for your design.

Table 10. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

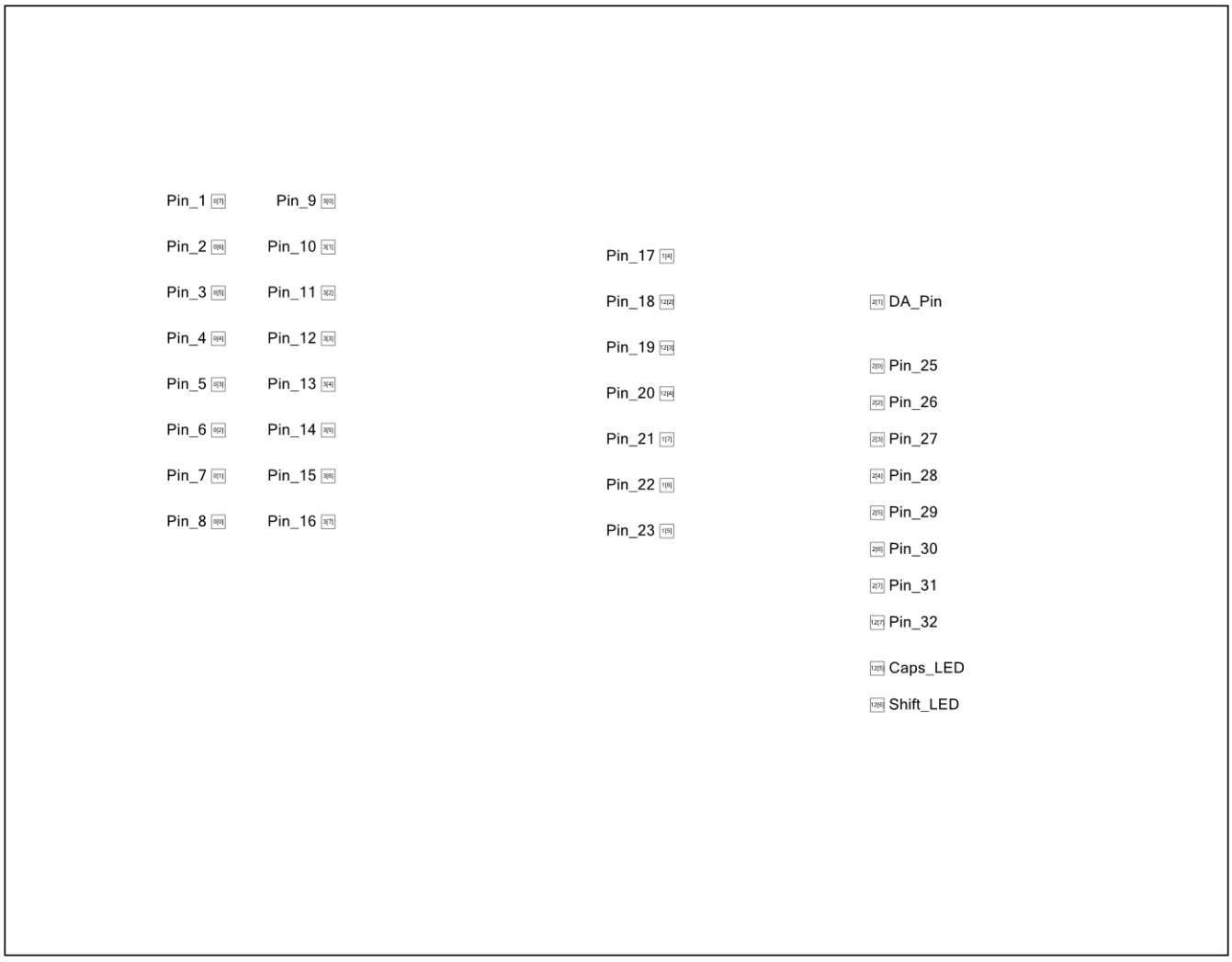
- Flash Protection chapter in the PSoC 5 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 4. Schematic Sheet: Page 1



8 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5 register map is covered in the PSoC 5 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5 Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine