```
Problem 4: [3 points] Drill problem
Filename: hw1prob4.sv
AndrewID: jtbell
```

```
1  `default_nettype none
2
3  module hw1prob4
4    (input logic a, b, c,
5     output logic f, g, h);
6      logic n_a, n_b, n_c, i, j, k, l;
7      not n1 (n_a, a),
8          n2 (n_b, b),
9          n3 (n_c, c);
10
11     and a1(i,n_a,b),
12         a2(j,a,n_b,c),
13         a3(k,n_a,c),
14         a4(l,b,c);
15
16     or  o1(f, i,j),
17         o2(g,i,k,l);
18     xor x1(h,n_a,n_b,n_c);
19 endmodule : hw1prob4
```

Problem 8: [5 points] Drill problem
Filename: hw1prob8.sv
AndrewID: jtbell

```
 1 module hw1prob8
 2    (output logic a, b);
 3    initial begin
 4     a = 0;
 5     b = 1;
 6     #3 a = 1;
 7        b = 0;
 8     #3 a = 0;
 9     #2 b = 1;
10     #5 b = 0;
11        a = 1;
12     #1 a = 0;
13     #4 $finish; end
14
15 endmodule : hw1prob8
16 module top();
17     logic a,b;
18     hw1prob8 t(.a(a),.b(b));
19 endmodule : top
```

```
Problem 11: [6 points] Drill problem
Filename: hw1prob11.sv
AndrewID: jtbell
```

```
1  `default_nettype none
2
3  module original
4      (input logic a, b, c,
5      output logic f);
6      logic h, i;
7
8      and a0(h, a, b);
9      and a1(i, a, c);
10     xor x0(f, h, i);
11
12 endmodule : original
13
14 module app
15     (input logic a, b, c,
16     output logic g);
17     logic h, i;
18
19     xor x0(h, b, c);
20     and(g, a, h);
21 endmodule : app
22
23 module hw1prob11
24     (output logic [2:0] vector,
25     input logic f, g);
26     initial begin
27         $monitor($time, "c = %b, b= %b, a = %b, f = %b, g = %b",
28             vector[2],vector[1],vector[0],f,g);
29     for(vector = 3'b0; vector < 3'd7;vector++) begin
30         #10
31         if (f != g) begin
32             $display("error message");
33             end
34         end
35     #10 $finish; end
36
37 endmodule : hw1prob11
38
39 module system();
40 logic a, b, c, f, g;
41     original org (.a(a),.b(b),.c(c),.f(f));
42     app ap (.a(a),.b(b),.c(c),.g(g));
43     hw1prob11 t (.vector({a,b,c}),.g(g),.f(f));
44
45
46 endmodule : system
47
```