Problem 5: [6 points] Drill problem
Filename: hw3prob5.sv
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```systemverilog
 1 module bcdAdd
 2     (input logic [3:0] a, b,
 3      input logic carryIn,
 4      output logic [3:0] Sum,
 5      output logic carryOut);
 6
 7      logic [4:0] sum_t;
 8
 9      assign sum_t = a + b + carryIn;
10      assign carryOut = (sum_t >= 10) ? 1 : 0;
11      assign Sum = (sum_t >= 10) ? sum_t-10 : sum_t[3:0];
12 endmodule : bcdAdd
13
14 module bcdAdd_test
15     (input logic [3:0] Sum,
16      input logic carryOut,
17      output logic [3:0] a,b,
18      output logic carryIn);
19      initial begin
20          $monitor($time,"sum = %b, carryOut = %b, a = %b, b = %b, carryIn = %b",
21                   Sum,carryOut,a,b,carryIn);
22
23          a = 4'd5; b = 4'd5; carryIn = 1'd0;
24          #10;
25          if(Sum != 4'd0 || carryOut != 4'd1)begin
26              $display("error");
27          end
28          a = 4'd1; b = 4'd3; carryIn = 1'd0;
29          #10;
30          if(Sum != 4'd4 || carryOut != 4'd0)begin
31              $display("error");
32          end
33          a = 4'd9; b = 4'd9; carryIn = 1'd0;
34          #10;
35          if(Sum != 4'd8 ||  carryOut != 4'd1)begin
36              $display("error");
37          end
38          $finish;
39      end
40
41 endmodule : bcdAdd_test
42 module top();
43      logic [3:0] a,  b, Sum;
44      logic carryIn, carryOut;
45          bcdAdd DUT (.a(a),.b(b),.carryIn(carryIn),.Sum(Sum),
46          .carryOut(carryOut));
47          bcdAdd_test test(.a(a),.b(b),.carryIn(carryIn),.Sum(Sum),
48          .carryOut(carryOut));
49
50
51
52 endmodule : top
```