```
Problem 7: [6 points]
Filename: hw4prob7.sv
AndrewID: jtbell
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```
1  `default_nettype none
2
3  module hw4prob7
4    (input  logic clock, reset, a, b,
5     output logic green, yellow, red);
6
7     logic [1:0] state, next_state;
8
9     always_comb begin
10     next_state[1] = ~a&b | ~state[0]|state[1];
11     next_state[0] = (~a&state[1]&state[0] | ~state[1]&~a&b | b&~state[1]
12     &state[0] | ~state[1]&~state[0]&a&~b);
13    end
14    assign red = (~state[1]&state[0] | ~state[0]&~state[1] | state[0]|state[1]);
15    assign yellow =(~state[1]&~state[0] | ~state[0]&state[1]);
16    assign green =(state[1]&state[0] | ~state[0]&state[1]);
17    always_ff @(posedge clock, negedge reset)
18      if (~reset)
19        state <= 2'b0;
20      else
21        state <= next_state;
22
23
24
25
26
27
28
29 endmodule: hw4prob7
```