Problem 1: [12 points] Drill problem
AndrewID: jtbell

Compilation Errors:

```
library_tests.sv: file does not exist
```

Problem 1: [12 points] Drill problem
Filename: library.sv
AndrewID: jtbell

```
`default_nettype none
module multiplexer8
(input logic I0, I1, I2, I3, I4, I5, I6, I7,
input logic [2:0] S, output logic Y);

    logic [7:0] v;
    assign v[0] =  (~S[0] & ~S[1] & ~S[2] & I0);
    assign v[1] =  (S[0] & ~S[1] & ~S[2] & I1);
    assign v[2] =  (~S[0] & S[1] & ~S[2] & I2);
    assign v[3] =  (S[0] & S[1] & ~S[2] & I3);
    assign v[4] =  (~S[0] & ~S[1] & S[2] & I4);
    assign v[5] =  (S[0] & ~S[1] & S[2] & I5);
    assign v[6] =  (~S[0] & S[1] & S[2] & I6);
    assign v[7] =  (S[0] & S[1] & S[2] & I7);
    assign Y = v[0] | v[1] | v[2] | v[3] | v[4] | v[5] | v[6] | v[7];
endmodule : multiplexer8
```

```
Problem 1: [12 points] Drill problem
Filename: library_tests.sv
AndrewID: jtbell

File library_tests.sv was not found
```

Problem 3: [4 points] Drill problem
Filename: hw2prob3.sv
AndrewID: jtbell

```
module hw2prob3
    (input logic [0:3] a,
    output logic y);

    assign y = a[0] ^ a[1] ^ a[2] ^ a[3];


endmodule: hw2prob3
```

Problem 4: [6 points]
Filename: hw2prob4.sv
AndrewID: jtbell

```
module Minority
    (output logic y,
    input logic a, b, c, d, e);

    assign y = (a+b+c+d+e < 3) ? 1 : 0;

endmodule : Minority

module Minority_tb
    (input logic y,
    output logic [4:0] vector);
        initial begin
        $monitor($time,,"e = %b, d = %b, c = %b, b = %b, a = %b, y = %b", vec...
Line length of 84 (max is 80)
        vector[3],vector[2],vector[1],vector[0],y);
        for (vector = 5'b0; vector < 5'd31;vector++) #10;
        $finish;
        end

endmodule : Minority_tb

module top();
    logic a,b,c,d,e,y;
        Minority m (.*);
        Minority_tb m_tb (.vector({a,b,c,d,e}),.y(y));

endmodule : top
```

Problem 5: [8 points]
AndrewID: jtbell

Compilation Errors:

```
hw2prob5.sv, library.sv: failed to compile

Error-[MPD] Module previously declared
  The module was previously declared at:
  ".../hw2prob5.sv",
  2
  It is redeclared later at:
  ".../library.sv",
  2: token is 'multiplexer8'
  module multiplexer8
                     ^
  Please remove one of the declarations and compile again.

1 error
```

Problem 5: [8 points]
Filename: hw2prob5.sv
AndrewID: jtbell

```
`default_nettype none
module multiplexer8
(input logic I0, I1, I2, I3, I4, I5, I6, I7,
input logic [2:0] S, output logic Y);

    logic [7:0] v;
    assign v[0] =  (~S[0] & ~S[1] & ~S[2] & I0);
    assign v[1] =  (S[0] & ~S[1] & ~S[2] & I1);
    assign v[2] =  (~S[0] & S[1] & ~S[2] & I2);
    assign v[3] =  (S[0] & S[1] & ~S[2] & I3);
    assign v[4] =  (~S[0] & ~S[1] & S[2] & I4);
    assign v[5] =  (S[0] & ~S[1] & S[2] & I5);
    assign v[6] =  (~S[0] & S[1] & S[2] & I6);
    assign v[7] =  (S[0] & S[1] & S[2] & I7);
    assign Y = v[0] | v[1] | v[2] | v[3] | v[4] | v[5] | v[6] | v[7];
endmodule : multiplexer8


module hw2prob5
    (input logic A,B,C,D,
    output logic F);

   logic [7:0]mux1,X1,X2;
   logic n_A;
   not n1(n_A,A);

   multiplexer8   m1(.I0(1'b0),.I1(A),.I2(A),.I3(n_A),.I4(n_A), .I5(1'b1), .I...
Line length of 114 (max is 80)



endmodule : hw2prob5

module hw2prob5_test
    (input logic F,
    output logic A,B,C,D);

    logic [3:0] vector;
    logic testF;

    initial begin

    for (vector = 4'b0; vector < 4'd15;vector++) begin;
      assign A =  vector[0];
      assign B =  vector[1];
      assign C =  vector[2];
      assign D =  vector[3];
      assign testF = (~A&~B&C&D)|(~A&B)|(A&B&D)|(A&~B&C&~D)|(A&~C&D);
        $monitor($time,, "A = %b, B = %b, C = %b, D = %b, F = %b",A,B,C,D,F);
        #10;
        if(F != testF)begin
             $display("error");
            end
        end
    end
endmodule : hw2prob5_test


module top();
    logic A,B,C,D,F;

    hw2prob5 h (.A(A),.B(B),.C(C),.D(D),.F(F));
    hw2prob5_test h1 (.A(A),.B(B),.C(C),.D(D),.F(F));

endmodule : top
```

Problem 6: [12 points]
Filename: hw2prob6.sv
AndrewID: jtbell

```
module hw2prob6
    (input logic a,b,c,d,e,f,
    output logic g,g00,g01,g10,g11);



    assign g11 = (~a|~e)&(~a|~b|d|e)&(a|~b|~d|e)&(~a|~b|~e)&(a|b|d|~e)&(~d|~e);
    assign g10 = (d|e)&(a|~b|~d|e)&(a|b)&(~(a^d)|b|e)&(~a|b|~e)&(a|b|d|~e);
    assign g01 = (~a|~b|d|e)&(~a|b|~d|~e)&(~a|~b|~e)&(a|~b|~d|~e)&(~b|d|e)&(a...
Line length of 86 (max is 80)
    assign g00 = (~(a^d)|b|e)&(~a|b|~e)&(~b|d|e)&(a|~b|~d|~e)&(a|b|d|~e);

    assign g = ((g00&(~c&~f)|g11&(c&f))|(g01&(~c&f)| g10&(c&~f)));

endmodule : hw2prob6

module hw2prob6_test
    (input logic g, g00, g01,g11,g10,
    output logic a,b,c,d,e,f);
    logic ogG;
    logic [5:0]vector;
    initial begin

    for(vector = 6'd0;vector < 6'd63;vector++)begin
    assign a = vector[0];
    assign b = vector[1];
    assign c = vector[2];
    assign d = vector[3];
    assign e = vector[4];
    assign f = vector[5];
    assign ogG = (~a|~c|~e|~f)&(~a|~b|d|e|~f)&(~c|~d|~e|~f)&
                (~c|d|e|f)&(a|~b|~c|~d|e)&(a|b|~c|f)&(~a|b|c|~d|~e|~f)&
                (~a|~b|~e|~f)&(~(a^d)|b|e|f)&(~a|b|~e|f)&(~b|c|d|e)&(a|~b|c|~...
Line length of 83 (max is 80)
                (a|b|d|~e);
        $monitor($time,, "abcdef=%b,g00 = %b, g11 = %b, g10 = %b, g01 = %b, g...
Line length of 110 (max is 80)
        #10;
        if(g != ogG)begin
            $display("Oops!");

             end

        end
        $finish;
   end
endmodule: hw2prob6_test
module top();
    logic a,b,c,d,e,f,g00,g10,g01,g11,g;
    hw2prob6 DUT (.a(a),.b(b),.c(c),.d(d),.e(e),.f(f),.g00(g00),.g01(g01),.g1...
Line length of 101 (max is 80)
    hw2prob6_test Test (.a(a),.b(b),.c(c),.d(d),.e(e),.f(f),.g00(g00),.g01(g0...
Line length of 107 (max is 80)
endmodule: top
```

Problem 7: [4 points]
Filename: hw2prob7.sv
AndrewID: jtbell

```
`default_nettype none
module hw2prob7
  (input logic [10:0]year,
   output logic leap4);

     logic [10:0]q;
     assign q = year >> 2;
     always_comb begin
        if (q+q+q+q == year)
            leap4 = 1;
        else
            leap4 = 0;
      end

endmodule : hw2prob7

module hw2prob7_test
    (input logic leap4,
    output logic [10:0]year);

    initial begin
    $monitor($time,,"year = %b, leap4 = %b",year,leap4);
        for (year = 11'd2000; year <= 11'd2021;year++) #10;
    #10
    $finish;
    end
endmodule : hw2prob7_test;

module top();
    logic [10:0]year, leap4;
    hw2prob7 DUT (.year(year),.leap4(leap4));
    hw2prob7_test tb (.year(year),.leap4(leap4));
endmodule : top
```

Problem 7: [4 points]
Filename: library.sv
AndrewID: jtbell

```
`default_nettype none
module multiplexer8
(input logic I0, I1, I2, I3, I4, I5, I6, I7,
input logic [2:0] S, output logic Y);

    logic [7:0] v;
    assign v[0] =  (~S[0] & ~S[1] & ~S[2] & I0);
    assign v[1] =  (S[0] & ~S[1] & ~S[2] & I1);
    assign v[2] =  (~S[0] & S[1] & ~S[2] & I2);
    assign v[3] =  (S[0] & S[1] & ~S[2] & I3);
    assign v[4] =  (~S[0] & ~S[1] & S[2] & I4);
    assign v[5] =  (S[0] & ~S[1] & S[2] & I5);
    assign v[6] =  (~S[0] & S[1] & S[2] & I6);
    assign v[7] =  (S[0] & S[1] & S[2] & I7);
    assign Y = v[0] | v[1] | v[2] | v[3] | v[4] | v[5] | v[6] | v[7];
endmodule : multiplexer8
```

Problem 8: [4 points]
Filename: hw2prob8.sv
AndrewID: jtbell

```
`default_nettype none
module hw2prob8
  (input logic [10:0]year,
   output logic leap4_100_400);

     logic [10:0] q;
     assign q = year >> 2;
     always_comb begin
        if (q+q+q+q == year)
            leap4_100_400 = 1'b1;
        else
            leap4_100_400 = 1'b0;
        case(year)
            11'd100: leap4_100_400 = 0;
            11'd200: leap4_100_400 = 0;
            11'd300: leap4_100_400 = 0;
            11'd400: leap4_100_400 = 1;
            11'd500: leap4_100_400 = 0;
            11'd600: leap4_100_400 = 0;
            11'd700: leap4_100_400 = 0;
            11'd800: leap4_100_400 = 1;
            11'd900: leap4_100_400 = 0;
            11'd1000: leap4_100_400 = 0;
            11'd1100: leap4_100_400 = 0;
            11'd1200: leap4_100_400 = 1;
            11'd1300: leap4_100_400 = 0;
            11'd1400: leap4_100_400 = 0;
            11'd1500: leap4_100_400 = 0;
            11'd1600: leap4_100_400 = 1;
            11'd1700: leap4_100_400 = 0;
            11'd1800: leap4_100_400  = 0;
            11'd1900: leap4_100_400 = 0;
            11'd2000: leap4_100_400 = 1;
            endcase
      end

endmodule : hw2prob8

module hw2prob8_test
    (input logic leap4_100_400,
    output logic [10:0]year);

    initial begin
    $monitor($time,,"year = %b, leap4_100_400 = %b",year,leap4_100_400);
        for (year = 11'd2000; year <= 11'd2021;year++) #10;
        $display("This output is from 0-2000 checking for leap year");
        for (year = 11'd000; year < 11'd2000;year = year + 100) #10;
        #10;
    $finish;
    end
endmodule : hw2prob8_test;

module top();
    logic [10:0]year, leap4_100_400;
    hw2prob8 DUT (.year(year), .leap4_100_400(leap4_100_400));
    hw2prob8_test test (.year(year),.leap4_100_400(leap4_100_400));
endmodule : top
```

Problem 9: [8 points]
Filename: hw2prob9.sv
AndrewID: jtbell

```
module Divider_C
    (input logic a,b,c,d,
    output logic e,f,g,h);

    logic n_c,n_b,n_a,n_d;
    logic X,X1,X2,X3,X4,X5;

    not n1(n_b,b),
        n2(n_a,a),
         n3(n_c,c),
         n4(n_d,d);

    and a1(e,a,n_c);

    and b1(X,n_a,b),
        b2(X1,n_a,n_c,b),
        b3(X2,a,n_c,d),
        b4(g,a,n_b,c,d),
        b5(X4,b,n_c),
        b6(X5,n_a,b,d);

    or o1(f,X,X1,X2),
       o2(h,X4,X5);

endmodule: Divider_C

module Divider_D
    (input logic a,b,c,d,
    output logic e,f,g,h);

    assign e = a & ~c;
    assign f = ~a&b |  ~a&b&~c | a&~c&d;
    assign g = a&~b&c&d;
    assign h = b&~c | ~a&b&d;

endmodule: Divider_D
```