

## 2021 Digital IC Design Homework 1

NAME	高士鈞																																						
Student ID	N26094922																																						
<b>Simulation Result</b>																																							
Functional simulation	pass	Gate-level simulation	pass	Gate-level simulation time	N/A																																		
<div style="text-align: center;">(your pre-sim result)</div> <pre style="font-family: monospace; font-size: 0.8em;">#      494 data is correct #      495 data is correct #      496 data is correct #      497 data is correct #      498 data is correct #      499 data is correct #      500 data is correct #      501 data is correct #      502 data is correct #      503 data is correct #      504 data is correct #      505 data is correct #      506 data is correct #      507 data is correct #      508 data is correct #      509 data is correct #      510 data is correct #      511 data is correct #-----PASS----- # All data have been generated successfully! # Break in Module RCA_tb at D:/classes/DIC/HW1/RCA_tb.v line 45</pre>			<div style="text-align: center;">(your post-sim result)</div> <pre style="font-family: monospace; font-size: 0.8em;">#      495 data is correct #      496 data is correct #      497 data is correct #      498 data is correct #      499 data is correct #      500 data is correct #      501 data is correct #      502 data is correct #      503 data is correct #      504 data is correct #      505 data is correct #      506 data is correct #      507 data is correct #      508 data is correct #      509 data is correct #      510 data is correct #      511 data is correct #-----PASS----- # All data have been generated successfully! # Break in Module RCA_tb at D:/classes/DIC/HW1/RCA_tb.v line 45</pre>																																				
<b>Synthesis Result</b>																																							
Total logic elements		10																																					
Total memory bit		0																																					
Embedded multiplier 9-bit element		0																																					
Clock Width (Cycle)		10																																					
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #0070C0; color: white;"> <th colspan="2">Flow Summary</th> </tr> </thead> <tbody> <tr> <td>Flow Status</td> <td>Successful - Wed Mar 31 12:58:41 2021</td> </tr> <tr> <td>Quartus II 64-Bit Version</td> <td>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</td> </tr> <tr> <td>Revision Name</td> <td>RCA</td> </tr> <tr> <td>Top-level Entity Name</td> <td>RCA</td> </tr> <tr> <td>Family</td> <td>Cyclone II</td> </tr> <tr> <td>Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Total logic elements</td> <td>10 / 68,416 ( &lt; 1 % )</td> </tr> <tr> <td>    Total combinational functions</td> <td>10 / 68,416 ( &lt; 1 % )</td> </tr> <tr> <td>    Dedicated logic registers</td> <td>0 / 68,416 ( 0 % )</td> </tr> <tr> <td>Total registers</td> <td>0</td> </tr> <tr> <td>Total pins</td> <td>14 / 622 ( 2 % )</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 1,152,000 ( 0 % )</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>0 / 300 ( 0 % )</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 ( 0 % )</td> </tr> </tbody> </table>						Flow Summary		Flow Status	Successful - Wed Mar 31 12:58:41 2021	Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition	Revision Name	RCA	Top-level Entity Name	RCA	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Total logic elements	10 / 68,416 ( < 1 % )	Total combinational functions	10 / 68,416 ( < 1 % )	Dedicated logic registers	0 / 68,416 ( 0 % )	Total registers	0	Total pins	14 / 622 ( 2 % )	Total virtual pins	0	Total memory bits	0 / 1,152,000 ( 0 % )	Embedded Multiplier 9-bit elements	0 / 300 ( 0 % )	Total PLLs	0 / 4 ( 0 % )
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<b>Description of your design</b>																																							
<p>First design a gate-level half adder with XOR and AND gate. Then combine two half adder to get a full adder, which is the basic element for target ripple carry adder.</p> <p>To get a 4-bits full adder, we connect four basic full adder to reach out target.</p>																																							