2021 Digital IC Design Homework 2

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	N/A

```
#        4012 data is correct
#        4013 data is correct
#        4014 data is correct
#        4015 data is correct
#        4016 data is correct
#        4017 data is correct
#        4018 data is correct
#        4019 data is correct
#        4020 data is correct
#        4021 data is correct
#        4022 data is correct
#        4023 data is correct
#        4024 data is correct
#        4025 data is correct
#        4026 data is correct
#        4027 data is correct
#        4028 data is correct
#        4029 data is correct
#        4030 data is correct
#        4031 data is correct
#        4032 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module booth_tb at D:/classes/DIC/HW2/booth_tb.v line 43
```

```
#        4020 data is correct
#        4021 data is correct
#        4022 data is correct
#        4023 data is correct
#        4024 data is correct
#        4025 data is correct
#        4026 data is correct
#        4027 data is correct
#        4028 data is correct
#        4029 data is correct
#        4030 data is correct
#        4031 data is correct
#        4032 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module booth_tb at D:/classes/DIC/HW2/booth_tb.v line 43
```

Synthesis Result

Total logic elements	107
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	30

Flow Summary	
Flow Status	Successful - Wed Apr 14 11:04:22 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	booth
Top-level Entity Name	booth
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	107 / 68,416 (< 1 %)
Total combinational functions	107 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	24 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

本題的 testbench 因為沒有給 clk 訊號，所以整個電路都需要用 combinational 完成，這裡採用的方式是用 for loop 複製出好幾份會根據 P[1:0]選擇不同模式的運算子電路；特別要注意在對 P 做運算時要以有號數處理以免出現溢位狀況，最後再將運算完成的 P 捨去 LSB 作為輸出的 output。

Scoring = Clock width