2021 Digital IC Design Homework 3

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	13820 (ns)

```
#
# Object38: PASS
#
# Object39: PASS
#
# Object40: PASS
#
# Object41: PASS
#
# Object42: PASS
#
# Object43: PASS
#
# Object44: PASS
#
# Object45: PASS
#
# Object46: PASS
#
# Object47: PASS
#
# Object48: PASS
#
# Object49: PASS
#
# Object50: PASS
#
# ------------------------------------------------------
# --    Simulation finish,  ALL PASS             --
# ------------------------------------------------------
# ** Note: $finish    : D:/classes/DIC/HW3/tb.sv(180)
#    Time: 34550 ns  Iteration: 1  Instance: /testfixture
# 1
# Break in Module testfixture at D:/classes/DIC/HW3/tb.sv line 180

VSIM 37>
```

```
# Object42: PASS
#
# Object43: PASS
#
# Object44: PASS
#
# Object45: PASS
#
# Object46: PASS
#
# Object47: PASS
#
# Object48: PASS
#
# Object49: PASS
#
# Object50: PASS
#
# ------------------------------------------------------
# --    Simulation finish,  ALL PASS             --
# ------------------------------------------------------
# ** Note: $finish    : D:/classes/DIC/HW3_post/tb.sv(180)
#    Time: 13820 ns  Iteration: 1  Instance: /testfixture
# 1
# Break in Module testfixture at D:/classes/DIC/HW3_post/tb.sv line 180
```

Synthesis Result

Total logic elements	611
Total memory bit	0
Embedded multiplier 9-bit element	4
Clock width (Cycle)	20

Flow Summary	
Flow Status	Successful - Wed May 12 12:16:48 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	PSE
Top-level Entity Name	PSE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	611 / 68,416 (< 1 %)
Total combinational functions	611 / 68,416 (< 1 %)
Dedicated logic registers	135 / 68,416 (< 1 %)
Total registers	135
Total pins	46 / 622 (7 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	0 / 4 (0 %)

Description of your design
Sorting 演算法採用常見的 bubble sort，雖然沒有發會硬體電路 reuse 特性，但相對較為穩健且易於理解。另外在計算外積時採用 assign 的寫法，讓 code 版面較為簡潔，sorting 的 sequential 電路只透過 combinational 算出的 swap 訊號決定是否交換位子，整體分工明確。整個系統採用 state machine 清楚劃分各階段工作，LOAD SORT OUT 三者不互相干擾。

Scoring = Total logic elements