2021 Digital IC Design Homework 4

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	8,110,226 (ns)

(your pre-sim result)

```
VSIM 26> run -all
# ------------------------------------------------------
#
# START!!! Simulation Start .....
#
# ------------------------------------------------------
#
#  Result image is correct !
#
# ------------------------------------------------------
#
# --------------------- S U M M A R Y -----------------
#
# Congratulations! Result image data have been generated successfully! The result is PASS!!
#
# ------------------------------------------------------
#
# ** Note: $finish    : D:/classes/DIC/HW4/testfixture.v(123)
#    Time: 1228875 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/classes/DIC/HW4/testfixture.v line 123
```

(your post-sim result)

```
VSIM 4> run -all
# ------------------------------------------------------
#
# START!!! Simulation Start .....
#
# ------------------------------------------------------
#
#  Result image is correct !
#
# ------------------------------------------------------
#
# --------------------- S U M M A R Y -----------------
#
# Congratulations! Result image data have been generated successfully! The result is PASS!!
#
# ------------------------------------------------------
#
# ** Note: $finish    : D:/classes/DIC/HW4_post/testfixture.v(123)
#    Time: 8110226132 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result	
Total logic elements	1319
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	45

(your flow summary)

Flow Summary	
Flow Status	Successful - Sun Jun 13 00:46:57 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	MFE
Top-level Entity Name	MFE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	1,319 / 68,416 (2 %)
Total combinational functions	1,318 / 68,416 (2 %)
Dedicated logic registers	105 / 68,416 (< 1 %)
Total registers	105
Total pins	57 / 622 (9 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

一開始的作法是把整張圖片讀進 reg 再做處理，但後來發現這樣會塞爆 FPGA，所以改為一次只讀入當下所需的 9 個 pixel，讀入之後再用基本的 bubble sort 挑出中間值並丟回 testbench；為了處理邊界條件，我把所有情況的所需的 data address 規則都一一條列(4 個 corner case, 4 個 side case, 1 個 general case)，再根據上面所得到的 9 個地址跟 testbench 討資料，如此就可以解掉 padding 的問題了!

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*