2021 Digital IC Design Homework 5

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	71197 (ns)

PRESIM

```
# ------------------------------------------------------
# FFT dataout on pattern         784 ~         799, PASS!!
# FFT dataout on pattern         800 ~         815, PASS!!
# FFT dataout on pattern         816 ~         831, PASS!!
# FFT dataout on pattern         832 ~         847, PASS!!
# FFT dataout on pattern         848 ~         863, PASS!!
# FFT dataout on pattern         864 ~         879, PASS!!
# FIR dataout on pattern         800 ~         900 !!, PASS !!
# ------------------------------------------------------
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/justi/Desktop/HW5/testfixture1.v(240)
#    Time: 104700 ns  Iteration: 0  Instance: /testfixture1
```

POSTSIM

```
# ------------------------------------------------------
# FFT dataout on pattern         784 ~         799, PASS!!
# FFT dataout on pattern         800 ~         815, PASS!!
# FFT dataout on pattern         816 ~         831, PASS!!
# FFT dataout on pattern         832 ~         847, PASS!!
# FFT dataout on pattern         848 ~         863, PASS!!
# FFT dataout on pattern         864 ~         879, PASS!!
# FIR dataout on pattern         800 ~         900 !!, PASS !!
# ------------------------------------------------------
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/justi/Desktop/HW5_pos/testfixture2.v(241)
#    Time: 71197 ns  Iteration: 0  Instance: /testfixture2
```

Synthesis Result	
Total logic elements	6365
Total memory bit	0
Embedded multiplier 9-bit element	112
Clock width (Cycle)	35

(your flow summary)

Flow Summary	
Flow Status	Successful - Tue Jun 29 11:01:45 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FAS
Top-level Entity Name	FAS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	6,365 / 68,416 (9 %)
Total combinational functions	6,059 / 68,416 (9 %)
Dedicated logic registers	2,560 / 68,416 (4 %)
Total registers	2560
Total pins	554 / 622 (89 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	112 / 300 (37 %)
Total PLLs	0 / 4 (0 %)

Description of your design

這次電路主要有三大區塊，FIR FFT analysis，我把它獨立成三個 module 方便 debug；FIR 部分用類似 16 級 pipeline 的概念去接 input，如此可以每個 cycle 都產生出一筆運算完的 fir_d；FFT 共有四個階層，所以我採用了 4 stage pipeline 降低 critical path 長度，其他就是照刻；analysis 部分就相對簡單，單純找出 16 筆資料中平方和最大者即可!

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*