Justin Hsu

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Github, Projects Web Page

Education

UC Davis

Bachelor of Science in Electrical Engineering
Expected graduation: June 2026

Skills

Programming - C, Python, Verilog, TCL, MATLAB

Software - ICC2, Design Compiler, HSPICE, Prime, VCS, OrCAD, Virtuoso, Spectre, Xcelium, PADS, CAM350, Vivado, Vitis, MAGIC, Yosys, KLayout, ModelSim, Quartus

Coursework

EEC 118 - Digital Integrated Circuits
EEC 116 - VLSI Design *(planned)*
EEC 216 - Low Power Digital IC Design *(planned)*
EEC 180 - Digital Systems II
EEC 289O - IC Design and Tapeout *(planned)*
EEC 283 - Advanced Design Verification Of Digital Systems

Organizations

Aggie Propulsion and Rocketry Labs

- Designed 4-layer PCBs in OrCAD with focus on signal integrity and power delivery for measuring instrumentation.
- Implemented SPI and I2C communication between onboard ICs to ensure reliable sensor interfacing.

UC Davis IEEE

Employment

Lotus Communication Systems - June 2025 ~ September 2025

- Developed a 2 channel jamming-resistant GPS receiving system on L1 band using the Xilinx Zynq 7000 SoC, using Vivado for Verilog RTL development to implement digital FIR filters for signal cleaning.
- Wrote C code in Vitis to perform Cholesky decomposition on the CPU and manage communication with various onboard ICs like DDR and flash using UART, I2C, and QSPI.
- Integrated and optimized system components to enhance GPS signal clarity and robustness against interference.

Lotus Communication Systems - June 2024 ~ September 2024

- Designed schematics using OrCAD and laid out the 4-layer PCB using PADS and CAM350 for a mixed-signal two-channel block up/down converter.
- Integrated digital microcontroller block and RF components, ensuring optimal signal integrity and performance.
- Performed DFM checks, signal analysis, and generated Gerber files for production.

Projects

32 Bit MIPS CPU - November 2024 ~ Present

- Designed a 32-bit MIPS CPU in Verilog with 5 stage pipelined datapath, hazard detection, and forwarding logic.
- Conducting ASIC layout using Synopsys Design Compiler and Skywater 130nm PDK. Performed RTL synthesis, static timing analysis, and clock tree synthesis. Optimizing design through efficient place-and-route and floorplanning.
- Implementing low power techniques like clock gating and variable supply.

Systolic Matrix Multiplier - January 2025 ~ June 2025

- Developed an 8×8 systolic array matrix multiplier in Verilog and carried it through RTL-to-GDSII implementation using Skywater 130nm PDK.
- Applied low-power physical design techniques including clock/circuit gating, power-aware floorplanning, and optimized placement of MAC units to reduce switching activity and area overhead.
- Achieved timing closure through careful pipelining, constraint tuning, and optimization across synthesis and place-and-route.

Configurable Logic Block Verification Tool - April 2025 ~ June 2025

- Implemented a Python-based verification framework using the PODEM algorithm to generate test vectors for fault detection in a Configurable Logic Block (CLB) within an FPGA.
- Modeled and verified the CLB components—including look up table (LUT), flip-flop, and multiplexer—to ensure functional correctness and fault coverage.

Game Boy Advance Core - August 2025 ~ Present

- Designing and implementing a Game Boy Z80 core, following RTL to GDSII pipeline.
- Conducting ASIC layout using Synopsys Design Compiler and Skywater 130nm PDK. Performed RTL synthesis, static timing analysis, and clock tree synthesis. Optimized design through efficient place-and-route and floorplanning.
- Developing modules using Verilog like a VGA controller, Z80 CPU, video memory, ROM, and SDRAM controller.