Justin Hsu

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LinkedIn, Github, Projects Web Page

Education

University of California, San Diego
Master of Science in Electrical Engineering
Expected graduation: June 2028

University of California, Davis
Bachelor of Science in Electrical Engineering
Expected graduation: June 2026

Skills

Programming - C, Python, Verilog, TCL, MATLAB

Software - ICC2, Innovus, Design Compiler, HSPICE, Prime, VCS, OrCAD, Virtuoso, Spectre, Xcelium, PADS, CAM350, Vivado, Vitis, MAGIC, Yosys, KLayout, ModelSim, Quartus

Coursework

EEC 116 - VLSI Design

EEC 118 - Digital Integrated Circuits

EEC 180 - Digital Systems II

EEC 216 - Low Power Digital IC Design

EEC 289Q - Hardware for Machine Learning *(planned)*

Organizations

Aggie Propulsion and Rocketry Labs
- Designed 4-layer PCBs in OrCAD with focus on signal integrity and power delivery for measuring instrumentation.
- Implemented SPI and I2C communication between onboard ICs to ensure reliable sensor interfacing.

Employment

Lotus Communication Systems - **RTL Design Engineer**- June 2025 ~ September 2025
- Developed a 2 channel jamming-resistant GPS receiving system on L1 band using the Xilinx Zynq 7000 SoC, using Vivado for Verilog RTL development to implement digital FIR filters and block up down converters.
- Wrote C code in Vitis to perform Cholesky decomposition on the CPU and manage communication with various onboard ICs like DDR and flash using UART, I2C, and QSPI.
- Integrated and optimized system components to enhance GPS signal clarity and robustness against interference.

Lotus Communication Systems - **PCB Design Engineer** - June 2024 ~ September 2024
- Designed schematics using OrCAD and laid out the 4-layer PCB using PADS and CAM350 for a mixed-signal two-channel block up/down converter.
- Integrated digital microcontroller block and RF components, ensuring optimal signal integrity and performance.
- Performed DFM checks, signal analysis, and generated Gerber files for production.

Projects

Subthreshold Minimum Energy 32 Bit Adder - January 2026 ~ Present
- Designed a pipelined subthreshold 32 bit adder operating at 100 MHz in Cadence Virtuoso using the NCSU 45nm PDK. Utilized a ripple carry static CMOS adder architecture implementing mirror full adder and clock gating.
- Conducted layout of this adder in Virtuoso and simulated for functionality using Spectre.

Multicore RISC-V Processor - January 2026 ~ Present
- Created a framework to implement big.LITTLE architecture to a multi-core RISC-V processor with cache coherence.
- Designed each core with a custom cache to meet target performance and efficiency metric through pipelining and low power techniques in SystemVerilog, verified functionality with Xcelium.
- Implementing physical layout using OpenLane VLSI flow with the Caravel SoC harness using custom layout scripts.

Live Video Feed Edge Detection Accelerator - September 2025 ~ Present
- Implemented a Canny edge detection accelerator on a DE1-SoC-utilizing Verilog to create accelerator modules for Calculating Gaussian blur and Sobel gradient, and utilizing the onboard Arm Cortex A9 CPU to compute Hysteresis Edge Tracking through an algorithm written in C.
- Developed additional modules in Verilog for 11x11 convolutional 2-D blurring filter and vignetting for video effects.

Systolic Matrix Multiplier - January 2025 ~ June 2025
- Designed an 8x8 systolic matrix multiplier in Verilog and carried through VLSI design flow with OpenLane with the Skywater 130nm PDK and custom scripts to automate efficient tiling of each systolic processing module.
- Applied low-power physical design techniques including clock/circuit gating, power-aware floorplanning, and optimized placement of MAC units to reduce switching activity and area overhead.