ECE284 FA25 Final Progress Report

Item	Current Status	Status during Poster Presentation	Note
Part1 Vanilla Version	Complete	Complete	Vanilla 8×8 weight-stationary systolic array fully implemented and verified with testbench controller; FPGA synthesis completed with frequency and power reported
Part2 2bit and 4bit Lane Reconfigurable SIMD Systolic Array	Complete	In progress	Lane-reconfigurable SIMD WS array supporting 2-bit and 4-bit activation implemented; 2-bit mode processes 16 output channels via controller-level tiling without modifying datapath.
Part3 Weight-stationary and output stationary reconfigurable PE	Complete	In progress	WS/OS reconfigurable architecture implemented with shared datapath and IFIFO support; OS mode verified using first convolution layer with partial channel and spatial mapping.
Alpha 1 Optimized training for Quantized VGG	Complete	Complete	Optimized quantization-aware training using Adam, label smoothing, and cosine scheduler to improve model accuracy.
Alpha 2 The C2F Pruning Method (Mixed-	Complete	Complete	Mixed-granularity pruning method balancing sparsity

Granularity)			and accuracy while remaining systolic-array friendly.
Alpha 3 Output Stationary Skip Optimization	complete	In progress	Output-stationary gate skipping implemented with fine-grained clock gating at the PE, row, and array levels; functionality validated by comparing testbench outputs against reference results.
Alpha 4 Scalable Multi cores Tiling	In progress	In progress	Multi-core tiling architecture implemented under weight-stationary execution; functional validation is ongoing due to remaining testbench issues.