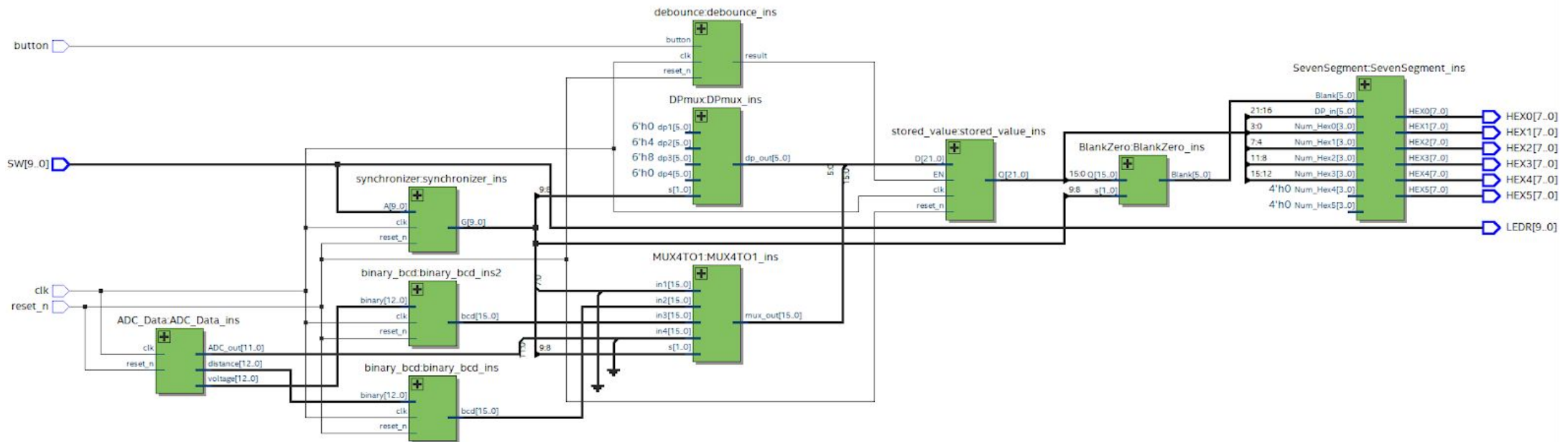



Lab 3 Design Record

Students: Jessica Ritchie, Jade Fjestad, Justin Ross


RTL Schematic











































1200mV 85C Model Fmax Summary

Slow 1200mV 85C Model Fmax Summary				
 <<Filter>>				
	Fmax	Restricted Fmax	Clock Name	Note
1	72.21 MHz	72.21 MHz	clk	
2	119.88 MHz	119.88 MHz	ADC_Data_ins ADC_ins ADC_Conversion_ins u0 altpll_sys sd1 pll7 clk[0]	

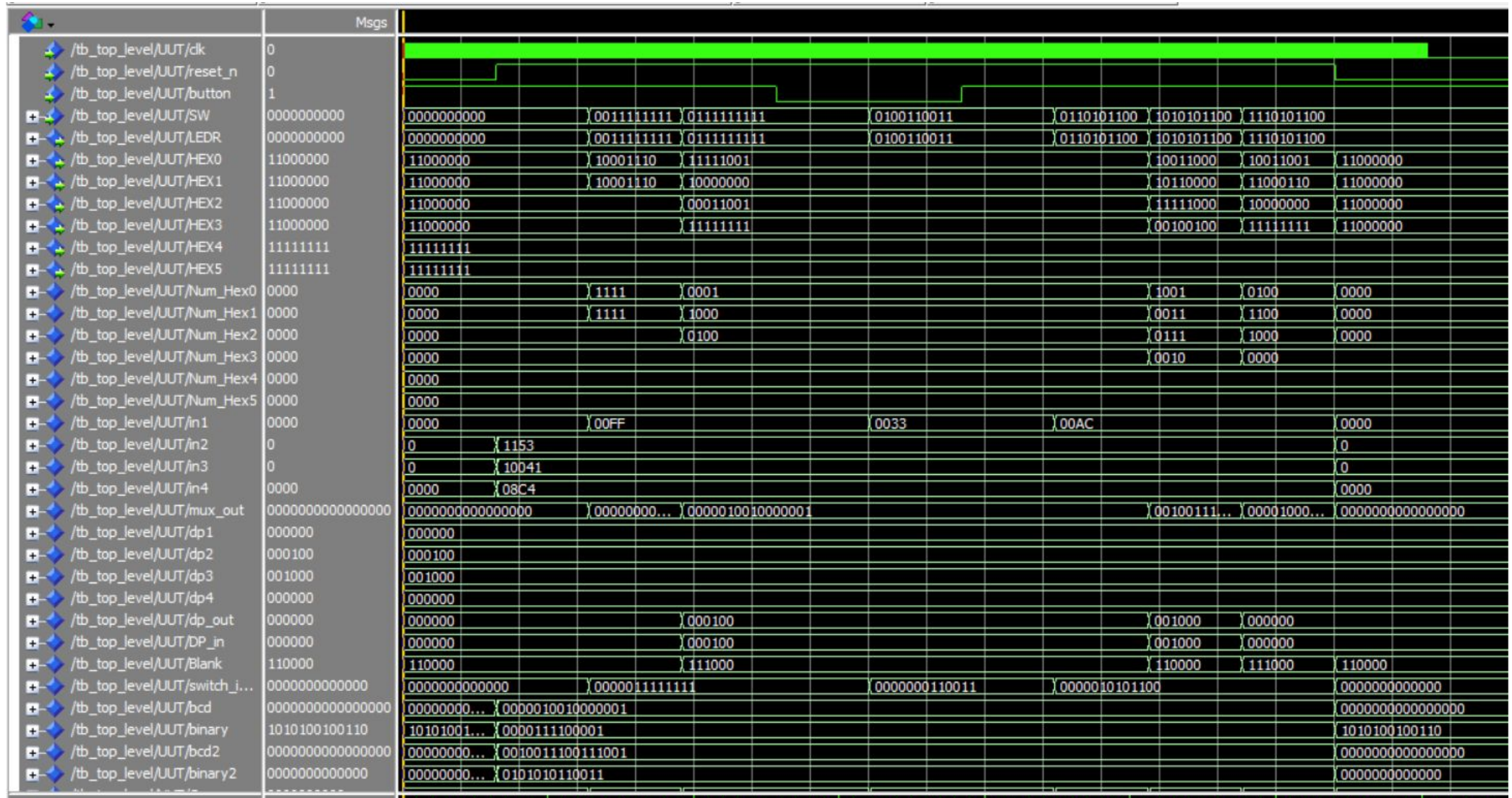
Message Window

Messages 

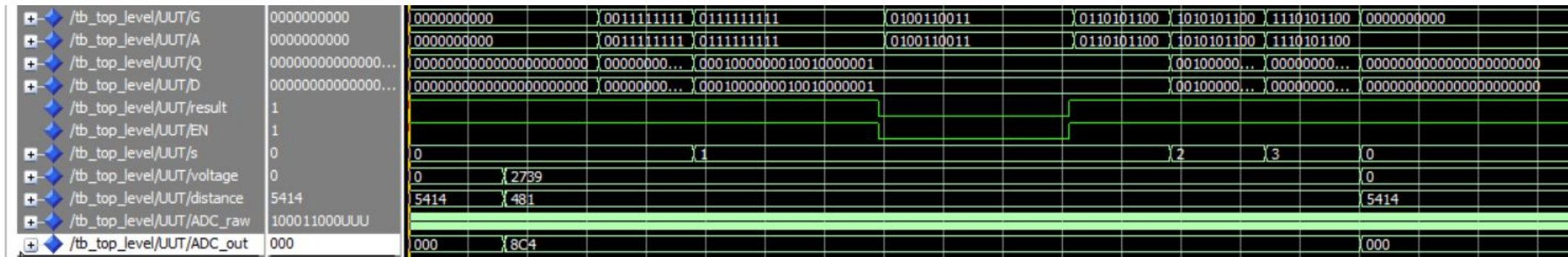
     <<Filter>>  Find...  Find Next

Type	ID	Message
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value
	12019	Can't analyze file -- file tb_MUX2T01.vhd is missing
	12019	Can't analyze file -- file MUX2T01.vhd is missing
	10036	Verilog HDL or VHDL warning at top_level.vhd(30): object "switch_inputs" assigned a value but never read
	10036	Verilog HDL or VHDL warning at top_level.vhd(43): object "ADC_raw" assigned a value but never read
	12125	Using design file adc_conversion.v, which is not specified as a design file for the current project, but contains definitions for 1 design units and 1 entities in project
	10036	Verilog HDL or VHDL warning at adc_conversion.v(98): object "cur_adc_ch" assigned a value but never read
	10036	Verilog HDL or VHDL warning at adc_conversion.v(99): object "adc_sample_data" assigned a value but never read
	10036	Verilog HDL or VHDL warning at altera_modular_adc_control_fsm.v(70): object "sync_ctrl_state_nxt" assigned a value but never read
	14284	Synthesized away the following node(s):
	12241	1 hierarchies have connectivity warnings - see the Connectivity Checks report folder
	13024	Output pins are stuck at VCC or GND
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value
	292013	Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
	15714	Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details
	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
	332049	Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
	332174	Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
	332049	Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
	15705	Ignored locations or region assignments to the following nodes
	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary
	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary
	171167	Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.
	169177	13 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value
	12914	The file, C:/Users/HREL/Documents/GitHub/ENEL-453/Lab 3 working FPGA/adc_qsys.sopcinfo, is not embedded into sof file as expected. Some tools, such as System Console, may not function
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value
	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
	332049	Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
	332174	Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
	332049	Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value

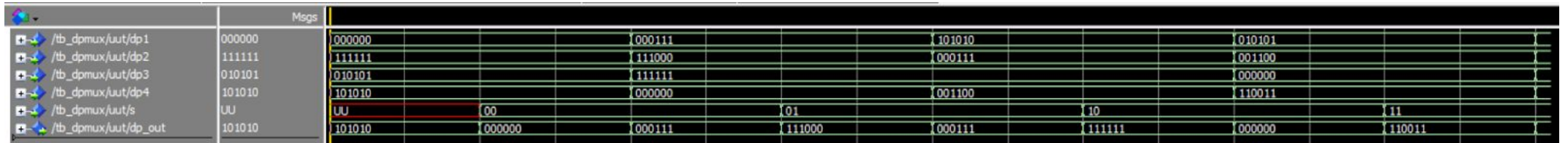
Top level Waveforms (1 of 2)



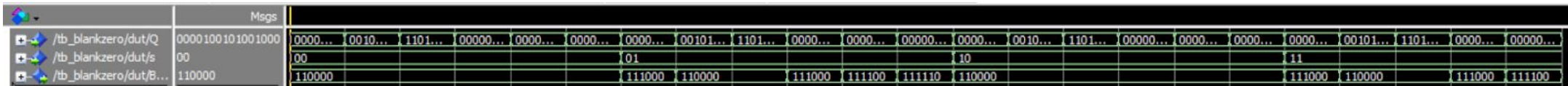
Top level Waveforms (2 of 2)



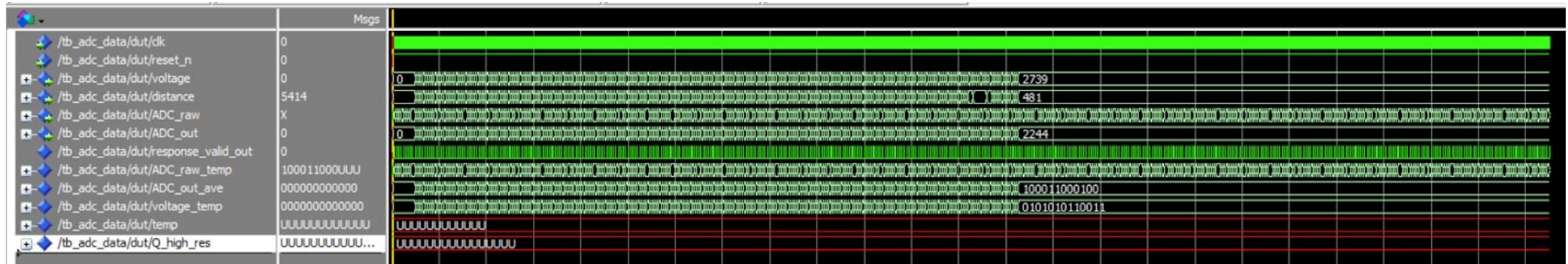
DPmux Waveforms



BlankZero Waveforms

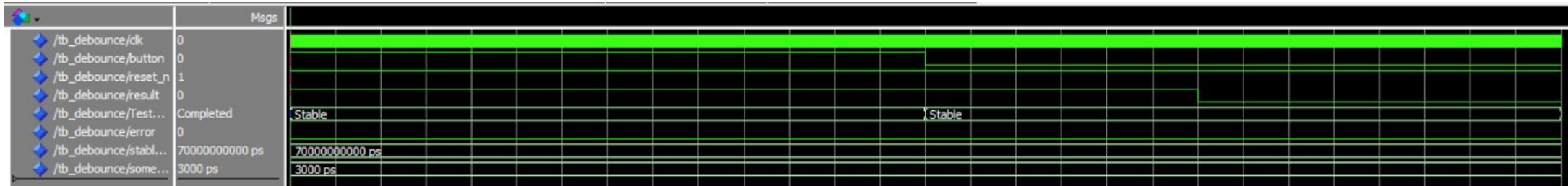


ADC_data Waveforms

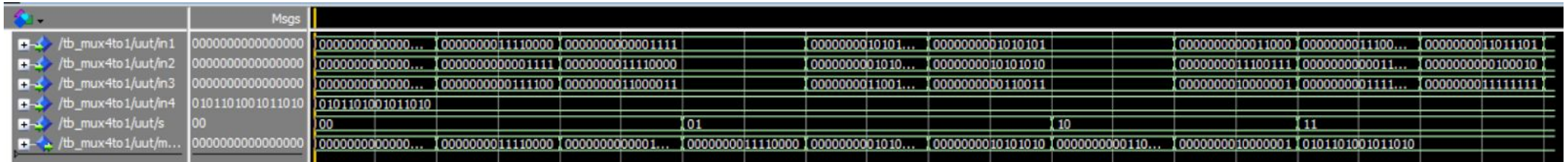


Modules included from Lab 2

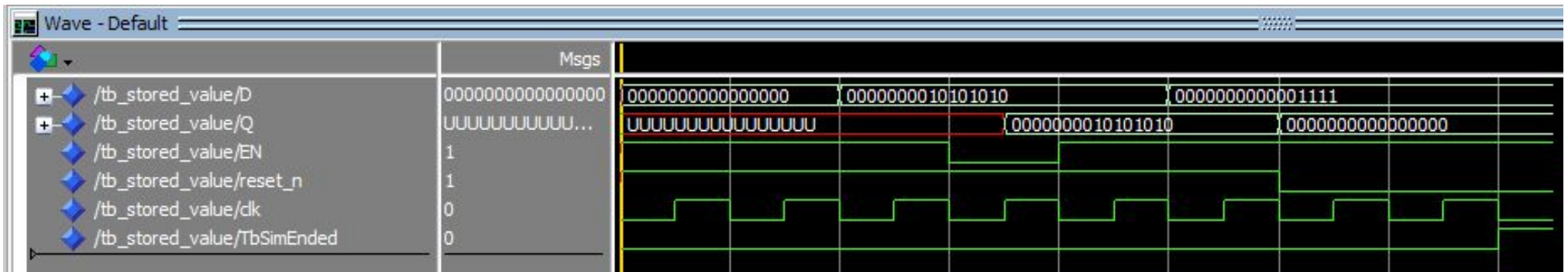
Debounce Waveforms



MUX4To1 Waveforms



Stored_value Waveforms



Synchronizer Waveforms

