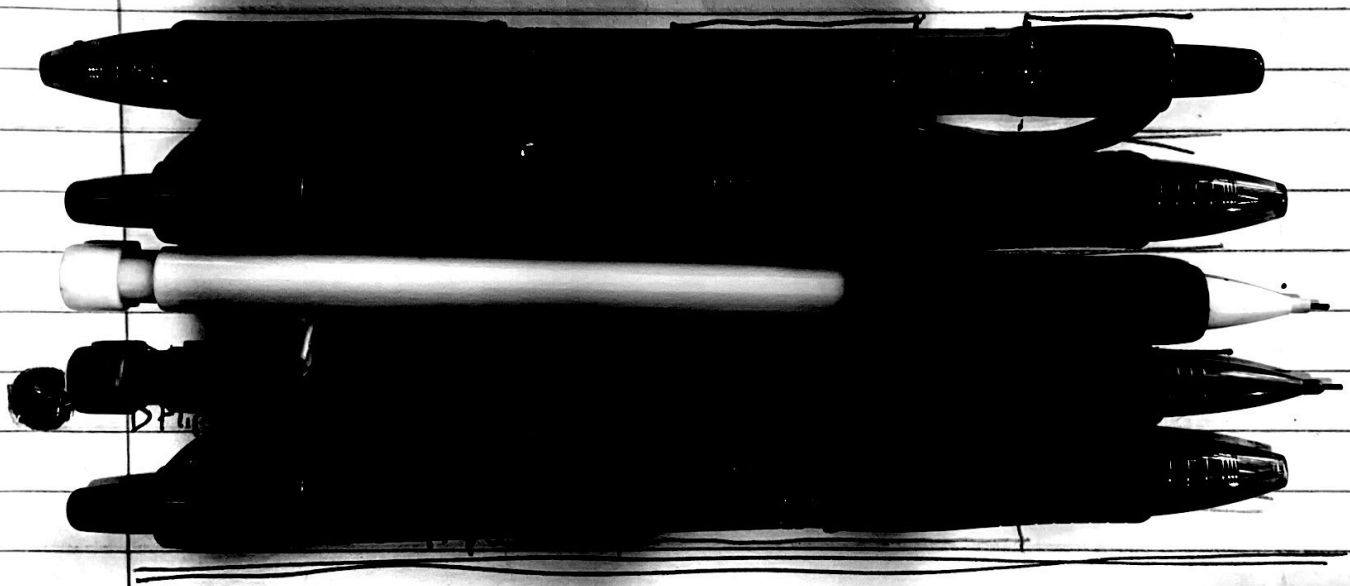
Pre-Lab 9:

2. (a) All useful memory devices have at least two inputs: a data signal, and a timing control signal.

(b) In a D-Latch, the input and output are the same if the timing control is asserted.

In a D-Flip Flop, the input can only be memorized when the timing control is transitioning.



3. (NAND SR-LATCH