ELC 2137 Lab 11: FSM: Guessing Game

Justin Woods

April 22, 2020

Summary

In this lab, a finite state machine(FSM) was created. This required the use of sequential logic, but in a way that does not produce repeating patterns. First, a debounce module was created so that when the Basys3 buttons are pressed, the output does not cycle. Thus, the input is held. Then, a guessing game module was created using the same usage of states, but in a way that produces an output appropriate for a guessing game. These two modules were instantiated in a top level module implemented into the Basys3 board, tested by gameplay.

Questions

1. At what time in the simulation did the de-bounce circuit reach each of the four states

   After 200ns, it would change states. It went from zero to wait1 at 220ns, wait1 to one at 420ns, and one to wait0 at 620ns.

2. Why can this game not be implemented with regular sequential logic?

   We cannot use regular sequential logic because the output is not regular, or repeating. We designed an element that can handle non-repeating conditions by creating several states that the input can but the element in.

3. What type of outputs did you use for your design (Mealy or Moore)? Explain.

   I used Moore outputs in my design. We see this in that the values of the output are synchronized with the clock, updating at the positive edge, and resetting at the negative edge. This way, only the present state of the machine can change the output.

Results

Time (ns):	0-5	5-10	10-15	15-20	20-25	25-30	30-35	35-40	40-45	45-50	50-55	55-60
clk	0	1	0	1	0	1	0	1	0	1	0	1
en	0	0	1	1	0	1	0	0	1	1	1	1
rst	0	1	0	0	0	0	0	0	0	0	0	0
count	X	0	0	1	1	2	2	2	2	3	3	0
tick	X	0	0	0	0	0	0	0	0	1	1	0

Figure 1:

Time (ms):	0-2	2-4	4-6	6-8	8-10	10-12	12-14	14-16	16-18	18-20
data	41	82	103	204	41	82	103	204	41	82
sign	0	0	0	0	0	0	0	0	1	1
hexDec	0	0	0	0	1	1	1	1	1	1
seg	79	24*to*0	40*to*79	79*to*24	40	40	10*to*12	79	40	3f
an	e	e*to*d	d*to*b	b*to*7	7	7*to*e	e*to*d	d*to*b	b	b*to*7
dp	1	1	1	1	1	1	1	1	1	1

Figure 2:

Figure 3:

Figure 4:

Code

Listing 1: guessFSM

Listing 2: guessFSM Test

Listing 3: Sseg4TDM Source Code

Listing 4: Sseg4TDM Test

Listing 5: CalcLab10