Lab 1 Report

ECE 124

Group 17 Session 204

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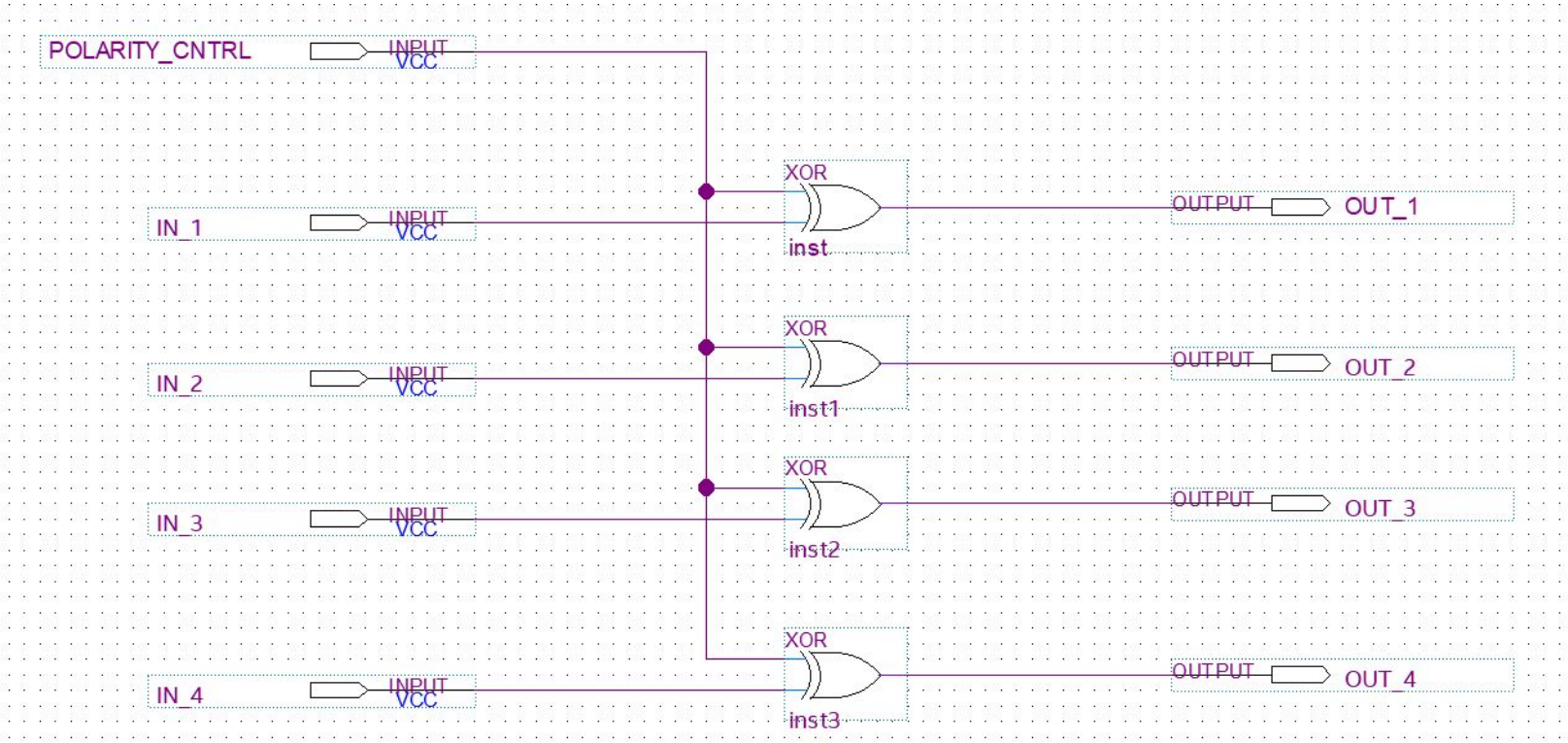
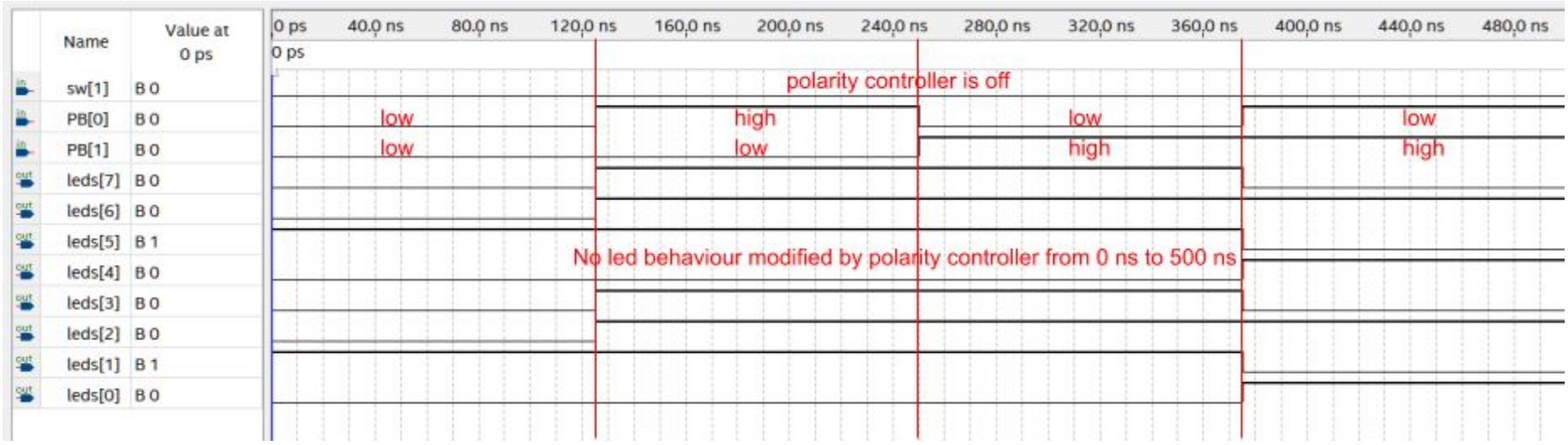
Screenshot of VHDL Polarity Control

```
 1   -- Author: Group 17, Justin Aujla, Yuhao Chen
 2   LIBRARY ieee;
 3   USE ieee.std_logic_1164.all;
 4   LIBRARY work;
 5
 6   ENTITY VHDL_polarity_ctrl IS
 7      PORT(
 8         POLARITY_CNTRL, IN_1, IN_2, IN_3, IN_4 : IN STD_LOGIC;
 9         OUT_1, OUT_2, OUT_3, OUT_4 : OUT STD_LOGIC
10      );
11   END VHDL_polarity_ctrl;
12
13   ARCHITECTURE dataflow OF VHDL_polarity_ctrl IS
14   BEGIN
15   OUT_1 <= POLARITY_CNTRL XOR IN_1;
16   OUT_2 <= POLARITY_CNTRL XOR IN_2;
17   OUT_3 <= POLARITY_CNTRL XOR IN_3;
18   OUT_4 <= POLARITY_CNTRL XOR IN_4;
19   END dataflow;
```

Screenshot of Schematic Polarity Control



Simulation with Annotation (sw[1] set to low)



Simulation with Annotation (sw[1] set to high)