Lab 3 Report

ECE 124

Group 17 Session 204

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4-bit Comparator Truth Table

Comparison Inputs from 1-Bit Comparators												4-Bit Comparator Outputs		
A3<B3	A3=B3	A3>B3	A2<B2	A2=B2	A2>B2	A1<B1	A1=B1	A1>B1	A0<B0	A0=B0	A0>B0	A<B	A=B	A>B
0	0	1	X	X	X	X	X	X	X	X	X	0	0	1
1	0	0	X	X	X	X	X	X	X	X	X	1	0	0
0	1	0	0	0	1	X	X	X	X	X	X	0	0	1
0	1	0	1	0	0	X	X	X	X	X	X	1	0	0
0	1	0	0	1	0	0	0	1	X	X	X	0	0	1
0	1	0	0	1	0	1	0	0	X	X	X	1	0	0
0	1	0	0	1	0	0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	0	1	0	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0	0	1	0	0	1	0

Top-level Design

```
1   -- Group 17: Yuhao Chen & Gurvijaypal Aujla
2   library ieee;
3   use ieee.std_logic_1164.all;
4
5
6   entity LogicalStep_Lab3_top is port (
7       clk_in      : in  std_logic;
8       pb          : in  std_logic_vector(3 downto 0);
9       sw          : in  std_logic_vector(7 downto 0);
10      leds        : out std_logic_vector(11 downto 0)
11
12  );
13  end LogicalStep_Lab3_top;
14
15  architecture design of LogicalStep_Lab3_top is
16
17  --
18  -- Provided Project Components Used
19  ------------------------------------------------------------------
20
21  component Tester port (
22      MC_TESTMODE             : in  std_logic;
23      I1EQI2,I1GTI2,I1LTI2 : in  std_logic;
24      input1                  : in  std_logic_vector(3 downto 0);
25      input2                  : in  std_logic_vector(3 downto 0);
26      TEST_PASS               : out std_logic
27  );
28  end component;
29
30  component HVAC port (
31      clk                     : in std_logic;
32      run_n                   : in std_logic;
33      increase, decrease      : in std_logic;
34      temp                    : out std_logic_vector (3 downto 0)
35  );
36  end component;
37
38  ------------------------------------------------------------------
39  -- Add Other Components here
40  component Compx4 port (
41      compx4_a, compx4_b: in std_logic_vector(3 downto 0);
42      compx4_lt, compx4_eq, compx4_gt : out std_logic
43  );
44  end component;
45
46  component EMAC port (
47      pb                          : in std_logic_vector(3 downto 0);
```

Top-level Design Continued

```
component EMAC port (
    pb                          : in std_logic_vector(3 downto 0);
    lt, eq, gt                  : in std_logic;
    leds                        : out std_logic_vector(5 downto 0);
    vacOn                       : out std_logic;
    increase, decrease, run_n : out std_logic
);
end component;

component Mux port (
    hex_num1, hex_num0 : in std_logic_vector(3 downto 0);
    mux_select         : in std_logic;
    hex_out            : out std_logic_vector(3 downto 0)
);
end component;


-----------------------------------------------------------------
-- Create any signals to be used
signal current_temp, mux_temp               : std_logic_vector(3 downto 0);  -- current_temp: stores 4-bit value of the current_temp
signal increase, decrease, run_n, lt, eq, gt : std_logic;                    -- mux_temp: stores 4-bit value of either desired_temp or vacation_temp, dependent on vacation_temp_mode input
                                                                             -- increase, decrease, run_n: stores the output of EMAC for input in HVAC, dependent on 4-bit comparator
                                                                             -- lt, eq, gt: stores the output of 4-bit comparator; 4-bit A < 4-bit B, 4-bit A == 4-bit B, 4-bit A > 4-bit B respectively
-----------------------------------------------------------------

-- Here the circuit begins

begin

-- 4-bit 2-1 mux for selecting desired_temp or vacation_temp

inst1: Mux port map (
    sw(7 downto 4), sw(3 downto 0),
    pb(3),
    mux_temp
);
-- HVAC component controlling current_temp
inst2: HVAC port map (
    clk_in,
    run_n,
    increase, decrease,
    current_temp(3 downto 0)
);

-- 4-bit comparator. Compare the value of the current_temp and the output of the 4-bit 2-1 mux
inst3: Compx4 port map (
    mux_temp(3 downto 0), current_temp(3 downto 0),
    lt, eq, gt
);

-- Tester component controlling MAG_test led
inst4: Tester port map (
    pb(2),
    eq, gt, lt,
    sw(3 downto 0),
    current_temp(3 downto 0),
    leds(6)
);

-- Energy Monitor and Control (EMAC) logic component
inst5: EMAC port map (
    pb(3 downto 0),
    lt, eq, gt,
    leds(5 downto 0),
    leds(7),
    increase, decrease, run_n
);

-- Assign the current_temp value to leds[11] to leds[8]
leds(11 downto 8) <= current_temp(3 downto 0);


end design;

```

4-bit 2 to 1 Multiplexer Design

```
1   -- Group 17: Yuhao Chen & Gurvijaypal Aujla
2   library ieee;
3   use ieee.std_logic_1164.all;
4
5   entity Mux is port (
6       hex_num1, hex_num0 : in std_logic_vector(3 downto 0);
7       mux_select         : in std_logic;
8       hex_out            : out std_logic_vector(3 downto 0)
9   );
10  end Mux;
11
12  architecture mux_logic of Mux is
13  |
14  --
15  -- Provided Project Components Used
16  ------------------------------------------------------------------------
17  |
18  ------------------------------------------------------------------------
19  -- Add Other Components here
20  |
21  ------------------------------------------------------------------------
22  -- Create any signals to be used
23  ------------------------------------------------------------------------
24  |
25  -- Here the circuit begins
26
27  begin
28  |
29  with mux_select select
30  hex_out <= hex_num0 when '0',
31             hex_num1 when '1';
32  |
33  end mux_logic;
34
```

1-bit Comparator Design

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity Compx1 is port (
    compx1_a, compx1_b              : in std_logic;
    compx1_lt, compx1_eq, compx1_gt  : out std_logic
);
end Compx1;

architecture dataflow of Compx1 is

--
-- Provided Project Components Used
------------------------------------------------------------------

------------------------------------------------------------------
-- Add Other Components here

------------------------------------------------------------------
-- Create any signals to be used
------------------------------------------------------------------


-- Here the circuit begins

begin

compx1_lt <= (not compx1_a) and compx1_b; -- A < B; 1-bit A < 1-bit B
compx1_eq <= not (compx1_a xor compx1_b); -- A == B; 1-bit A == 1-bit B
compx1_gt <= compx1_a and (not compx1_b); -- A > B; 1-bit A > 1-bit B

end dataflow;
```

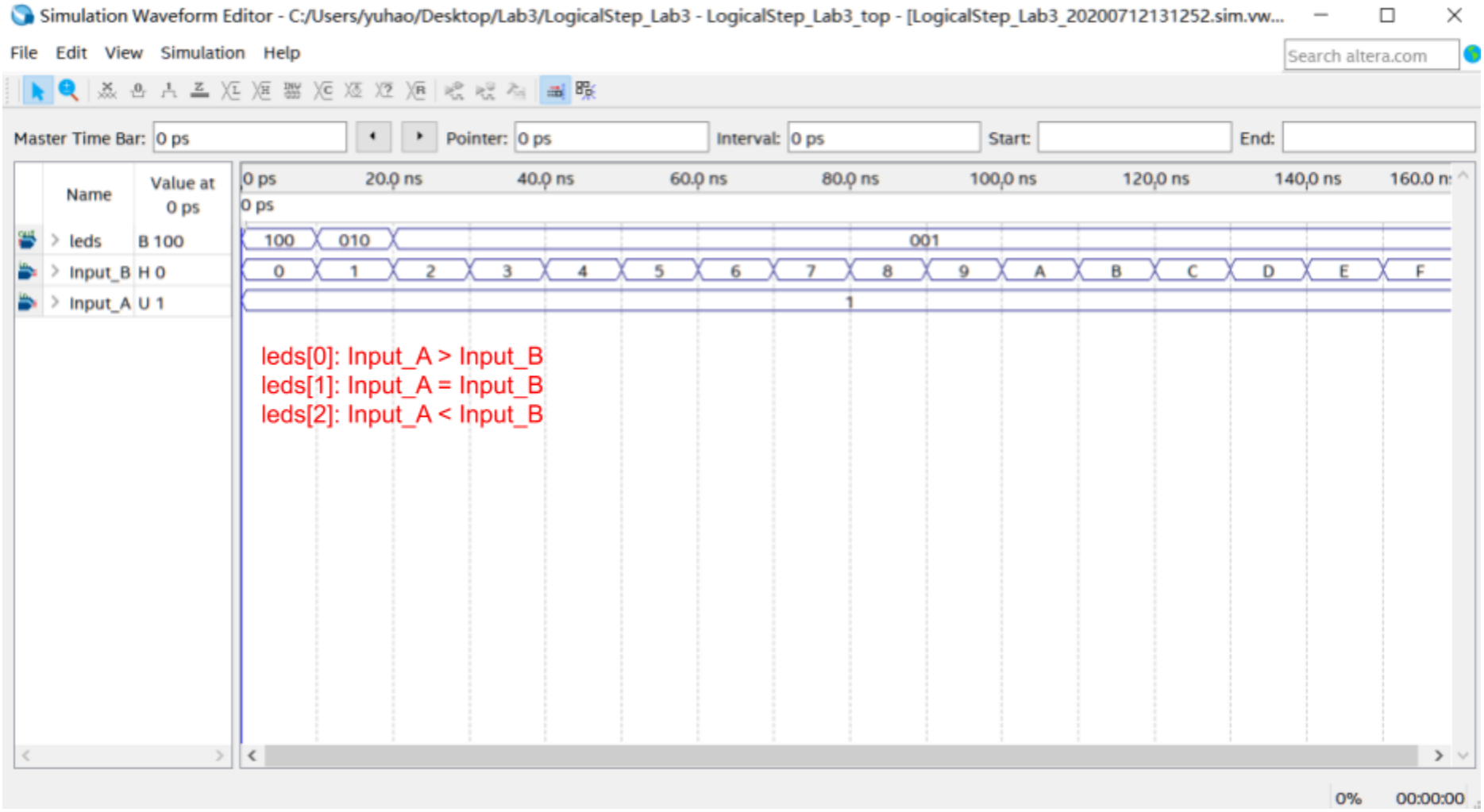
4-bit Comparator Design

```vhdl
-- Group 17: Yuhao Chen & Gurvijaypal Aujla
library ieee;
use ieee.std_logic_1164.all;

entity Compx4 is port (
    compx4_a, compx4_b              : in std_logic_vector(3 downto 0);
    compx4_lt, compx4_eq, compx4_gt  : out std_logic
);
end Compx4;

architecture dataflow of Compx4 is


-- Provided Project Components Used
------------------------------------------------------------------
------------------------------------------------------------------
-- Add Other Components here

component Compx1
    port (
        compx1_a, compx1_b              : in std_logic;
        compx1_lt, compx1_eq, compx1_gt  : out std_logic
    );
end component;

------------------------------------------------------------------
-- Create any signals to be used
signal res_gt, res_eq, res_lt : std_logic_vector(3 downto 0);  -- res_gt, res_eq, res_lt: signal used to store the values of each bit comparison for each of the 4 1-bit comparators
                                                               -- each 1-bit comparator will store their outputs to each (A > B), (A == B), and (A < B) vector for later use
------------------------------------------------------------------

-- Here the circuit begins

begin

-- 1-bit comparator for 1st bit of each 4-bit input
inst1: Compx1 port map (
    compx4_a(3), compx4_b(3),
    res_lt(3), res_eq(3), res_gt(3)
);

-- 1-bit comparator for 2nd bit of each 4-bit input
inst2: Compx1 port map (
    compx4_a(2), compx4_b(2),
    res_lt(2), res_eq(2), res_gt(2)
);

-- 1-bit comparator for 3rd bit of each 4-bit input
inst3: Compx1 port map (
    compx4_a(1), compx4_b(1),
    res_lt(1), res_eq(1), res_gt(1)
);

-- 1-bit comparator for 4th bit of each 4-bit input
inst4: Compx1 port map (
    compx4_a(0), compx4_b(0),
    res_lt(0), res_eq(0), res_gt(0)
);

compx4_lt <= res_lt(3) or (res_eq(3) and res_lt(2)) or (res_eq(3) and res_eq(2) and res_lt(1)) or (res_eq(3) and res_eq(2) and res_eq(1) and res_lt(0)); -- A < B; 4-bit A < 4-bit B
compx4_eq <= res_eq(3) and res_eq(2) and res_eq(1) and res_eq(0);                                                                                    -- A == B; 4-bit A == 4-bit B
compx4_gt <= res_gt(3) or (res_eq(3) and res_gt(2)) or (res_eq(3) and res_eq(2) and res_gt(1)) or (res_eq(3) and res_eq(2) and res_eq(1) and res_gt(0)); -- A > B; 4-bit A > 4-bit B

end dataflow;
```

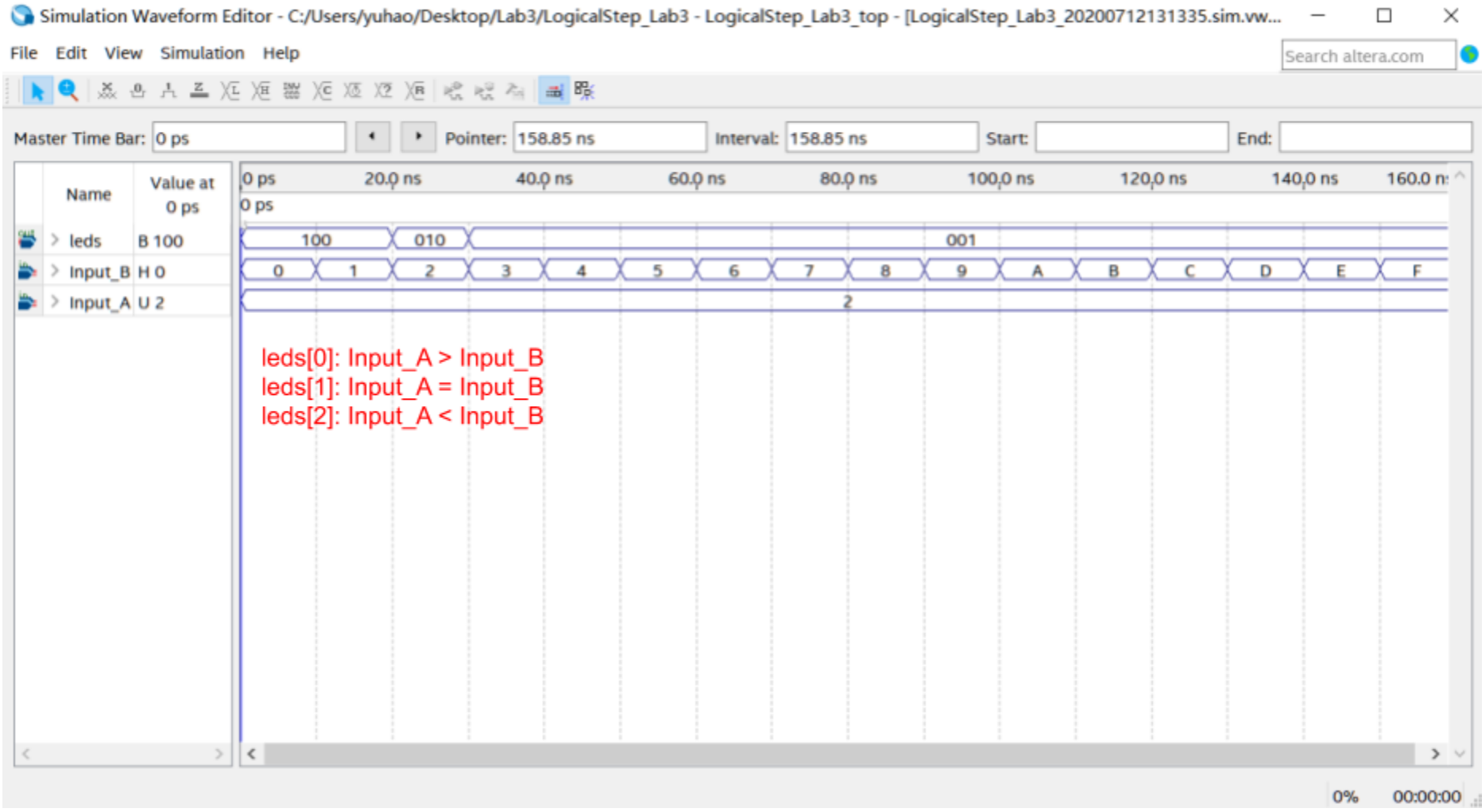
Energy Monitor and Control Logic Design

```
1   -- Group 17: Yuhao Chen & Gurvijaypal Aujla
2   library ieee;
3   use ieee.std_logic_1164.all;
4
5
6   entity EMAC is port (
7       pb                      : in std_logic_vector(3 downto 0);
8       lt, eq, gt              : in std_logic;
9       leds                    : out std_logic_vector(5 downto 0);
10      vacOn                   : out std_logic;
11      increase, decrease, run_n : out std_logic
12  );
13  end EMAC;
14
15  architecture design of EMAC is
16
17  --
18  -- Provided Project Components Used
19  ------------------------------------------------------------------
20
21  ------------------------------------------------------------------
22  -- Add Other Components here
23
24  ------------------------------------------------------------------
25  -- Create any signals to be used
26  ------------------------------------------------------------+-----
27
28
29  -- Here the circuit begins
30
31  begin
32
33  increase <= gt;                                         -- mux_temp > current_temp ==> increase
34  decrease <= lt;                                         -- mux_temp < current_temp ==> decrease
35  run_n <= pb(2) or pb(1) or pb(0);                       -- run_n set to off (according to HVAC requirements) when MC_test_mode, door_open, or window_open are enabled
36  leds(2) <= lt;                                          -- when mux_temp < current_temp, ac is on
37  leds(0) <= gt;                                          -- when mux_temp > current_temp, furnace is on
38  leds(1) <= eq;                                          -- when mux_temp == current_temp, are at right temp
39  leds(3) <= (not eq) and (not (pb(2) or pb(1) or pb (0)));   -- when mux_temp /= current_temp, and mc_test_mode, window_open, or door_open are not on, blower is on
40  leds(5) <= pb(0);                                       -- when door_open is on, door_open_led is on
41  leds(4) <= pb(1);                                       -- when window_open is on, window_open_led is on
42  vacOn <= pb(3);                                         -- when vacation_mode is on, Vacation_mode_led is on
43
44  end design;
45
```

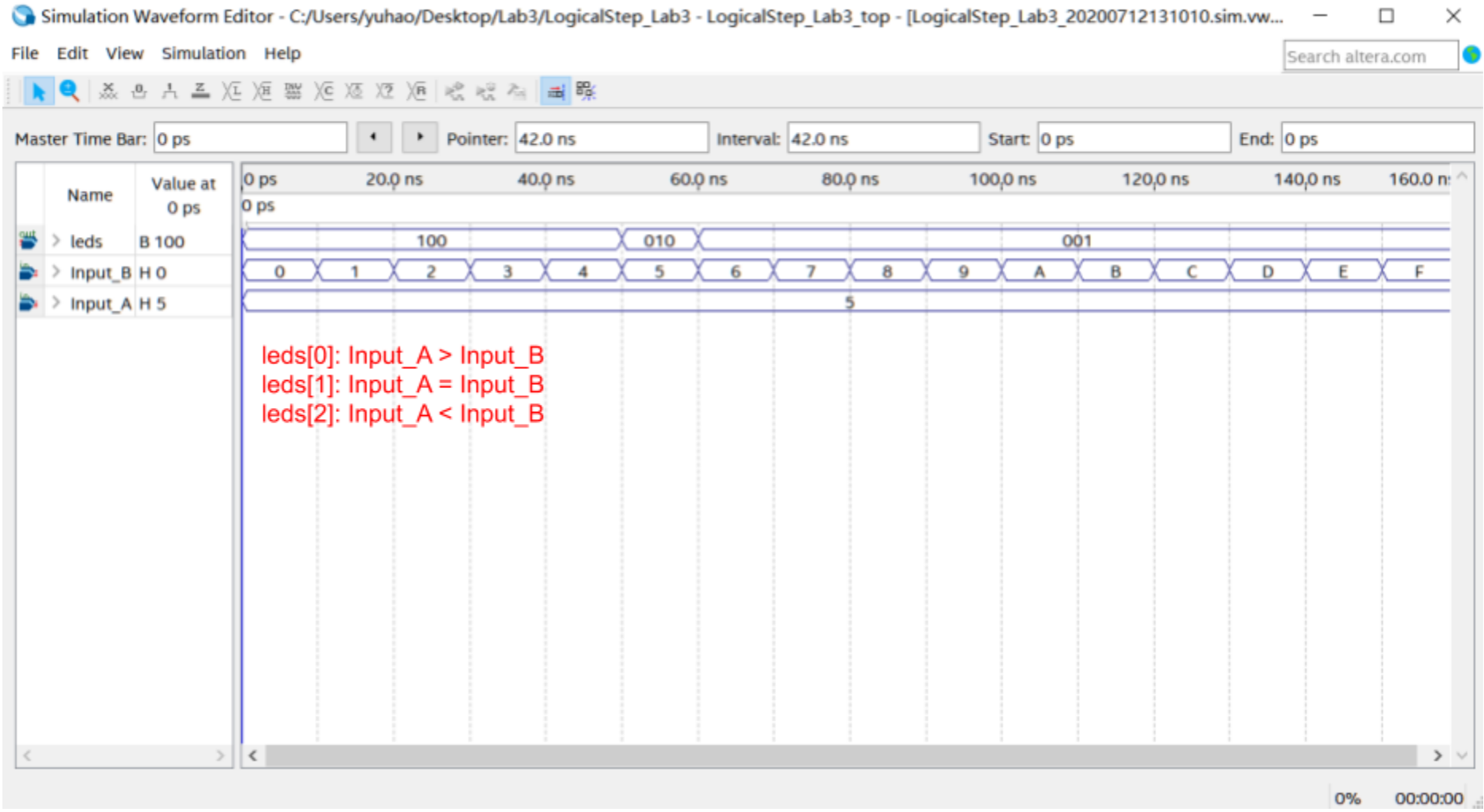
Functional Simulation 1 of the 4-bit Comparator (PART A): Input_A = 1



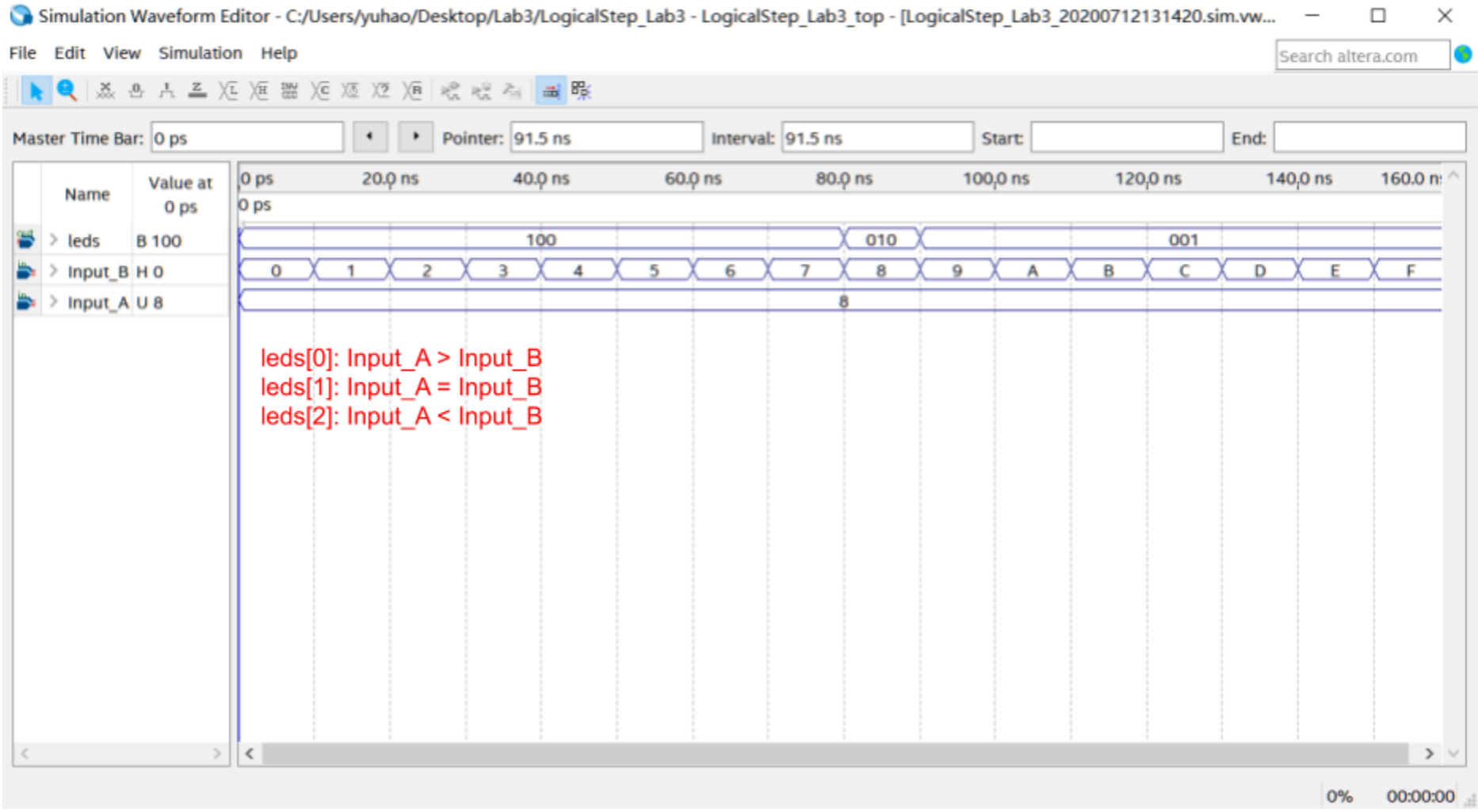
Functional Simulation 2 of the 4-bit Comparator (PART A): Input_A = 2



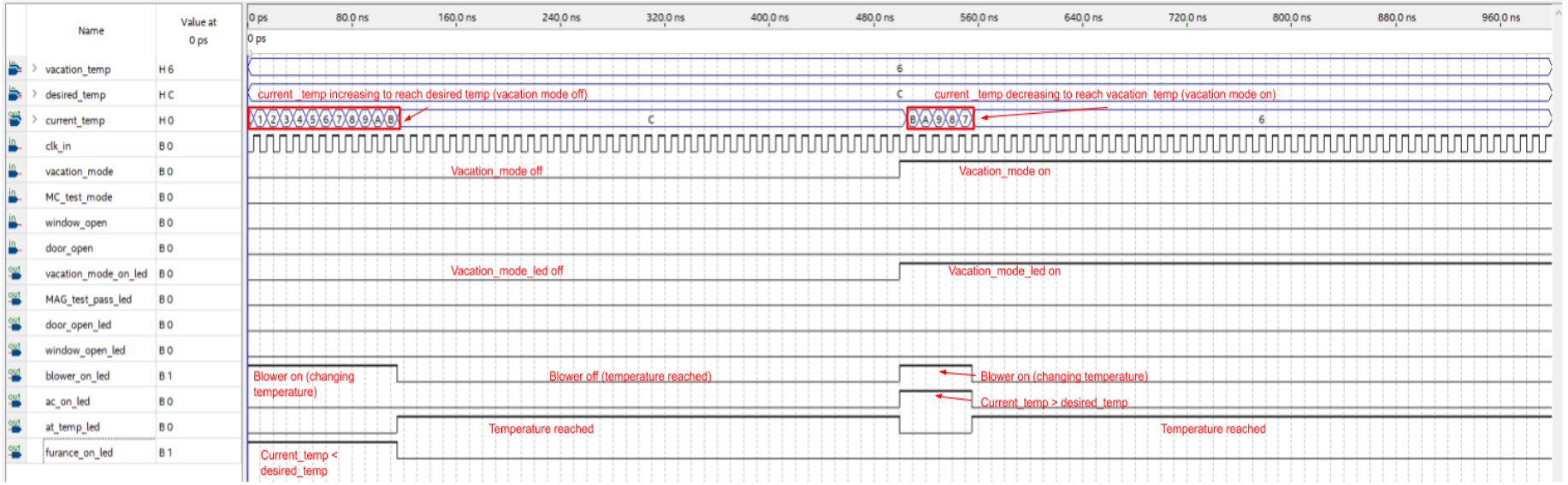
Functional Simulation 3 of the 4-bit Comparator (PART A): Input_A = 5



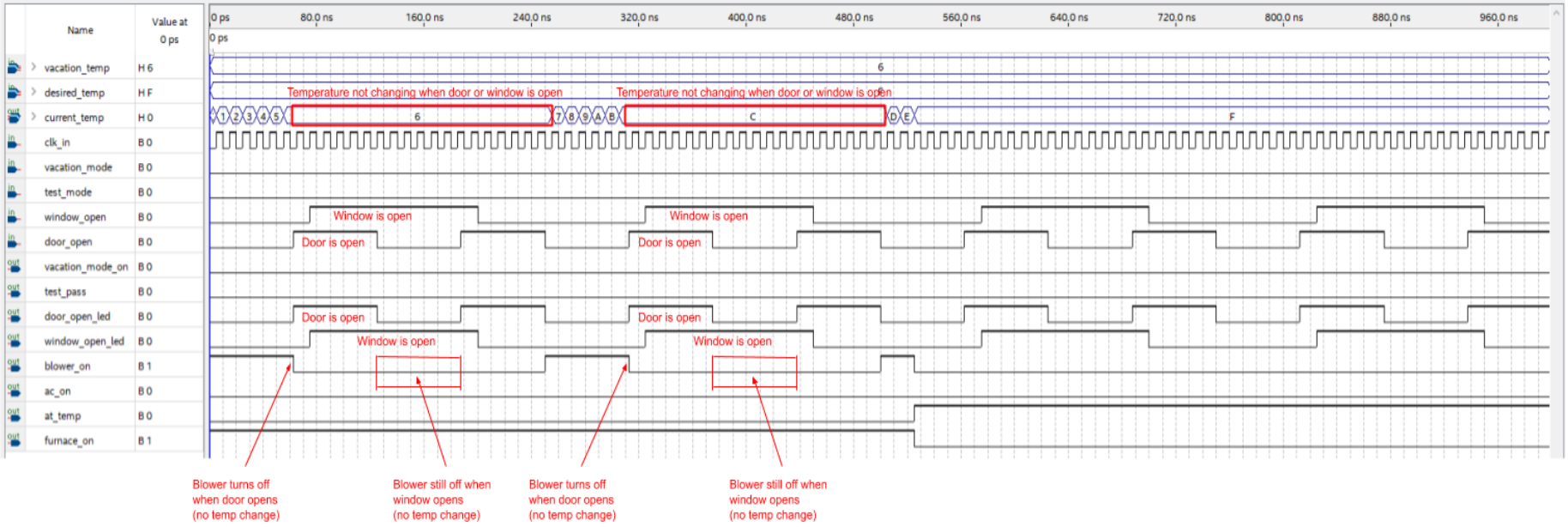
Functional Simulation 4 of the 4-bit Comparator (PART A): Input_A = 8



Functional Simulation 1 of the Energy Monitor (PART B): HVAC Control Waveform



Functional Simulation 2 of the Energy Monitor (PART B): SENSOR Operations Waveform



Functional Simulation 3 of the Energy Monitor (PART B): Tester Operations Waveform