

# SENIOR DESIGN PROJECT REPORT

## EE 4097 – Spring 2020

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**Project title:** Discord of DAQ Dissection

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# 1 Introduction

## 1.1 Executive Summary

A DAQ system will be designed in simulation using TI TINA to read analog and digital voltage signals and display them on a computer through LABVIEW software. The DAQ system will operate on a large range of voltages from -50 V to 50 V with frequencies up to 1 MHz. The system was divided into the analog section and the digital section. The analog section will condition the input signals to manageable levels and be able to perform mathematical operations on the input analog signals. The analog section will also condition the signals to be read by the digital section. The digital section included a microcontroller that read the signals from the analog section and outputted the data on a display using LABVIEW.

The analog section was simulated using TI TINA. The DAQ system will have four analog input channels and four digital input channels and can display two input channels and one mathematical operation. Each of the analog inputs had three different volts per division ratio by dividing the input voltage by 5, 10, or 20. The system was designed in simulation as multiple circuit files. The outputs of one circuit file were exported and used as inputs for the next circuit file in the system. The exported data was formatted using a macro in Microsoft Excel to a readable format by TI TINA. The conditioned output of the analog system was then exported as a CSV to be read by the digital section of the system.

The digital section was implemented using LABVIEW software. LABVIEW was used to read the CSV data from the analog section and display it on an HMI screen. The display will allow the operator to view the different channel signals and the math operation in the analog system to allow for a greater understanding of the DAQ system operation.

The system was designed by three electrical engineering students Jesse Dengel, Justin Chau, and Matt Mutarelli. The DAQ system was designed to be a cheaper alternative to measure a large range of analog voltage levels over a large bandwidth. The DAQ system was also designed to perform mathematical operations on the input signals digitally and through analog circuits.

## 1.2 Background and Problem Statement

DAQ systems are expensive devices that are difficult to maintain due to the enclosed structure of the device. A powerful DAQ system can cost hundreds of dollars to replace. Operators have a difficult time understanding DAQ systems because it is difficult to observe the internal workings of the system. The project was designed to solve these problems by creating an open, low-cost system that allowed the operator to observe the internal operation of the system.

### 1.2.1 Existing Works

There are many existing DAQ systems produced by multiple different companies. The proposed DAQ system was compared to three existing DAQ systems by three different companies.

- DATAQ DI 1110 Low-cost USB Data Acquisition (DAQ) System [1].
  - **Voltage Range:**  $\pm 100$  V
  - Analog Ports: 8
  - Digital Ports: 7
  - Sampling Rate: 160 kHz
  - Analog to Digital Resolution: 12 Bits
  - Cost: \$89.99

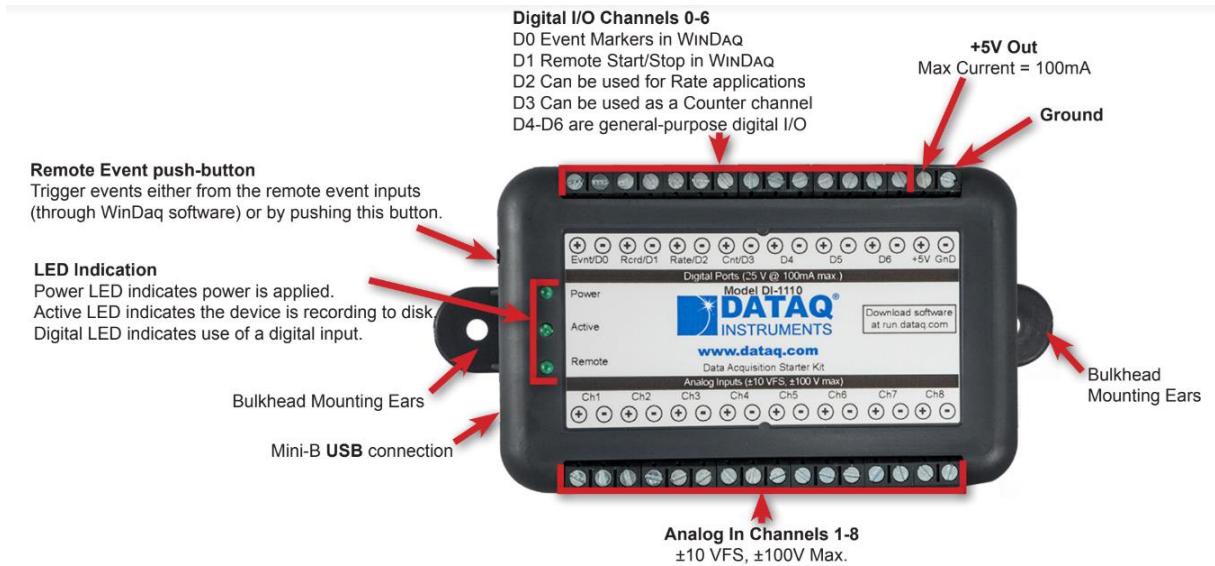


Figure 1. DATAQ 1110 USB DAQ System Layout

- MC USB-1608FS-Plus [2]
  - **Voltage Range:**  $\pm 10$  V
  - Analog Ports: 8
  - More Digital Ports: 8
  - Sampling Rate: 100 kHz
  - Analog to Digital Resolution: 16 Bits
  - Cost: \$440.00



Figure 2. MC USB 1608 FS-Plus DAQ System Layout

- NI 9381[3]
  - Voltage Range: 0 to 5V
  - Analog Ports: 8
  - Digital Ports: 4
  - Analog Sampling Rate: 20 kHz
  - Analog to Digital Resolution: 12 Bits
  - Cost: \$457.00



Figure 3. NI 9381 DAQ System Layout

The observed existing DAQ systems had eight analog input ports which was twice as the four analog input ports in the proposed system. Existing DAQ systems also had four or more digital input ports which was equal to or greater than the four digital input ports on the proposed system. Overall the existing DAQ systems can measure more inputs at a time than the proposed system. The advantage of the proposed DAQ system was the wide range of input analog signals. The proposed system was able to have input voltages between -50V to 50V which was larger than most of the existing DAQ systems except the DATAQ DI 1110. The proposed system was also planned to operate on signal frequencies up to 1 MHz, which was much larger than the input frequency range of the existing systems. An analog to digital resolution of twelve bits used in the proposed system was the same as most existing DAQ systems.

### **1.2.2 Global and Societal Context and Motivation**

- The analog section of the DAQ system was broken into many smaller simulation files. Operators of the simulation system can see the data at the different stages in the DAQ by observing the output of the different simulation files. The smaller simulation files were easier to understand than analyzing the entire system at once.
- The project created a cheap and simple DAQ system that can be used on a wide range of signal voltage levels and frequencies using simple circuits. The project will also act as a tool to understand DAQ design and operation so that future DAQ systems can be designed and maintained.



## 2 Design and Methods

The DAQ system was designed to measure analog voltages that ranged from  $\pm 50V$  with a frequency up to  $1\text{ MHz}$  accurately with no phase shift. The analog voltages were transformed to lower voltage levels that were manageable by the  $\pm 12V$  DAQ system. The system then performed mathematical operations on the signal. The different math operations that the system performed were addition, subtraction, integration, and differentiation. The system also allowed the signals to pass through without performing any operation or inverted the signal. The analog system then transformed the signal into a signal that can be read by the microcontroller analog-to-digital converter (ADC). The ADC of the microcontroller was able to read positive voltages up to  $+2V$ .

The original analog voltage range was  $\pm 100V$ , but was reduced to prevent the input voltage from exceeding the system voltage. The lowest voltage division divided the input analog voltage by 5. If a  $100V$  signal was used with the lowest voltage division, the system will experience a voltage of  $20V$ . The voltage was larger than the supply voltage which will cause the system to not work properly and may damage the system. One proposed solution was to increase the supply voltage, but the linear power supply was already purchased and provided  $\pm 12V$ . The input range was reduced to  $50V$  so that at the lowest division, the system will experience a voltage of  $10V$  which was less than the supply voltage.

The original system was also planned to have an equalizer function to increase the magnitude of signal in different frequency bands. The graphic equalizer was to be implemented using ten fifth order bandpass filters for ten different frequency bands from  $0\text{ Hz}$  to  $1\text{ MHz}$ . The equalizer was unable to be included in the design due to time constraints. The created system included an inversion operation which was not part of the original design to make up for the equalizer function.

The original system included a  $\pm 12V$  power system with taps for  $0.85V$ ,  $2.0V$ ,  $3.3V$ , and  $5V$  DC voltage. The  $\pm 12V$  power system was updated need tap voltages at  $1.65V$ ,  $3.3V$ , and  $-5V$ . The power system was simplified by improving the microcontroller conditioning circuit. The  $1.65V$  and  $3.3V$  taps were used for digital inputs and the  $-5V$  tap was used for conditioning the signals for the microcontroller.

### 2.1 Goals

#### 2.1.1 Goal 1: Power Supply System

##### 1) Task 2.1: Design a Power Supply System with Necessary Taps

**Description:** The DAQ system was designed using a  $\pm 12V$  power supply system and used tap voltages at  $1.65V$ ,  $3.3V$ , and  $-5V$ .

**Challenges:** A linear power supply provided a smoother reference than a switch mode power supply but was difficult to design, so a  $\pm 12V$  power supply was purchased. The tap voltages were created using a voltage divider between two resistors, which needed to be precise to obtain the correct tap voltage. Zener diodes can also be used to generate the tap voltages.

#### 2.1.2 Goal 2: Analog Input Signal Conditioning

##### 1) Task 2.1: Voltage Divider Transformation

**Description:** Design a voltage divider system that will transform the input analog voltage from  $\pm 50\text{ V}$  to  $\pm 2.5\text{V}$ . Include voltage divisions that divided the input analog voltage by 5, 10, and 20.

**Challenges:** The resistance of the voltage divider will act as the input resistance of the probe. The resistance of the voltage divider must be as large as possible to act as an effective probe. The end of the voltage divider will be grounded, so the probe was unable to be used as a differential probe.

## 2) Task 2.2: Anti-Aliasing Filter

**Description:** A third order low pass filter was designed to limit the input signal frequency to  $1\text{ MHz}$ . The anti-aliasing filter attenuated all frequencies above the maximum frequency.

**Challenges:** The cut off frequency of the anti-aliasing filter was set to be much higher than the maximum frequency of  $1\text{ MHz}$  to ensure that no attenuation was experienced. The increased range was also to ensure that the phase of the input signal was not shifted. It was imperative to maintain phase for the integration and differentiation operations.

### 2.1.3 Goal 3: Analog Signal Operations

#### 1) Task 3.1: Analog Pass and Invert Operations

**Description:** A buffer and inverting buffer were designed to allow signals to pass through with and without inversion over the range of  $0\text{ Hz}$  to  $1\text{MHz}$  that were limited to  $\pm 2.5\text{V}$ .

**Challenges:** The operational amplifiers used to create the buffers must be able to operate at high frequencies up to  $1\text{MHz}$ . The inverting buffer must have a gain of one, so precision resistors must be used.

#### 2) Task 3.2: Analog Summation Operation

**Description:** An inverting summation amplifier was designed using operational amplifiers to sum two signals over the range of  $0\text{ Hz}$  to  $1\text{MHz}$  that were limited to  $\pm 2.5\text{V}$ .

**Challenges:** The inverting summation amplifier must be able to sum signals over a large frequency range, so commercial operational amplifiers with a large bandwidth were used. The summation amplifier must also provide a gain of unity, so the value of the resistors used must be precise.

#### 3) Task 3.3: Analog Subtraction Operation

**Description:** A difference amplifier was designed using operational amplifiers to subtract two signals over the range of  $0\text{ Hz}$  to  $1\text{MHz}$  that were limited to  $\pm 2.5\text{V}$ .

**Challenges:** The difference amplifier must be able to subtract signals over a large frequency range, so commercial operational amplifiers with a large bandwidth were used. The summation amplifier must also provide a gain of unity, so the value of the resistors used must be precise. The inputs to the subtraction operation were inverted so that the difference was the inverse of the desired difference to be consistent with the other inverting operations.

#### 4) Task 3.4: Analog Integration Operation

**Description:** An integration equalizer was designed using active low pass filters to integrate signals over the range of  $0\text{ Hz}$  to  $1\text{MHz}$  that were limited to  $\pm 2.5\text{V}$ . The

integration equalizer was composed of six integrators that each operated on a different decade in the range. The integrator of the corresponding frequency range of the signal was used as the overall output of the integrator.

**Challenges:** The low pass filters performed integration when they were in the reject band of the low pass filters. The filters caused attenuation in the signal, so the gain of the integrators was set to  $20dB$  and the integration was divided so that only one decade ( $-20dB$ ) of attenuation was experienced for any frequency. The integrators integrated sine and cosine waves by performing a phase shift so it was imperative that the signals remained in phase after being measured by the probes.

## 5) Task 3.5: Analog Differentiation Operation

**Description:** A differentiation equalizer was designed using active high pass filters to differentiate signals over the range of  $0\text{ Hz}$  to  $1MHz$  that were limited to  $\pm 2.5V$ . The differentiation equalizer was composed of six differentiators that each operated on a different decade in the range. The integrator of the corresponding frequency range of the signal was used as the overall output of the integrator.

**Challenges:** The high pass filters performed integration when they were in the reject band of the high pass filters. The filters caused attenuation in the signal, so the gain of the differentiators was set to  $20dB$  and the differentiation was divided so that only one decade ( $-20dB$ ) of attenuation was experienced for any frequency. The differentiators differentiated sine and cosine waves by performing a phase shift so it was imperative that the signals remained in phase after being measured by the probes.

### 2.1.4 Goal 4: Microcontroller Conditioning

#### 1) Task 4.1: Analog Signal Offset

**Description:** The system operated on signals up to positive and negative signals that ranged from  $\pm 5V$ . The signals must be offset by  $5V$  using an inverting summing amplifier to ensure that the signal was always positive.

**Challenges:** The inverting summation amplifier also inverted the signal, so a value of  $-5V$  was added to the signal and then the signal was inverted. The  $-5V$  tap was provided by the power supply system. A diode was added to ensure that the signal was always positive to prevent damage to the microcontroller ADC.

#### 2) Task 4.2: Analog Signal Scaling

**Description:** The microcontroller ADC was read small voltages up to  $+2V$ . The signal voltage range after offset was from  $0V$  to  $+10V$ . The signal was scaled by  $0.1$  using an inverting amplifier. An additional inverting buffer was needed to rectify the signal so that the signal range was from  $0V$  to  $+1V$  which was within the microcontroller ADC range.

**Challenges:** The inverting amplifier scaled the result based on the ratio of resistances. The precision resistors were needed so that the gain was close to  $0.1$  for the first inverting amplifier and the gain of the second inverting amplifier was unity.

### 2.1.5 Goal 5: Analog Simulation Model

#### 1) Task 5.1: Analog Simulation Design

**Description:** The analog section of the DAQ system was simulated using TI TINA. The analog section was divided into multiple simulation files to perform the different analog system tasks. The simulation files outputted a comma delimited file (CSV) of the data that was read by the digital section of the DAQ system.

**Challenges:** TI TINA was used because it included the Spice files for many Texas Instruments integrated circuits. The simulation was divided into multiple files to decrease simulation time and to observe the signal at different parts in the system.

## 2) Task 5.2: Simulation File Integration

**Description:** The simulation files for the DAQ system were independent files. The outputs of one file were used as the inputs of the next stage by exporting the data and then importing the data into the next file.

**Challenges:** The DAQ system contained many simulation files, so data was exported and imported into TINA multiple times which will takes time. The exported data contained approximately 10 times as many data points as the input. An Excel macro was developed using visual basic for applications (VBA) to filter the data and format the data to be imported into the next simulation file.

## 2.2 Deliverables

The designed DAQ system was composed of an analog section and a digital section. The analog section was composed of TINA simulation files that measured simulated signals and performed mathematical operations on the signals. The analog system was able to perform addition, subtraction, integration, differentiation, and inversion. The simulation files then outputted the information as CSVs that were read and displayed by the digital section of the system.

## 2.3 Specifications and Requirements

**Table 1: Requirements Matrix**

ID	Title	Note	Verification
Requirement 1:	Power Supply System	The power system in the simulation will use a include a $\pm 12V$ power supply with a resistive network to create taps for different voltage levels needed for different components in the system. The power system will have taps for $\pm 12V$ , $1.65V$ , $3.3V$ , and $-5V$	The power supply system simulation file in TINA will be tested by performing DC analysis on the system to observe the DC node voltage at each tap.
Requirement 2:	Analog Signal Conditioning	The simulation probes will use a voltage divider relationship with to transform the input voltage from $\pm 50V$ to $\pm 2.5V$ . The simulation	The system was tested in TINA using frequency analysis to observe the gain and phase of the simulation probes for the frequency

		will also use a third order low pass filter as an anti-aliasing filter to limit frequencies to 1 MHz with no phase shift.	range. The gain of the probes should match the desired division for the entire frequency range and the phase should be zero.
Requirement 3:	Pass Through and Inversion Operations	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file included buffers and inverting buffers to buffer the input signals or invert them. The system was designed to do the opposite of the expected operation. The pass through operation inverted the signal and the inversion operation let the signal pass through.	The system was tested in TINA by performing the pass through and inversion operations for sine waves. The output of was observed to be either be buffered or inverted depending on the operation.
Requirement 4:	Addition Circuit	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file added two signals together using an inverter summation amplifier with a gain of one.	The system was tested in TINA by adding two signals generated by waveform generators. The output of the inverting summation amplifier will be the sum of the two signals and was inverted.
Requirement 5:	Subtraction Circuit	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file subtracted two signals together using a difference amplifier with a gain of one. The signals were arranged to produce the inverse of the desired difference.	The system was tested in TINA by subtracting two signals generated by waveform generators. The output of the difference amplifier will be the difference of the two signals and was inverted.
Requirement 6:	Differentiator Circuit	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file used six active high pass filters. The high pass filters had a gain of ten and each had	The system was tested in TINA using frequency analysis to observe the gain and phase of the differentiators for the frequency range. The cut off frequency for the different integrators was

		a different cut off frequency to differentiate for one decade within the range of 0Hz to 1 MHz. The high pass filter corresponding to the correct frequency of the signal was selected and outputted.	checked so that the entire frequency range was within the roll off rate of one of the filters. The phase of the filters was also observed. A phase shift of 90° indicated integration.
Requirement 7:	Integrator Circuit	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file used six active low pass filters. The low pass filters had a gain of ten and each had a different cut off frequency to integrate for one decade within the range of 0Hz to 1 MHz. The low pass filter corresponding to the correct frequency of the signal was selected and outputted.	The system was tested in TINA using frequency analysis to observe the gain and phase of the integrators for the frequency range. The cut off frequency for the different integrators was checked so that the entire frequency range was within the roll off rate of one of the filters. The phase of the filters was also observed. A phase shift of $-90^\circ$ indicated integration.
Requirement 8:	Microcontroller Conditioning	The simulation file used input and output signals within the frequency range of 0 Hz to 1 MHz and the voltage range $\pm 2.5V$ . The simulation file included offset from an inverting amplifier. The signal was then scaled using an inverting amplifier and was inverted again using an inverting buffer to transform a signal from $\pm 5V$ to $0V$ to $+1V$ .	The system was tested in TINA by conditioning a sine wave within the input voltage range and frequency. The output signal was within the expected output range and was inverted from the input.
Requirement 9:	Simulation File Integration	Excel macros were developed to format data exported from TINA to a format that can be imported into the next file in the simulation. An Excel macro was also developed to format the microcontroller signal into a CSV format to be read by the digital section.	The Excel macros were used to import data from one file to another file. The signal was tested to import signals with a high frequency and a low frequency. The CSV macro was tested on sample data and was then read by the digital section to display the sample data.

Requirement: 10	Digital Input Conditioning	The simulation file will include a comparator system with a Zener diode to compare the digital signal voltage with the reference voltage $1.65V$ . If the digital signal voltage was larger a digital one was outputted as a $3.3V$ pulse. If the digital signal was smaller, a digital zero $0V$ was outputted. The outputted digital signal was exported as a CSV that was read by the digital section.	The digital input section was tested by using square waves at different amplitudes and frequencies as digital inputs. The output waveform should have pulses at $3.3V$ when a digital one was observed and a value of $0V$ when a digital zero was read.
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### 3 Technical Approach and Results

#### 3.1 Final Design

##### 3.1.1 Overview

The DAQ system was composed of different subsystems that were separate simulation files in TINA. The DAQ system was designed to measure analog input voltages between  $\pm 100V$  with frequencies up to  $1\text{ MHz}$ . The DAQ system was designed with four probes to measure up to four different analog signals. The input signals were divided by the different voltage dividers in parallel and were then filtered using the low pass anti-aliasing filters. The different voltage divider signals for each probe were routed to an analog multiplexer. The analog multiplexers were used to select which of the different voltage divisions was used by the system.

The select voltage division for each probe was then routed to two analog multiplexers to select channel 1 and channel 2 signals for the DAQ system. The DAQ system measured and operated on the signals in channel 1 and channel 2, where channel 1 was the primary channel and channel 2 was the secondary channel. The DAQ system performed pass through operations on both channel 1 and channel 2 to allow the measured channel signals to pass through without any mathematical operation or inverted the signal. The DAQ system also performed mathematical operations on one or two signals. The integration and differentiation operations were single signal operations that were performed on the signal in channel 1. The addition and subtraction operations used two signals. The signal in channel 1 was used as the primary signal for the addition and subtraction operation, and the signal in channel 2 was used as the secondary signal for the two signal operations. The operations were performed all in parallel and the operation outputted was selected using an analog multiplexer.

The selected operation was then conditioned to be read by the microcontroller. The microcontroller had three ADC channels. It was planned for one of the channels to be used for the channel 1 pass through operations, another channel was to be used for the channel 2 pass through operations, and the last channel was used for the selected math operation. The microcontroller was a low voltage device, so the ADC was only able to read positive voltages no more than  $+2V$ . The analog system conditioned the output signal to be within the readable range of the microcontroller. The signal was then exported as a CSV that was read by the digital section of the system.

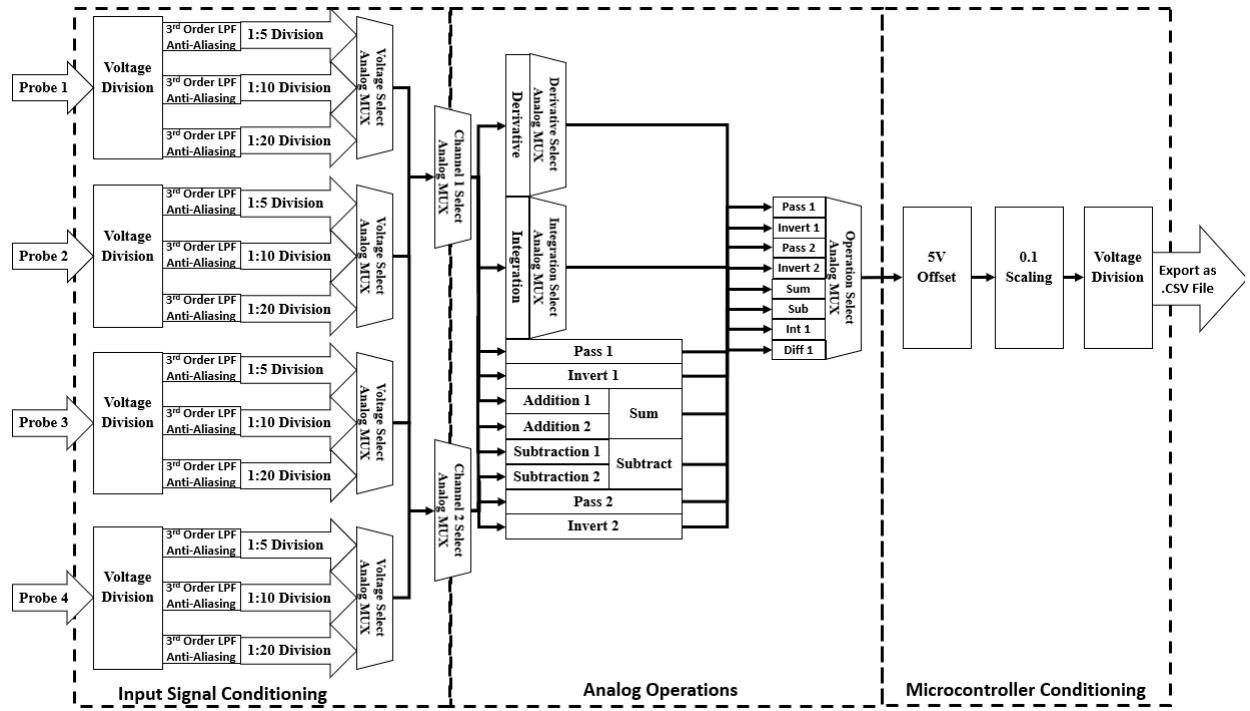


Figure 3. Analog Input Block Diagram

The DAQ system also measured digital signals using four digital signal probes. The digital signal probes regulated the voltage to within the system voltage range of  $\pm 12V$  by using Zener diodes. The regulated voltage was then compared using a comparator integrated circuit. The signal was compared to  $1.65V$  which was half of the logic high voltage of the system which was  $3.3V$ . If the signal was greater than half the logic high voltage, then a logic one at  $3.3V$  was outputted. If the signal was less than half the logic high voltage, then a logic zero at  $0V$  was outputted. The outputted signal was converted into a CSV and was exported to the digital section of the system.

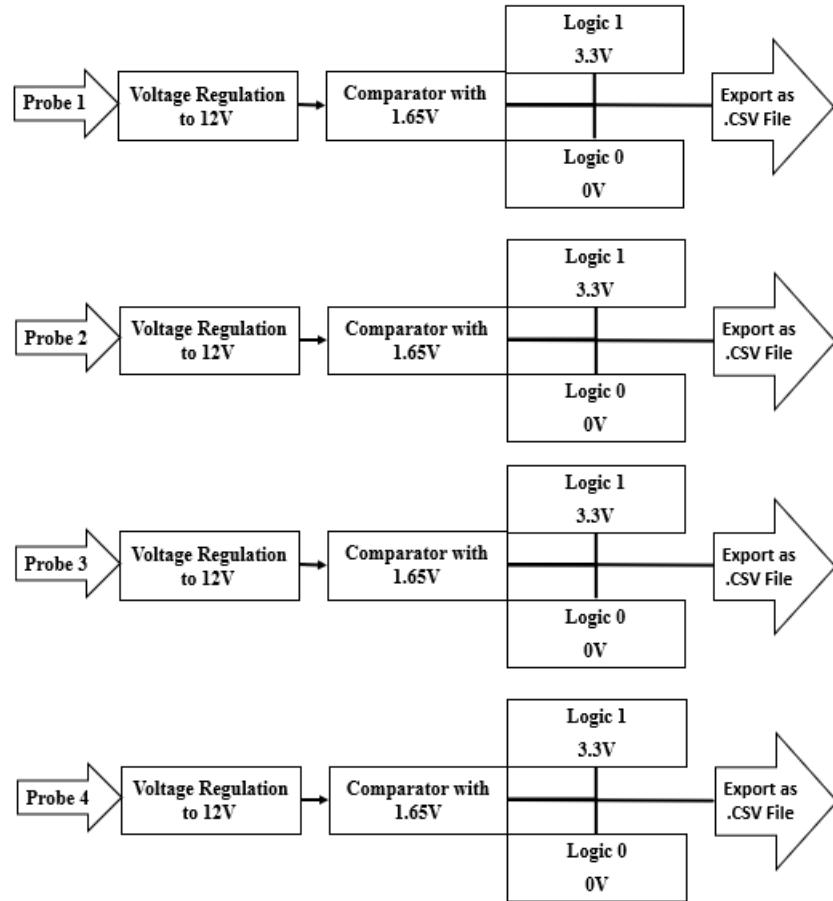


Figure 4. Digital Input Block Diagram

### **3.1.2 Analog System Flow and Excel Macros**

The DAQ system was simulated by starting at the analog probe simulation to measure a simulated signal. The next simulation file used the output of the previous file as the input to simulate a continuous system over different simulation files. The output signals of one circuit in the simulation files were used as the input of the next circuit by exporting the outputs and importing them into the next circuits. TI TINA had the ability to export simulation files as text files. The text files were opened in Microsoft Excel and processed using an Excel Macro written in Visual Basic for Application (VBA). Three macros were designed to format exported data throughout the system.

The first macro was the split samples macro. When the outputs of TINA simulation were exported, they were all saved in one text file. The split samples macro splits the outputs to separate files so that each output can be imported separately. The split samples macro was used for the analog probe circuit to separate the different voltage division outputs into different files to be imported to the next circuit.

When a TINA simulation used an imported signal, the output had approximately ten times as many samples as the input. The DAQ simulation system used continuous exported and imported signals. If the samples multiplied by ten each time a signal was exported, the number of samples used in the later sections of the circuit will be too large and cause the simulation time to increase. The Excel macro filter samples was designed to split the output samples to individual files similar to the split samples macro. The filter samples macro also contained a modulus counter that only extract one out of every ten samples. The filter samples macro was designed so that the number of output and input samples was the same. The filter samples macro was used for the output of all the simulation files except for the analog probe circuit and the microcontroller conditioning circuit. The filter samples macro was used for files simulation files with only one output signal to reduce the number of output samples.

The CSV sample macro was used on the output of the microcontroller conditioning circuit to prepare the data into a format that can be read by the digital system. The CSV samples macro formatted the CSV file so that the first line contained the total simulation time. The second line contained the DC offset of the signal in millivolts. The DC offset was always 500 mV because the microcontroller conditioning circuit had a fixed offset of 5V that was scaled by an inverting amplifier with a gain of 0.1. The third line contained the scaling factor used to multiply the data to obtain the actual values. The scaling factor was based on the voltage division selected in the voltage select circuit. The microcontroller output must be set to match the voltage division selected in the voltage select circuit to simulate the communication between different circuits in the analog section of the DAQ system. The scaling factor was equal to the voltage division selected multiplied by ten because of the fixed scaling factor in the microcontroller conditioning circuit. The next lines contained the data points exported from TINA.

### 3.1.3 Power Supply Design

The DAQ system was designed to be powered with a  $\pm 12V$  linear power supply. A linear power supply was used because a linear power supply produced less ripples than a switch mode power supply. It was imperative to maintain smooth voltages levels to act as a smooth reference for the measured signals. The tap voltages were obtained from the power supply by using a voltage divider. It was also possible to generate the tap voltages using Zener diodes with the corresponding reverse breakdown voltage.

The  $\pm 12V$  was used throughout the system to power all operational amplifiers and integrated circuits used in the DAQ system. The  $1.65V$  and  $3.3V$  taps were used only for the digital input to compare and generate digital signals readable by the microcontroller. The  $-5V$  tap was used only for the microcontroller conditioning circuit to add an offset so that the signal experienced by the microcontroller was always positive.

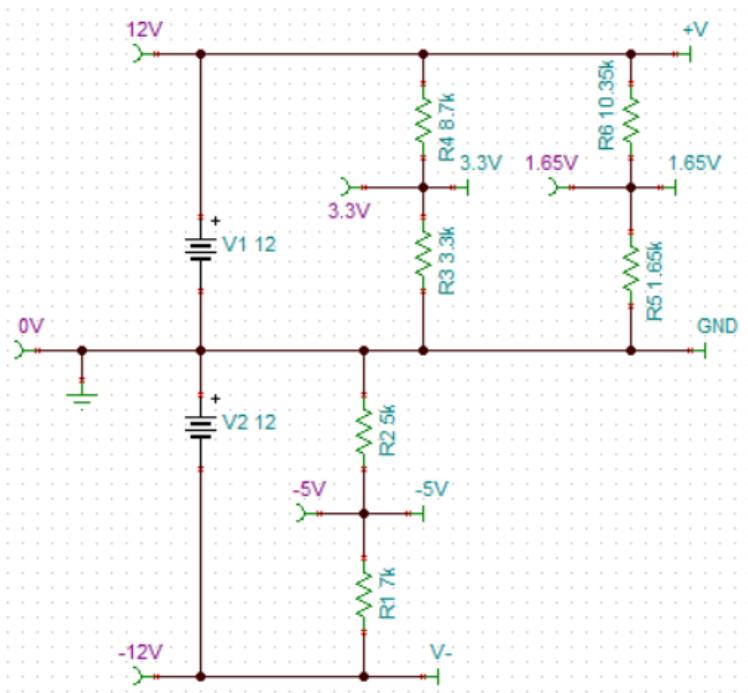


Figure 5. Power Supply Circuit Diagram

$$V_{tap} = \pm 12 \left( \frac{R_2}{R_1 + R_2} \right)$$

$$R_1 + R_2 = 12 \text{ k}\Omega$$

$V_{tap} = 1.65V$	$V_{tap} = 3.3V$	$V_{tap} = -5V$
$R_1 = 10.35 \text{ k}\Omega$	$R_1 = 8.7 \text{ k}\Omega$	$R_1 = 7 \text{ k}\Omega$
$R_2 = 1.65 \text{ k}\Omega$	$R_2 = 3.3 \text{ k}\Omega$	$R_2 = 5 \text{ k}\Omega$

### 3.1.4 Analog Probe Conditioning Design

The DAQ system included four probe circuits to measure four different analog voltages. One end of the probe was attached to the measuring point in the circuit and the other end of the probe was grounded. The analog probes designed for the DAQ system were grounded, so the system cannot perform differential measurements with one probe. The probes divided the analog signal using voltage divider resistance chain. The signal was then filtered using a third order low pass filter to prevent aliasing. The signal for each of the voltage dividers in the resistance chain were filtered and outputted.

The first system inside of the probe conditioning circuit was the voltage divider resistance chain. The resistance chain generated the different division voltages based on the voltage divider of the different resistances. The overall resistance of the probe was the sum of the entire resistance chain. A good oscilloscope probe had a large input resistance so that it acted as an open circuit in most circuits and did not disturb the circuit it was measuring. A typical oscilloscope probe has an input resistance of  $1 M\Omega$ , but the input resistance of the designed probe was much less than  $1 M\Omega$ . It was possible to increase the input resistance of the probe by increasing the resistances of all the resistors in the resistance chain by the same factor.

The voltage divider resistance chain was set to divide the analog voltage by 5, 10, and 20. The system voltage was  $\pm 12V$ , so the input voltage should be not be larger than  $\pm 12V$ . The worst case was considered when a  $\pm 50V$  signal was read by the probe at the lowest voltage division. The observed signal at a voltage division of 5 read a signal by  $\pm 10V$  which was the maximum acceptable voltage in the system. A solution to this problem was to increase the system voltage to  $\pm 24V$ , however, the  $\pm 12V$  linear power supply was already purchased.

The anti-aliasing filters were first order low pass filters with buffers spaced between them to provide isolation. The cut off frequency of the low pass filters was set to be much larger than the maximum system frequency of  $1 MHz$ . The cut off frequency was set to be higher so that  $1 MHz$  signals were well within the pass band of the filters so that they were not attenuated or phase shifted. Attenuation or phase shift caused by the anti-aliasing filters will cause the measured signal to appear incorrect at the output.

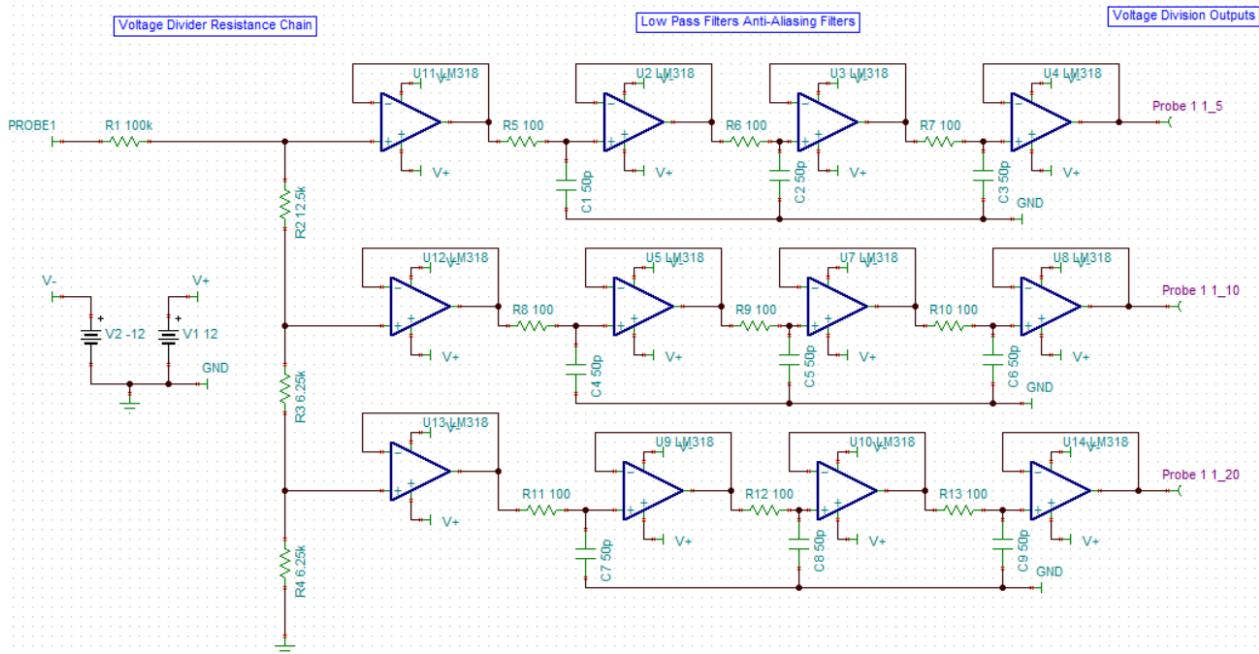


Figure 6. Analog Probe Conditioning Circuit Diagram

$$\begin{aligned}
 R_{in} &= R_1 + R_2 + R_3 + R_4 \\
 R_{in} &= 100 + 12.5 + 6.25 + 6.25 \\
 R_{in} &= 125 \text{ k}\Omega
 \end{aligned}$$

$$\begin{aligned}
 f_{cut} &= \frac{1}{2\pi RC} \\
 f_{cut} &= \frac{1}{2\pi(100)(50 * 10^{-12})} \\
 f_{cut} &= 31.83 \text{ MHz}
 \end{aligned}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_N}{R_1 + R_2 + R_3 + R_4}$$

<i>Voltage Divider</i> $\frac{1}{5}$	<i>Voltage Divider</i> $\frac{1}{10}$	<i>Voltage Divider</i> $\frac{1}{20}$
$12.5 + 6.25 + 6.25$	$6.25 + 6.25$	$6.25$
$\frac{1}{100 + 12.5 + 6.25 + 6.25}$	$\frac{1}{100 + 12.5 + 6.25 + 6.25}$	$\frac{1}{100 + 12.5 + 6.25 + 6.25}$
$\frac{V_{out}}{V_{in}} = \frac{1}{5}$	$\frac{V_{out}}{V_{in}} = \frac{1}{10}$	$\frac{V_{out}}{V_{in}} = \frac{1}{20}$

### 3.1.5 Voltage Select Design

Each of the four analog probes generated three signals for the different voltage divisions. The voltage division used by the DAQ system must be selected from the three provided. The voltage selection circuit consisted of the three voltage divisions for each probe connected to an analog 8:1 multiplexer. The analog multiplexer was controlled by manually controlled switches to select the desired voltage division. The same voltage division was used for all analog probes to maintain consistency for math operations that used two probes inputs.

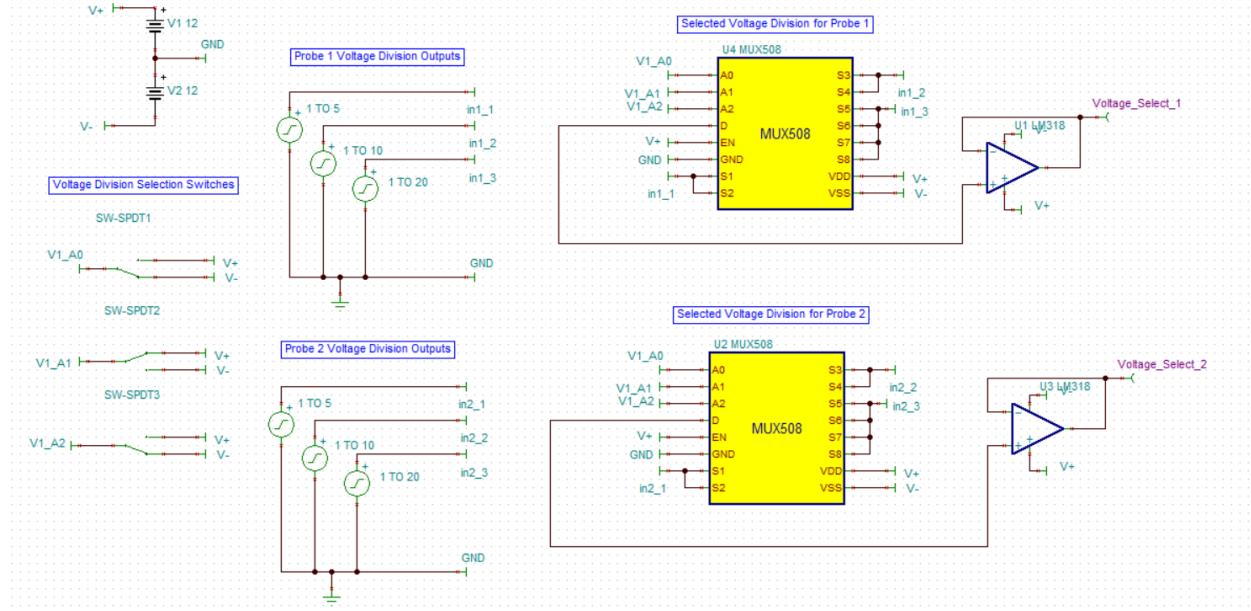


Figure 7. Voltage Division Select Circuit Diagram

### 3.1.6 Channel Select Design

The DAQ system was designed with four analog probes but was only able to measure two signals at a time. The two signals selected from the four probes were denoted as Channel 1 and Channel 2. The selected voltage division for each probe was routed to a separate analog 8:1 analog multiplexer. One analog multiplexer selected the signal for Channel 1 and the other analog multiplexer selected the signal for Channel 2. Channel 1 was considered the primary channel and channel 2 was considered the secondary channel. The analog multiplexers were controlled with a separate set of switches so that the choice of channel signals was complete independent from each other. It was possible to select the same probe signal for Channel 1 and Channel 2. The DAQ system performed all operations and measurements on the signals in Channel 1 and Channel 2.

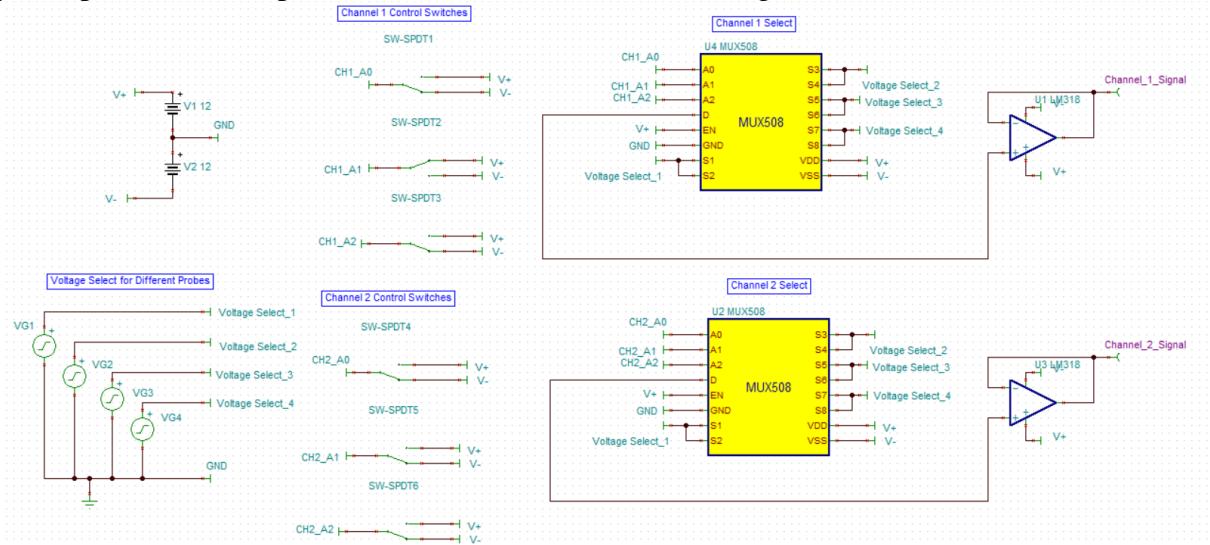


Figure 8. Channel Select Circuit Diagram

### 3.1.7 Pass and Invert Operation Design

The DAQ system performed the pass and invert operations on signals in both Channel 1 and Channel 2. The pass operation let the measured signal to be passed through the DAQ system without performing any mathematical operation. The invert operation inverted the channel signal and then passed the signal through the DAQ system without any mathematical operation. The DAQ system included an additional inverting buffer so all signals were inverted from the desired waveform. The pass operations used an inverting amplifier with a gain of one to invert the signal so that it will be inverted again at the end of the system. The invert operations used a buffer to pass the signal so that it will be inverted at the end of the system.

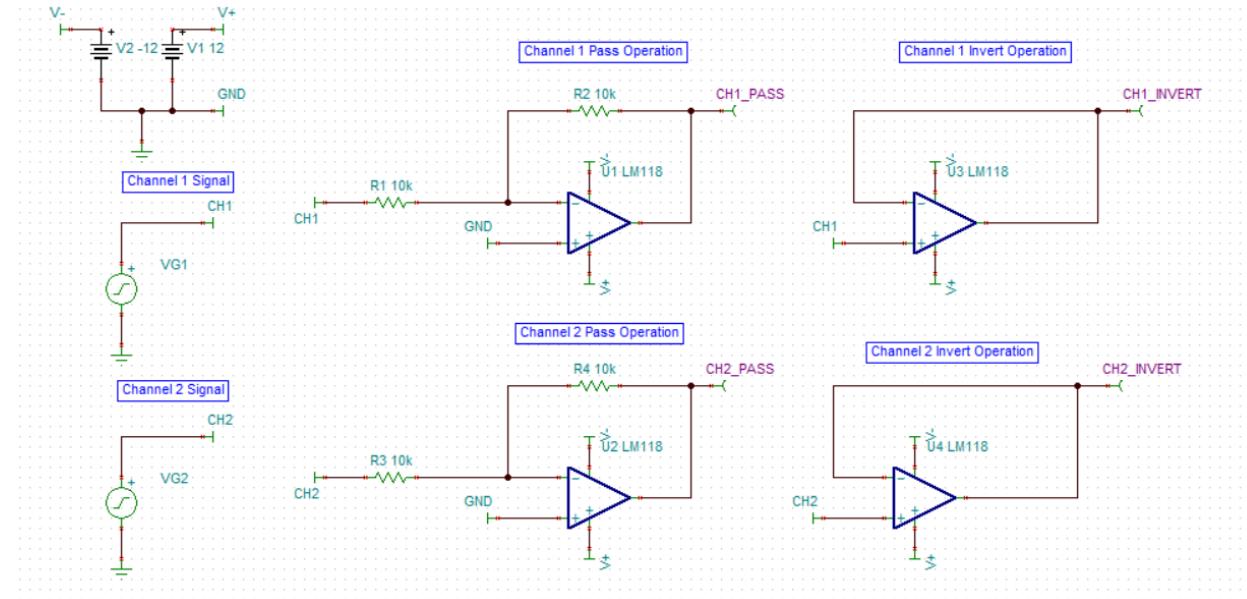


Figure 9. Pass and Invert Operation Circuit Diagram

$$A = -\frac{R_2}{R_1}$$

$$A = -\frac{10 \text{ k}\Omega}{10 \text{ k}\Omega}$$

$$A = -1$$

### 3.1.8 Addition Operation Design

The DAQ system performed the addition operation using both channel signals with an inverting amplifier. The gain of the inverting summing amplifier was dependent on the ratio of resistances. The gain of the inverting summing amplifier was set to one so that the circuit added the signals without any additional gain. The inverting summing amplifier also inverted the signal and was buffered.

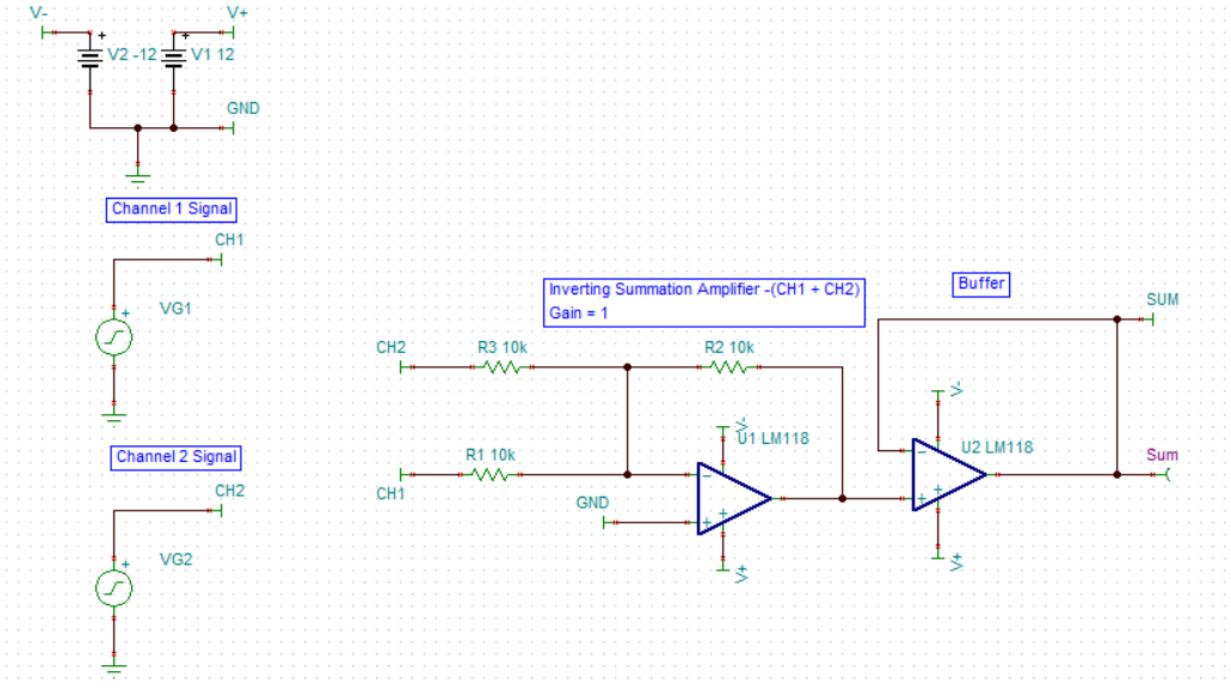


Figure 10. Inverting Summation Circuit Diagram

$$\begin{aligned}
 V_{out} &= -\frac{R_2}{R_1} CH1 + -\frac{R_3}{R_1} CH2 \\
 V_{out} &= -\frac{10 k\Omega}{10 k\Omega} CH1 + -\frac{10 k\Omega}{10 k\Omega} CH2 \\
 V_{out} &= -(CH1 + CH2)
 \end{aligned}$$

### 3.1.9 Subtraction Operation Design

The DAQ system performed the subtraction operation using both channel signals with a difference amplifier. The difference amplifier was connected so that the operation  $CH2 - CH1$  was performed and then buffered. The end of the analog DAQ system contained an additional inverting buffer that will invert the signal to the desired  $CH1 - CH2$ . The transfer function of the difference amplifier was calculated using circuit analysis assuming an ideal operational amplifier.

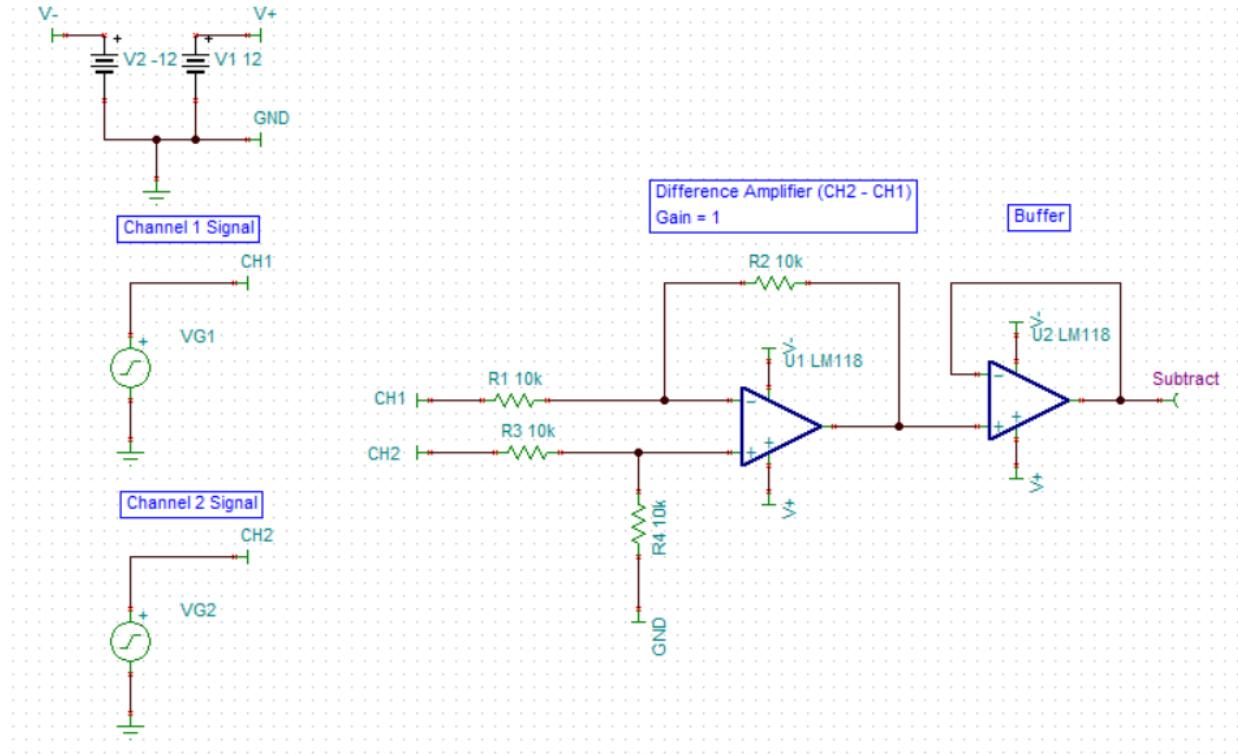


Figure 11. Difference Amplifier Circuit Diagram

$$\begin{aligned}
V_2 &= \left( \frac{R_4}{R_4 + R_3} \right) CH2 \\
I_1 &= \frac{\frac{V_1 - V_2}{CH1 - V2}}{R_1} \\
I_1 &= \frac{CH1 - \left( \frac{R_4}{R_4 + R_3} \right) CH2}{R_1} \\
I_2 &= \frac{V_2 - V_{out}}{R_2} \\
I_2 &= \frac{\left( \frac{R_4}{R_4 + R_3} \right) CH2 - V_{out}}{R_2} \\
I_1 &= I_2 \\
\frac{CH1 - \left( \frac{R_4}{R_4 + R_3} \right) CH2}{R_1} &= \frac{\left( \frac{R_4}{R_4 + R_3} \right) CH2 - V_{out}}{R_2} \\
V_{out} &= \left( \left( \frac{R_4}{R_4 + R_3} \right) + \left( \frac{R_2 R_4}{R_1 (R_4 + R_3)} \right) \right) CH2 - \left( \frac{R_2}{R_1} \right) CH1 \\
V_{out} &= \left( \frac{R_4 R_1 + R_2 R_4}{R_1 (R_4 + R_3)} \right) CH2 - \left( \frac{R_2}{R_1} \right) CH1 \\
V_{out} &= \left( \frac{R_4}{R_4 + R_3} \right) \left( \frac{R_1 + R_2}{R_1} \right) CH2 - \left( \frac{R_2}{R_1} \right) CH1 \\
R_1 &= R_2 = R_3 = R_4 = 10 \text{ k}\Omega \\
V_{out} &= CH2 - CH1
\end{aligned}$$

### 3.1.10 Derivative Operation Design

The DAQ system performed the derivative operation only on the Channel 1 signal. The derivative operation was performed using an active high pass filter. A high pass filter acted as a differentiator when the signal was in the reject band of the filter. The further the signal was in the reject band, the stronger the attenuation. A derivative equalizer was designed so that for each decade in the frequency range from 1 Hz to 1 MHz a separate high pass filter performed the differentiation. The frequency range from 1 Hz to 1 MHz was six decades, so a total of six differentiator circuits were used. The Channel 1 signal was buffered and split between three differentiators each to prevent fan-out issues.

The derivative equalizer was designed so that only one decade of attenuation was experienced for any differentiated signal regardless of frequency. The gain for each active high pass filter was set to 10 to offset the attenuation experienced in the cut off region. The filters were designed to operate in the cut off region, so the high pass filters were designed with cut off frequencies approximately one decade higher than the specified derivative range.

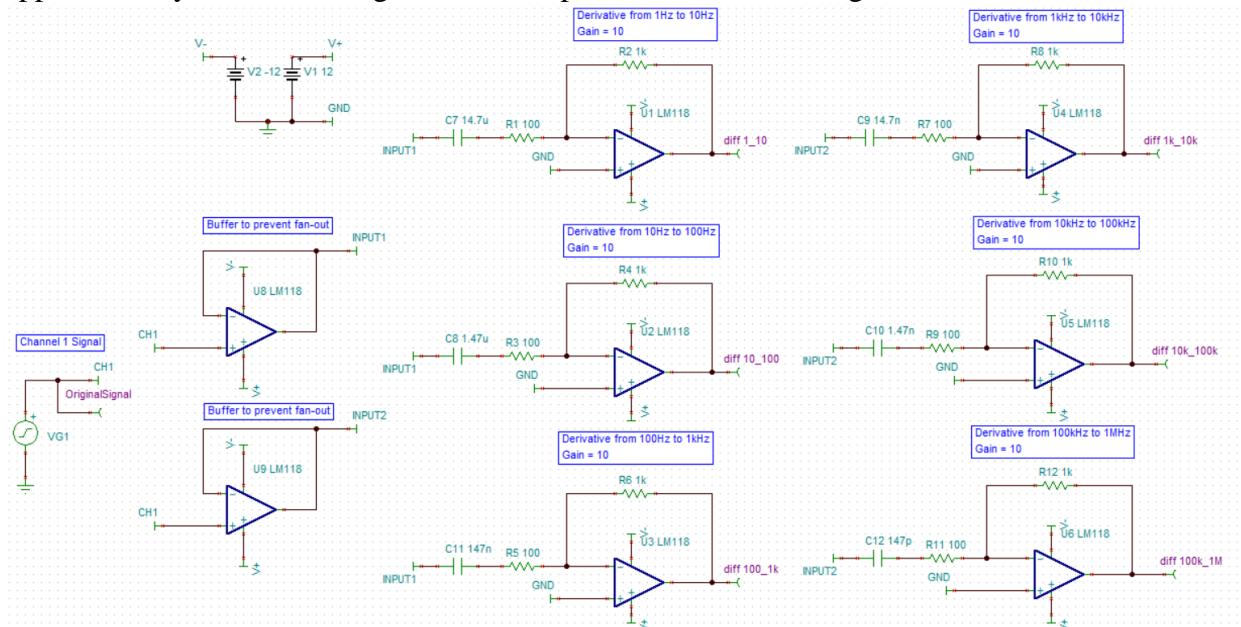


Figure 12. Derivative Operation Circuit Diagram

$1 \text{ Hz to } 10 \text{ Hz}$	$10 \text{ Hz to } 100 \text{ Hz}$	$100 \text{ kHz to } 1 \text{ kHz}$
$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(14.7 * 10^{-6})}$ $f_{cut} \approx 100 \text{ Hz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(1.47 * 10^{-6})}$ $f \approx 1 \text{ kHz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(147 * 10^{-9})}$ $f \approx 10 \text{ kHz}$

$1 \text{ kHz to } 10 \text{ kHz}$	$10 \text{ kHz to } 100 \text{ kHz}$	$100 \text{ kHz to } 1 \text{ MHz}$
$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(14.7 * 10^{-9})}$ $f \approx 100 \text{ kHz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(1.47 * 10^{-9})}$ $f \approx 1 \text{ MHz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100)(147 * 10^{-12})}$ $f \approx 10 \text{ MHz}$

### 3.1.11 Derivative Select Design

The derivative equalizer applied all six differentiators in parallel, so the correct differentiator must be selected based on the frequency of the signal. The derivative outputs for all the differentiators were inputted into an analog multiplexer. The multiplexer was controlled by manual switches to choose the correct differentiator and the output was buffered.

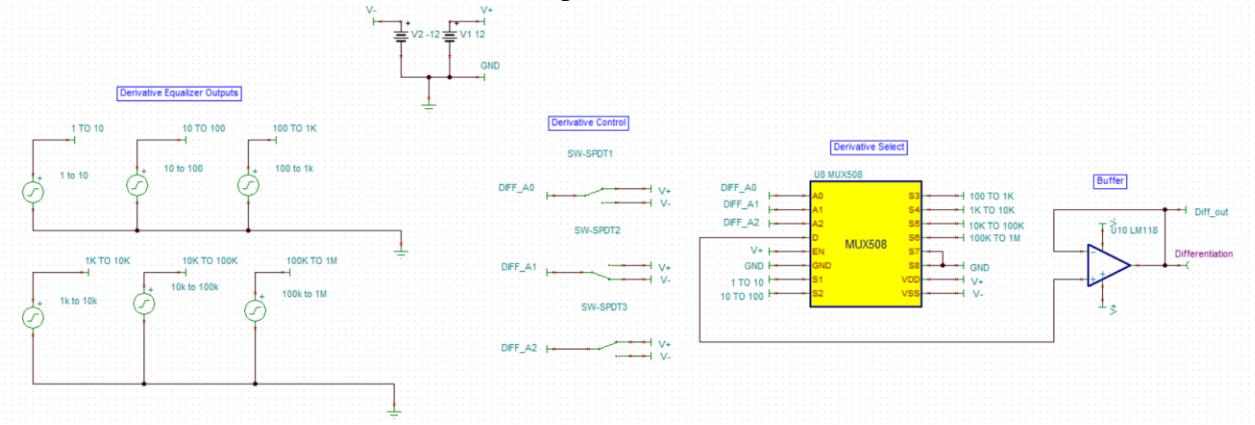


Figure 13. Derivative Select Circuit Diagram

### 3.1.12 Integration Operation Design

The DAQ system performed the integration operation only on the Channel 1 signal. The integration operation was performed using an active low pass filter. A low pass filter acted as a differentiator when the signal was in the reject band of the filter. The further the signal was in the reject band, the stronger the attenuation. An integrator equalizer was designed so that for each decade in the frequency range from 1 Hz to 1 MHz a separate low pass filter performed the integration. The frequency range from 1 Hz to 1 MHz was six decades, so a total of six integrator circuits were used. The Channel 1 signal was buffered and split between three integrators each to prevent fan-out issues.

The integration equalizer was designed so that only one decade of attenuation was experienced for any integrated signal regardless of frequency. The gain for each active low pass filter was set to 10 to offset the attenuation experienced in the cut off region. The filters were designed to operate in the cut off region, so the low pass filters were designed with cut off frequencies approximately one decade less than the specified derivative range.

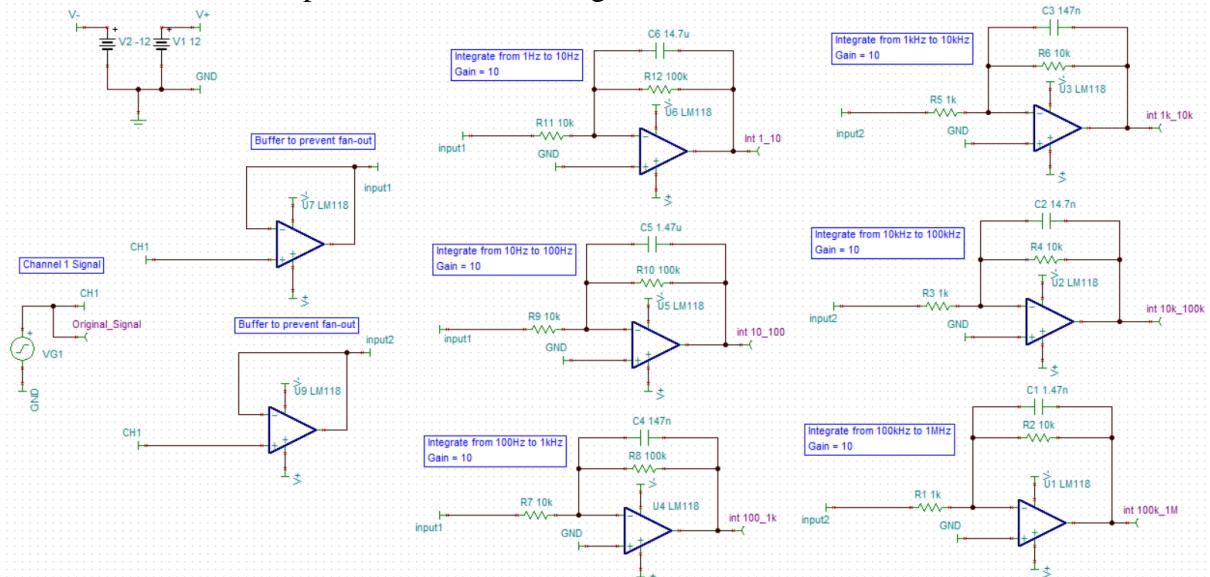


Figure 14. Integration Operation Circuit Diagram

$1 \text{ Hz to } 10 \text{ Hz}$	$10 \text{ Hz to } 100 \text{ Hz}$	$100 \text{ kHz to } 1 \text{ kHz}$
$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100 * 10^3)(14.7 * 10^{-6})}$ $f_{cut} \approx 0.1 \text{ Hz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100 * 10^3)(1.47 * 10^{-6})}$ $f \approx 1 \text{ Hz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(100 * 10^3)(147 * 10^{-9})}$ $f \approx 10 \text{ Hz}$

$1 \text{ kHz to } 10 \text{ kHz}$	$10 \text{ kHz to } 100 \text{ kHz}$	$100 \text{ kHz to } 1 \text{ MHz}$
$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(10 * 10^3)(147 * 10^{-9})}$ $f \approx 100 \text{ Hz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(10 * 10^3)(14.7 * 10^{-9})}$ $f \approx 1 \text{ kHz}$	$\frac{1}{2\pi RC}$ $\frac{1}{2\pi(10 * 10^3)(1.47 * 10^{-9})}$ $f \approx 10 \text{ kHz}$

### 3.1.13 Integration Select Design

The integration equalizer applied all six integrators in parallel, so the correct integrator must be selected based on the frequency of the signal. The integration outputs for all the integrators were inputted into an analog multiplexer. The multiplexer was controlled by manual switches to choose the correct integrator and the output was buffered.

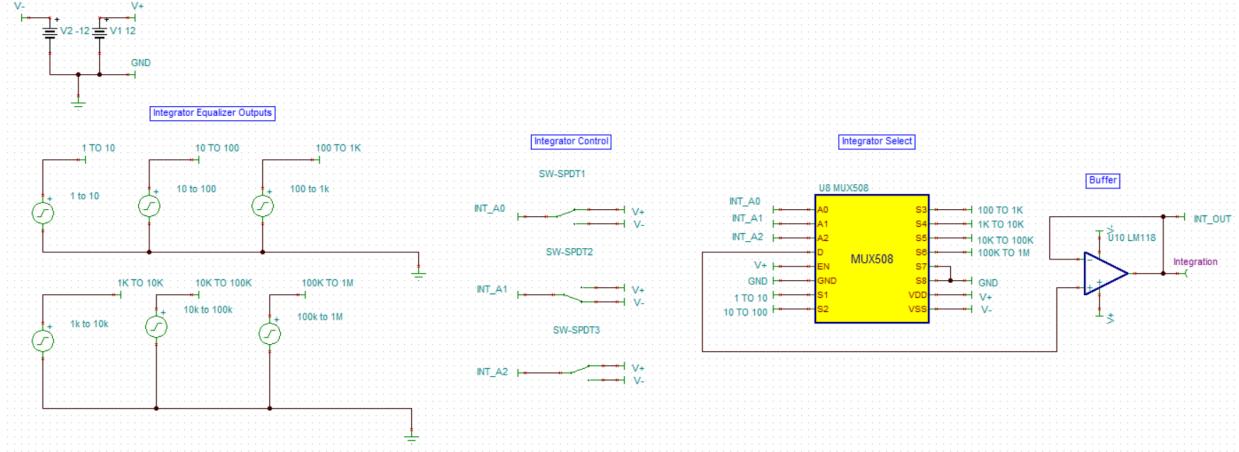


Figure 15. Integration Select Circuit Diagram

### 3.1.14 Operation Select Design

The DAQ system performed all operations in parallel and the desired operation to display must be selected. The output for all the operations was routed to an analog multiplexer that controlled which operation was outputted to the microcontroller. The operation selection multiplexer was controlled by a set of manual switches to select the desired operation. The selected operation was then buffered.

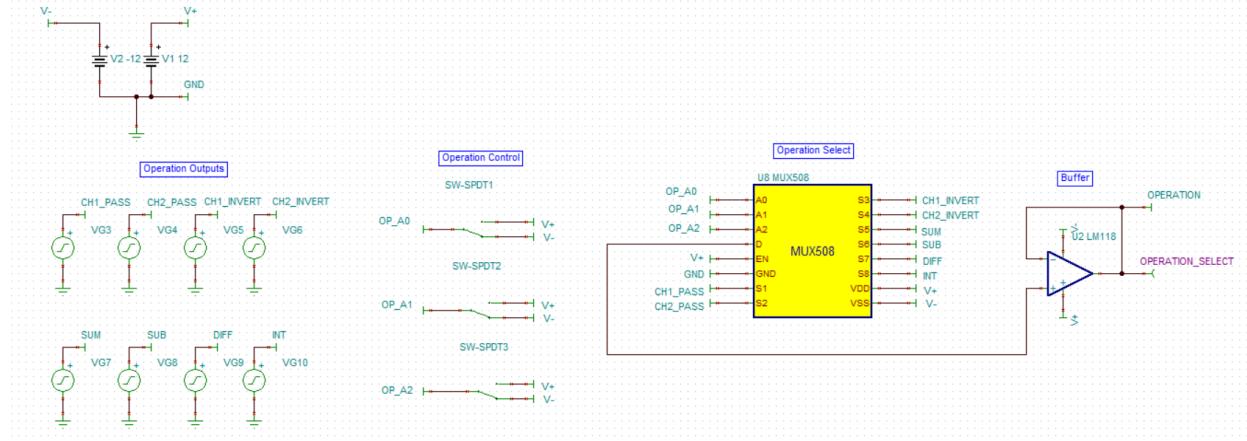


Figure 16. Operation Select Circuit Diagram

### 3.1.15 Microcontroller Conditioning Design

The selected operation must be conditioned to be a signal that the microcontroller can read. The selected operation signal ranged in value from  $\pm 5V$ . The microcontroller was a low voltage device, so the ADC of the microcontroller was only able to read positive voltages up to  $+2V$ . The signal was offset by  $-5V$  using an inverting amplifier so that the signal was always positive. A diode was added at the output to check to make sure that the signal was always positive.

$$-(\pm 5 - 5) = 0V \text{ to } 10V$$

The magnitude of the signal was too large, so the signal was scaled using an inverting amplifier with a gain of 0.1.

$$-(0.1)(+10V) = 0V \text{ to } -1V$$

An additional inverting buffer with a gain of one was added to correct the inverted signal

$$(-1)(-1V) = 0V \text{ to } 1V$$

The microcontroller conditioning circuit also included a voltage select switch system. The voltage select switch system was used to denote what voltage division was used. The other outputs were set to the negative supply voltage to denote that they were not used. The TINA files were independent simulation files, so the switch system was necessary to communicate information from the voltage select circuit to the microcontroller conditioning circuit. An actual DAQ system will be able to communicate with the different parts of the system without the need for the switch system. The output signal was exported as a text file and formatted to a CSV file to be read by the digital section of the DAQ system.

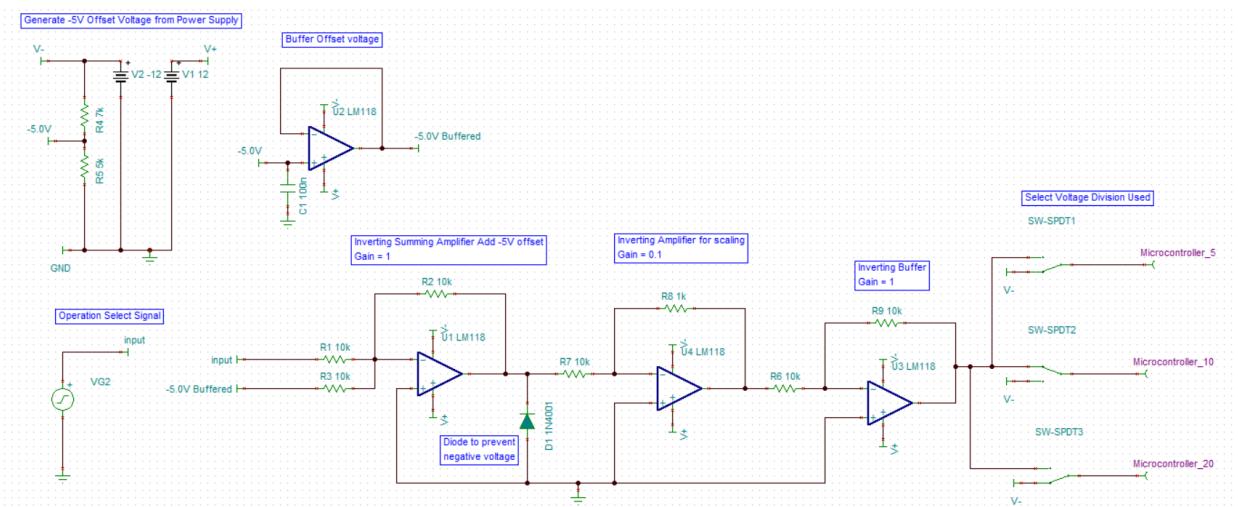


Figure 17. Microcontroller Conditioning Circuit Diagram

### 3.1.16 Digital Probe Design

The digital input probe was designed to read a digital signal and compare it to the logic voltage of the microcontroller to determine if the signal was a logic one or a logic zero. The microcontroller used a voltage of  $3.3V$  for logic one and a voltage of  $0V$  for logic zero. The input digital signal was first regulated and rectified using a Zener diode. The Zener diode was designed to have a reverse breakdown voltage of  $10V$ , so that the input positive was clipped at  $10V$ . The Zener diode also clipped the input negative voltages to around  $-1V$  based on the turn on voltage of the Zener diode. The digital voltage was regulated between  $-1V$  and  $10V$  so that the digital voltage did not exceed the system voltage of  $\pm 12V$ . The regulated voltage was then compared with the  $1.65V$  tap voltage, which was half of the digital one voltage. If the digital signal was greater than half of the digital one voltage, the  $3.3V$  reference voltage was pulled down and a digital one was read. If the digital signal was less than the digital one voltage, the output was grounded to  $0V$  and a digital zero was read. The output digital signal was then exported as a text file. The CSV samples macro was run on the text file to convert the digital output to a CSV that was read by the digital system.

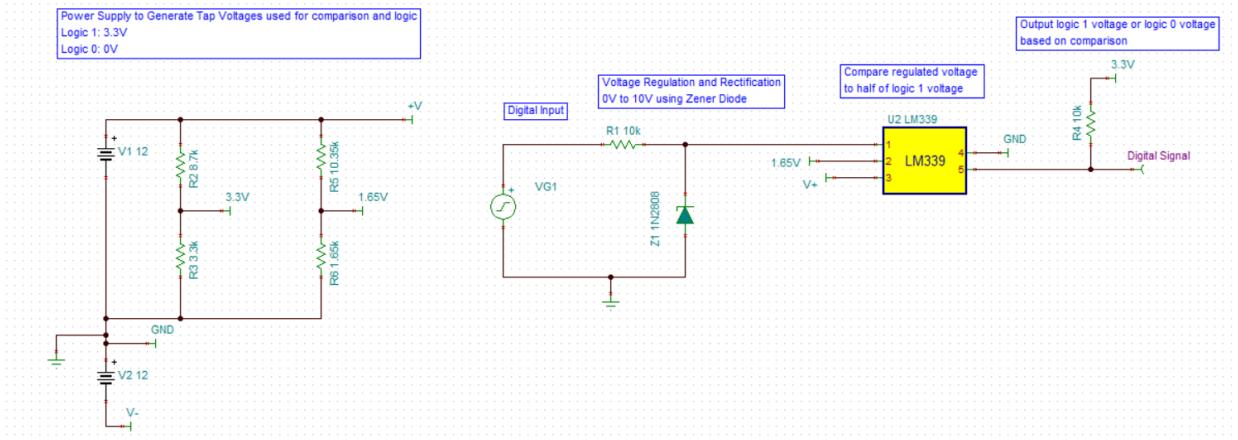
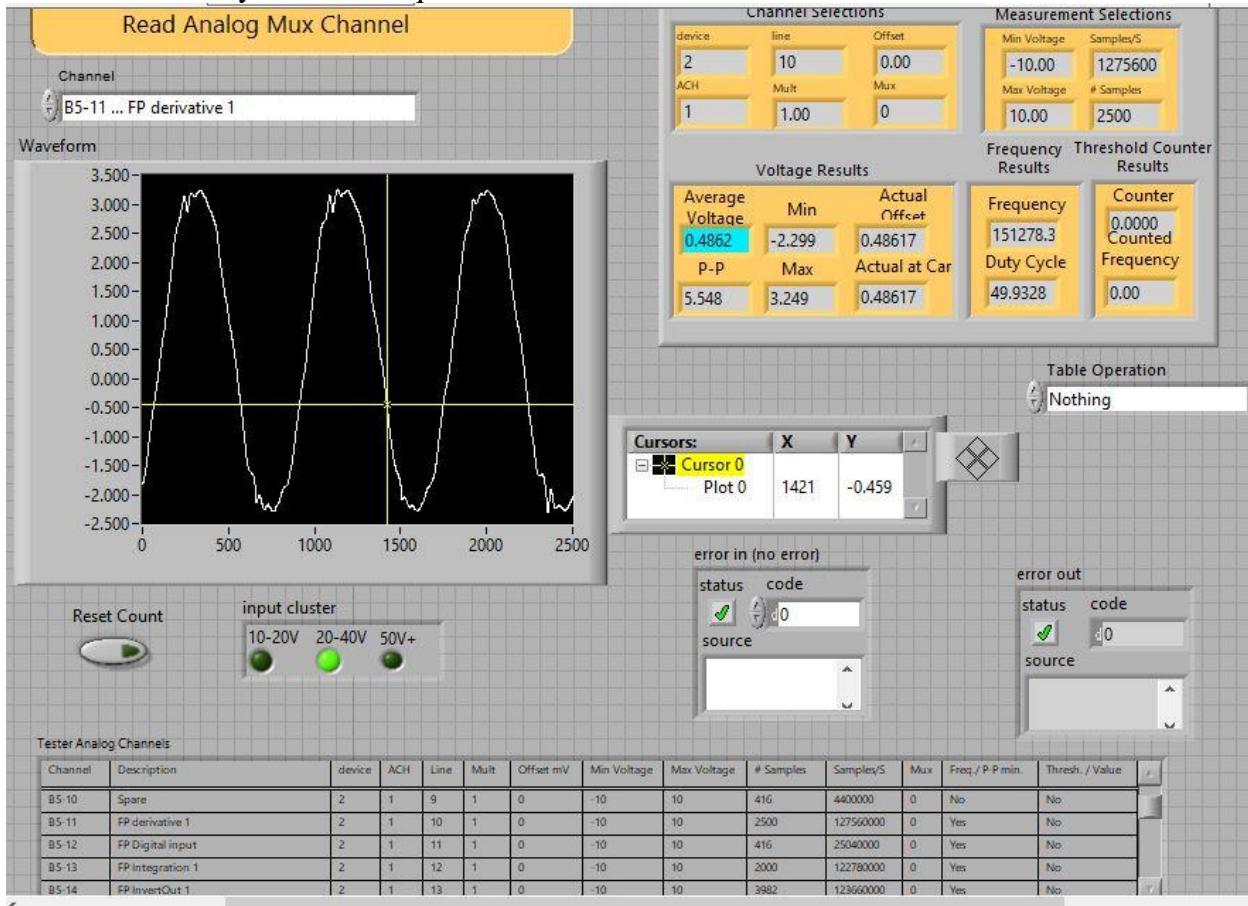


Figure 18. Digital Probe Circuit Diagram

### 3.1.17 Digital User Interface

The end digital user interface uses LabVIEW to view the received signal, either real or simulated from the data acquisition device or from the simulated CSV file. The end user display has a

configurable array that allows the user to alter the samples per second of the signal and allows for easy scaling of the end waveform. The user interface also allows the user to easily select which channel they desire to acquire a waveform from.



## 3.2 Results

### 3.2.1 Power Supply Verification

The power supply system was verified by performing DC analysis on the TINA circuit. The table of DC values shows that all node values were equal to the expected values needed for the DAQ system.

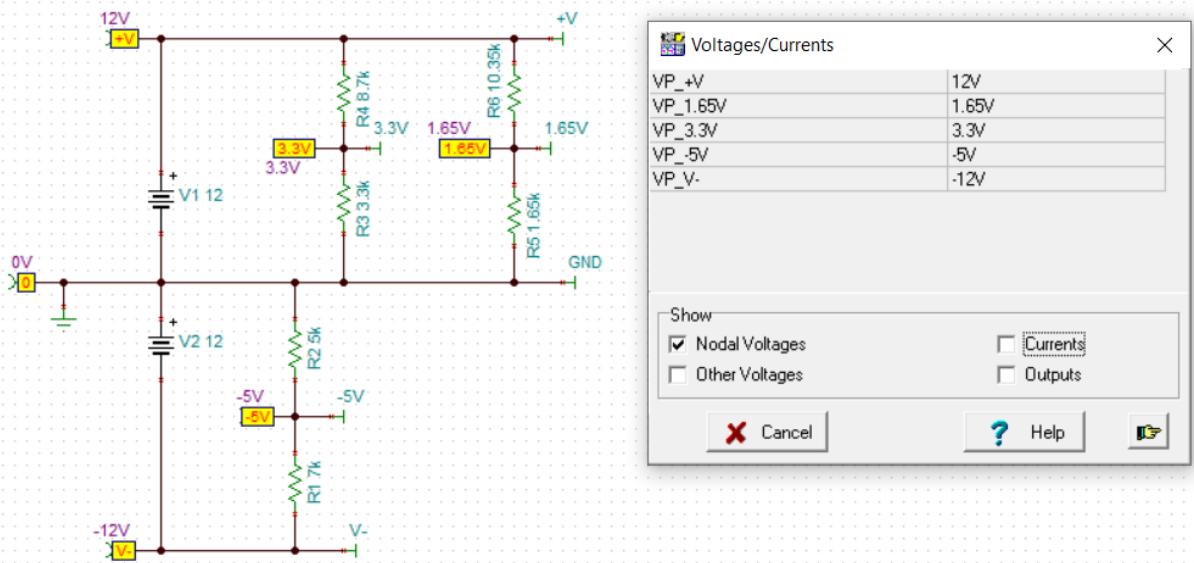


Figure 19. Power Supply DC Analysis

### 3.2.2 Analog Probe Verification

The voltage probe for each of the voltage divisions was analyzed in TINA using AC analysis. The anti-aliasing filter for each of the voltage divisions was designed with a cut off frequency of 31.83 MHz. The response was observed for frequencies well within the passband of the anti-aliasing filter and at the frequency limit of 1 MHz.

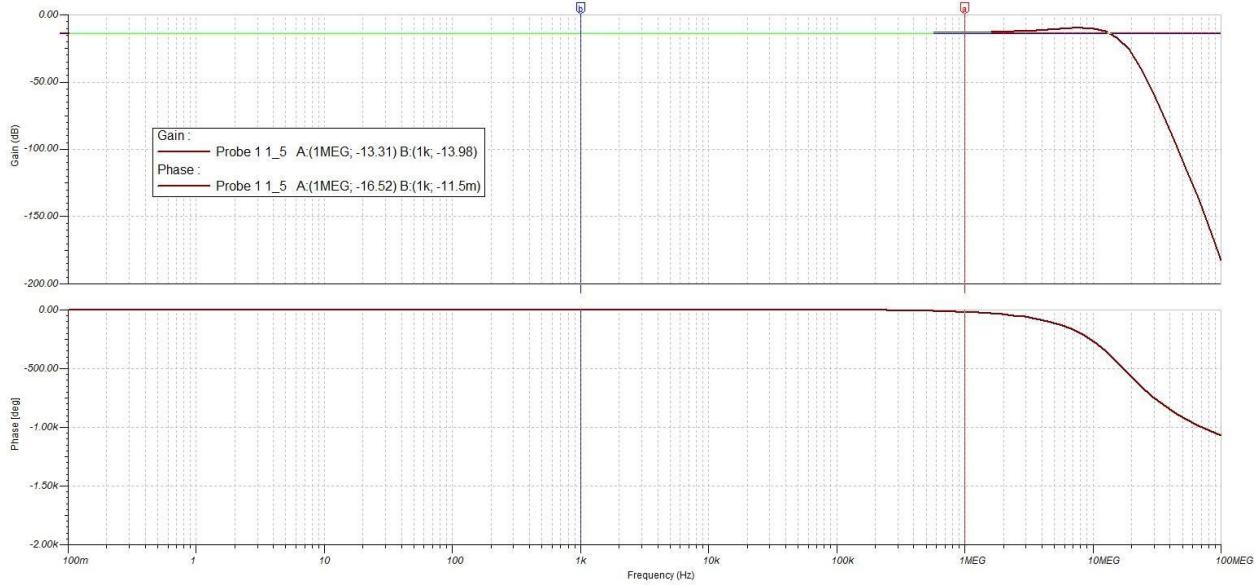


Figure 20. Analog Probe 1:5 Frequency Analysis

Pass Band	Frequency Limit
$G = 10^{\frac{-13.98}{20}}$	$G = 10^{\frac{-13.31}{20}}$
$G = 0.19999$	$G = 0.21602$
$G \approx \frac{1}{5}$	$G \approx \frac{1}{5}$
$\text{Phase Shift} = -0.00115^\circ$	$\text{Phase Shift} = -16.52^\circ$
$\text{Phase Shift} \approx 0^\circ$	

The attenuation was reduced slightly at the frequency limit but was still relatively close to the voltage division. The phase shift within the passband of the filter was near zero, but the phase at the frequency limit of 1 MHz experienced a significant phase shift. All phase shifts in the DAQ system were relative to the measured phase of the voltage probe, so the displayed signal will be out of phase of the original signal by a significant amount.

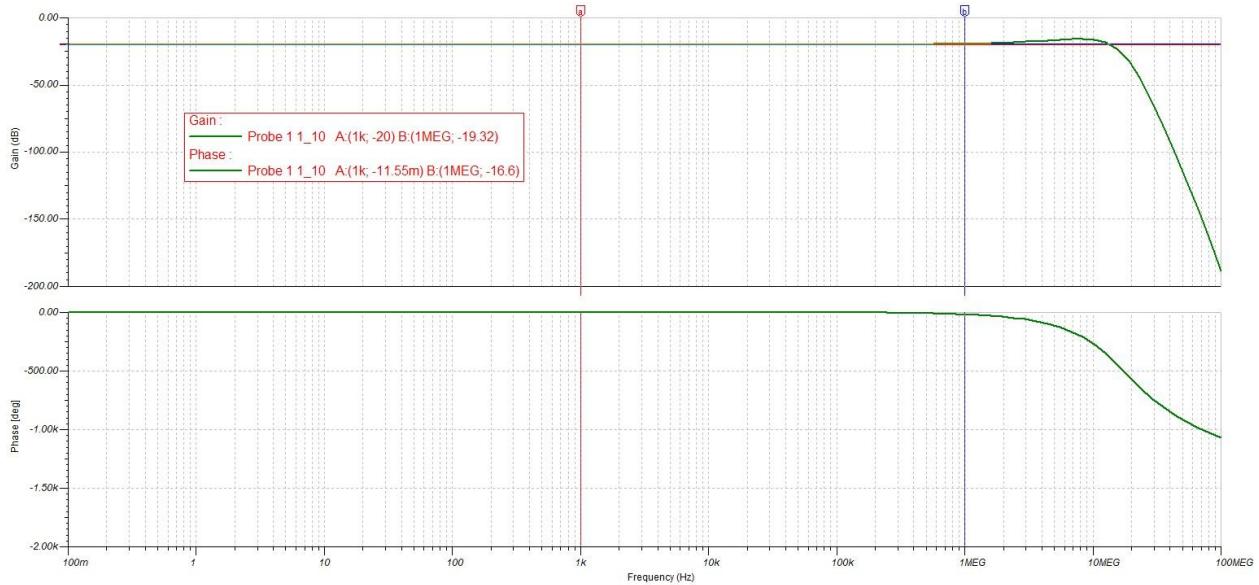


Figure 21. Analog Probe 1:10 Frequency Analysis

<i>Pass Band</i>	<i>Frequency Limit</i>
$G = 10^{\frac{-20}{20}}$	$G = 10^{\frac{-19.32}{20}}$
$G = 0.1$	$G = 0.1081$
$G \approx \frac{1}{10}$	$G \approx \frac{1}{10}$
$\text{Phase Shift} = -0.001155^\circ$	$\text{Phase Shift} = -16.6^\circ$
$\text{Phase Shift} \approx 0^\circ$	

The attenuation was reduced slightly at the frequency limit, but was still relatively close to the voltage division. The phase shift within the passband of the filter was near zero, but the phase at the frequency limit of 1 MHz experienced a significant phase shift. All phase shifts in the DAQ system were relative to the measured phase of the voltage probe, so the displayed signal will be out of phase of the original signal by a significant amount.

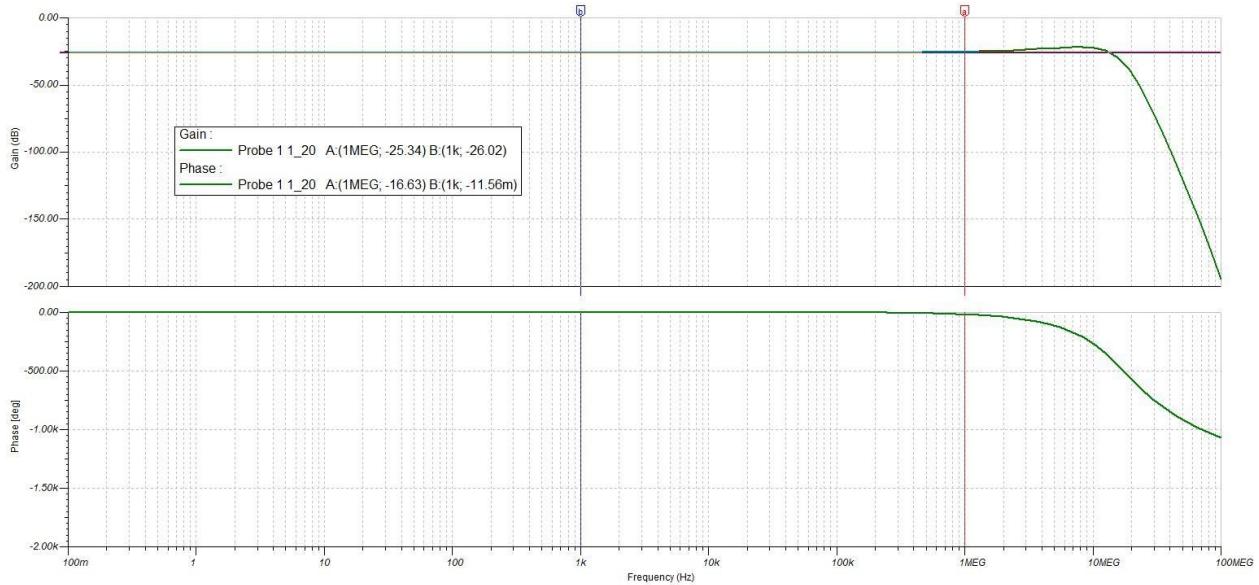


Figure 22. Analog Probe 1:20 Frequency Analysis

<i>Pass Band</i>	<i>Frequency Limit</i>
$G = 10^{\frac{-26.02}{20}}$ $G = 0.050003$ $G \approx \frac{1}{20}$	$G = 10^{\frac{-25.34}{20}}$ $G = 0.054075$ $G \approx \frac{1}{20}$
$Phase\ Shift = -0.001156^\circ$ $Phase\ Shift \approx 0^\circ$	$Phase\ Shift = -16.63^\circ$

The attenuation was reduced slightly at the frequency limit, but was still relatively close to the voltage division. The phase shift within the passband of the filter was near zero, but the phase at the frequency limit of 1 MHz experienced a significant phase shift. All phase shifts in the DAQ system were relative to the measured phase of the voltage probe, so the displayed signal will be out of phase of the original signal by a significant amount.

### 3.2.3 Pass and Invert Operation Verification

The pass and invert operations were verified by performing the pass and invert operations using signals generated from a waveform generator. The pass and invert operations were verified for both Channel 1 and Channel 2. The signal in Channel 1 was a sine wave with an amplitude of 2V and a frequency of 144 kHz. The signal in Channel 2 was a DC signal with a value of 2V.

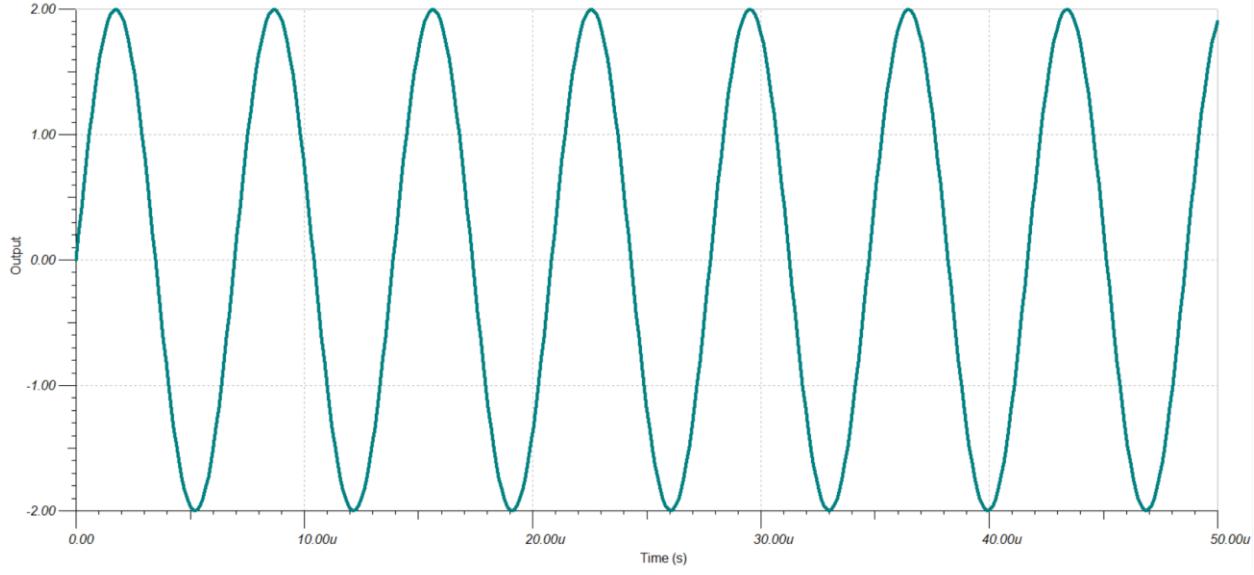


Figure 23. Channel 1 Signal for Pass and Invert Operations

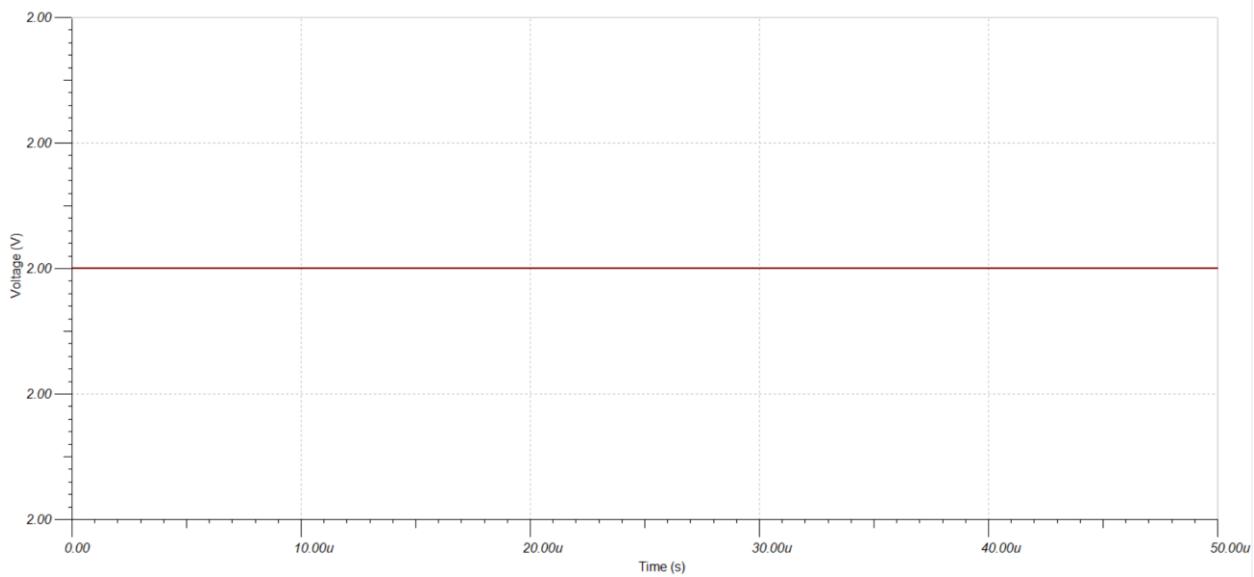


Figure 24. Channel 2 Signal for Pass and Invert Operations

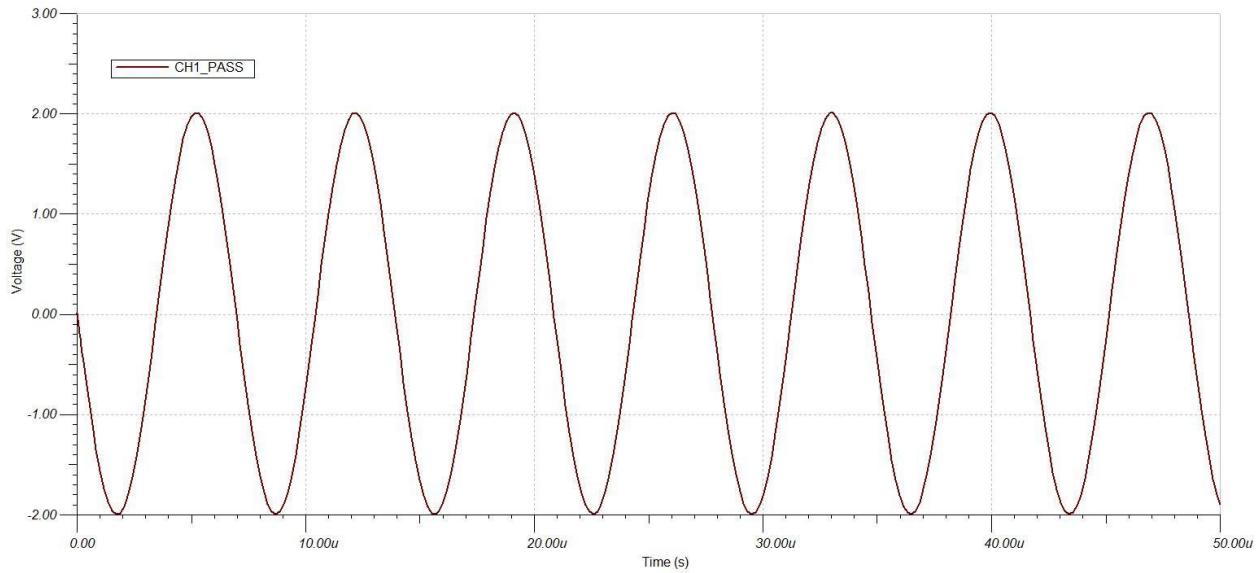


Figure 25. Output of Channel 1 Pass Operation

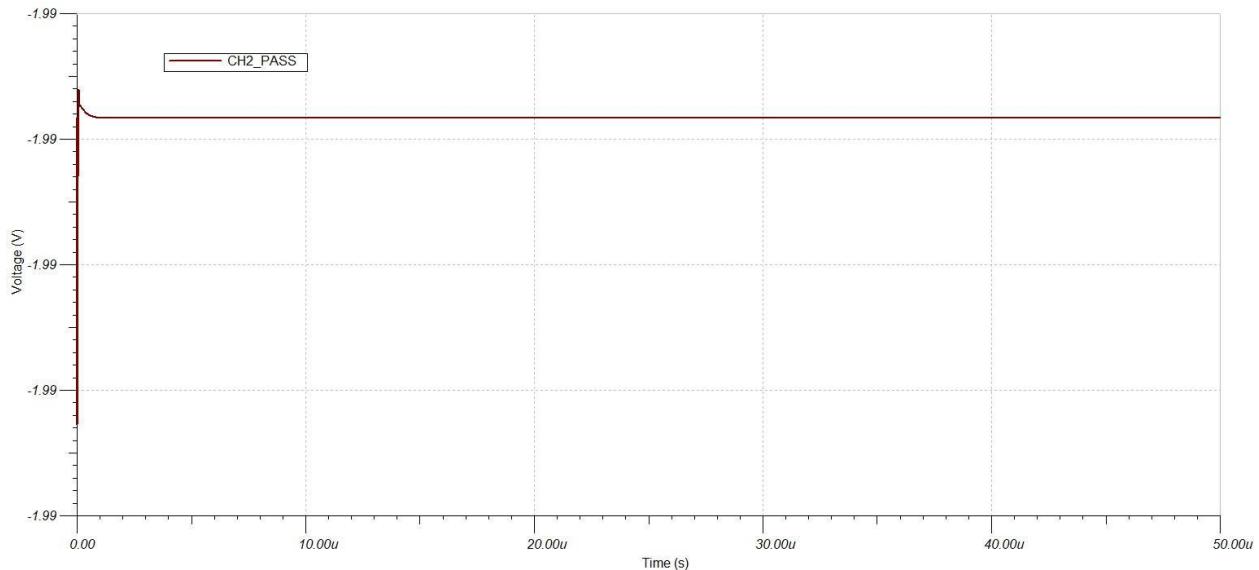


Figure 26. Output of Channel 2 Pass Operation

The channel pass operations were observed to invert the channel signals. The pass operations inverted the channel signals because the signal will be inverted when it was conditioned for the microcontroller.

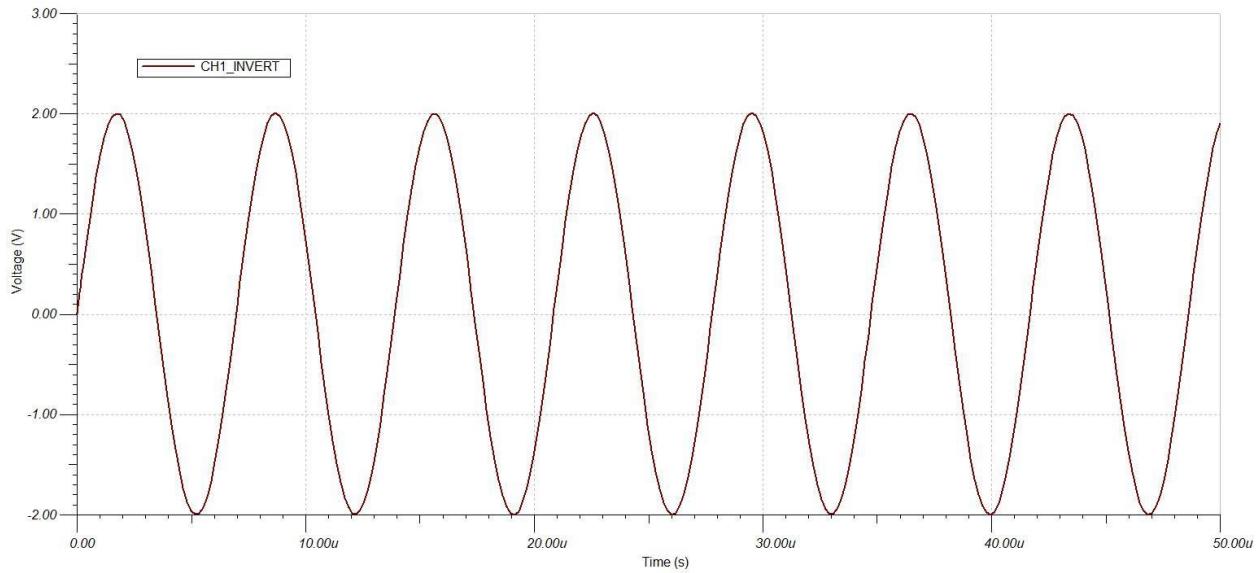


Figure 27. Output of Channel 1 Invert Operation

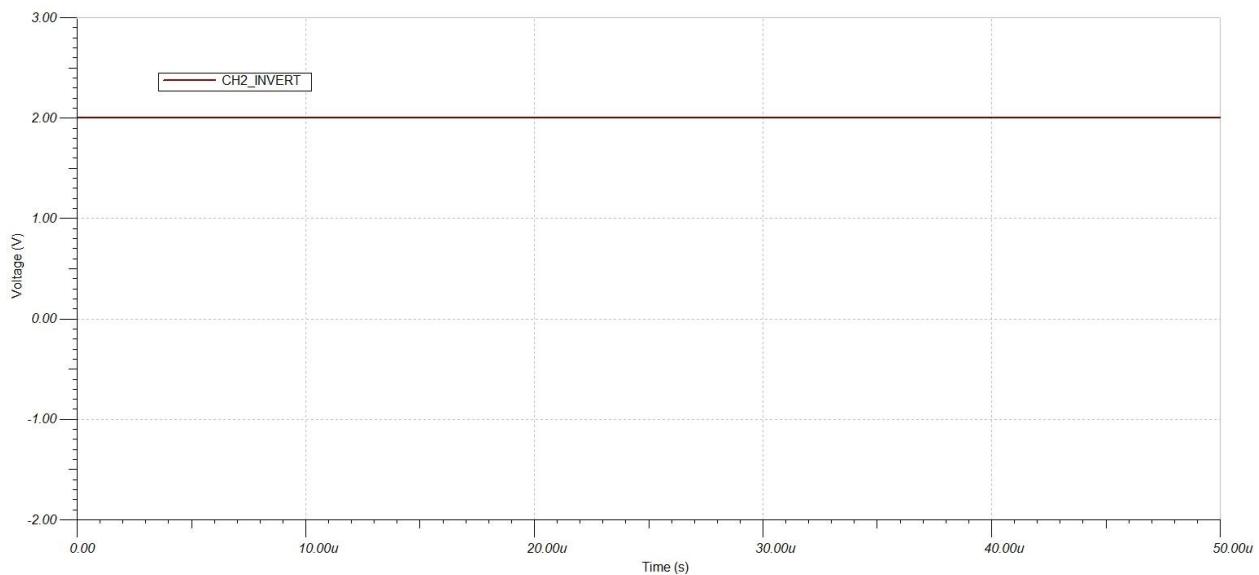


Figure 28. Output of Channel 2 Invert Operation

The channel invert operations were observed to let the channel signals pass without any operation. The invert operation did not invert the channel signals because the signal will be inverted when it was conditioned for the microcontroller.

### 3.2.4 Addition Operation Verification

The addition circuit was verified by adding two signals generated by waveform generators using an inverting summing amplifier. The gain of the two signals was one, so the inverted sum of the two signals was expected at the output. The signal in Channel 1 was a sine wave with an amplitude of  $2V$  with a frequency of  $144\text{ kHz}$ . The signal in Channel 2 was a DC signal with a value of  $2V$ .

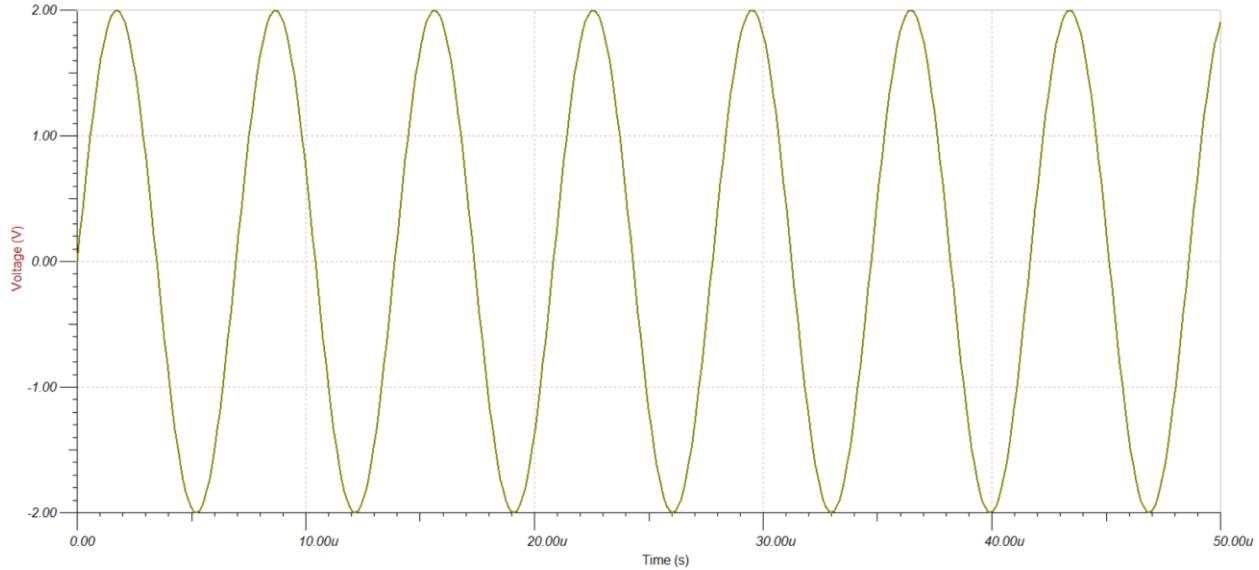


Figure 29. Channel 1 Signal for Inverting Summing Amplifier

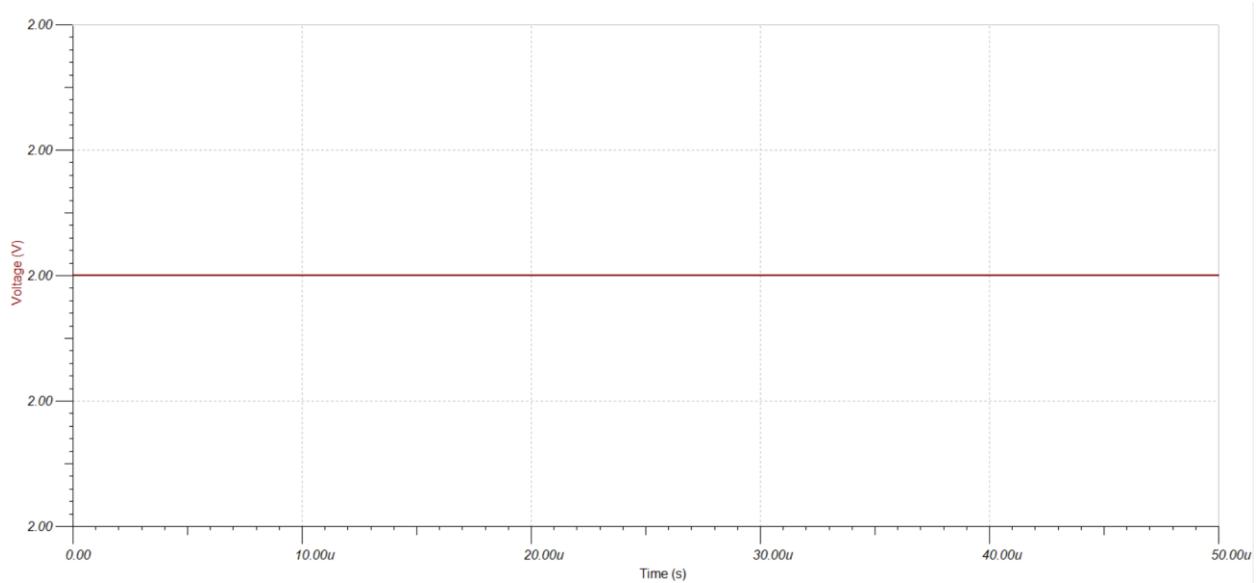


Figure 30. Channel 2 Signal for Inverting Summing Amplifier

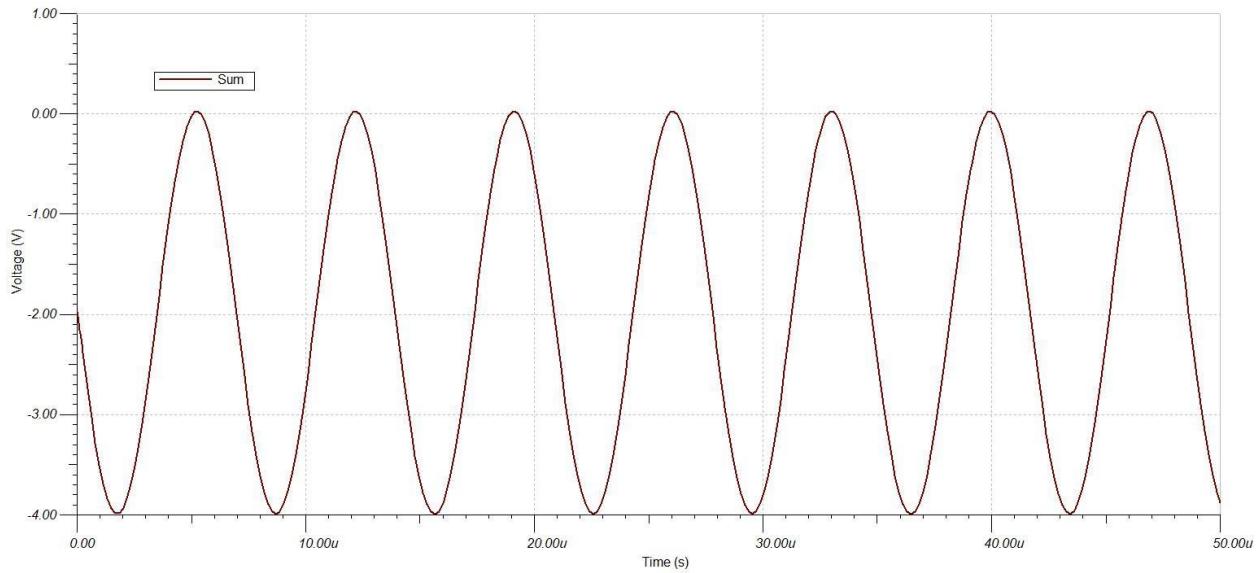


Figure 31. Output of Inverting Summing Amplifier

The summation signal was a negative sine wave with an amplitude of  $2V$  with a DC offset of  $-2V$ . The sum of the signals was observed to be the inverted sum of the signals as expected from an inverting summing amplifier with a gain of one.

### 3.2.5 Subtraction Operation Verification

The subtraction circuit was verified by subtracting two signals generated from waveform generators with a difference amplifier. The gain of the difference amplifier was set to one so the output was expected to be the difference between the two signals with no scaling. The signal in Channel 1 was a sine wave with an amplitude of 2V with a frequency of 144 kHz. The signal in Channel 2 was a DC signal with a value of 2V. The difference amplifier was designed to subtract Channel 1 from Channel 2.

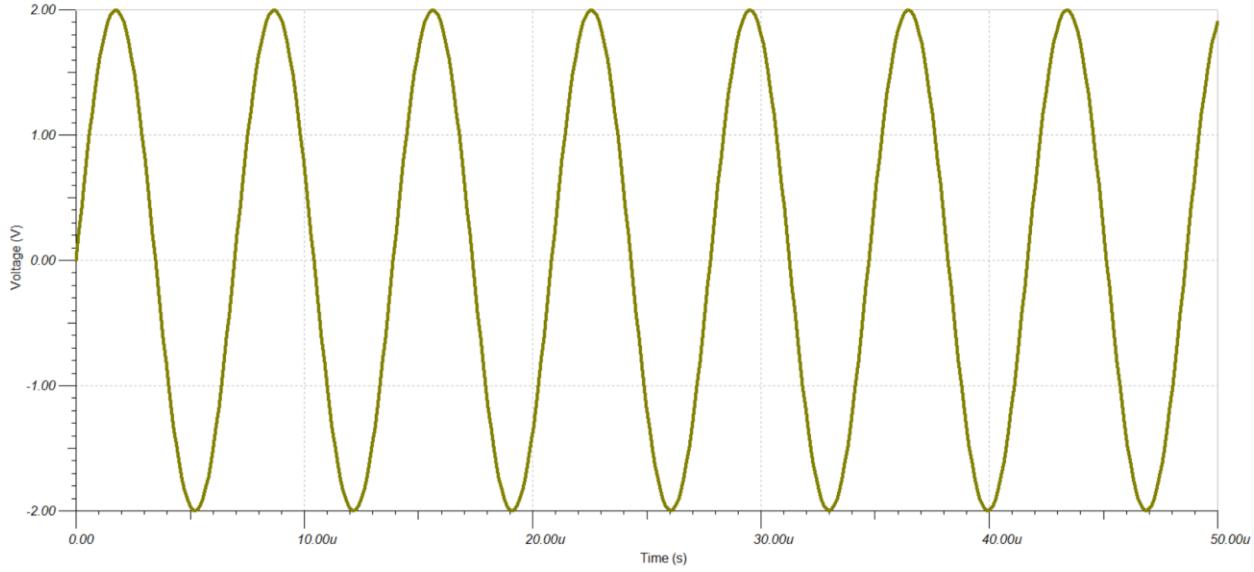


Figure 32. Channel 1 Signal for Difference Amplifier

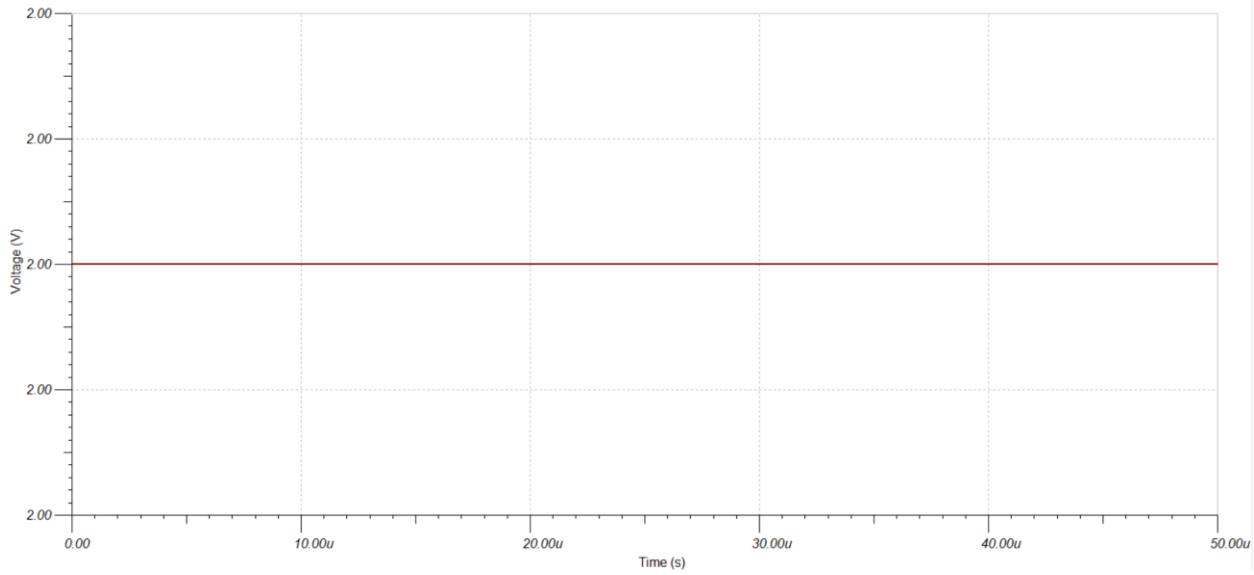


Figure 33. Channel 2 Signal for Difference Amplifier

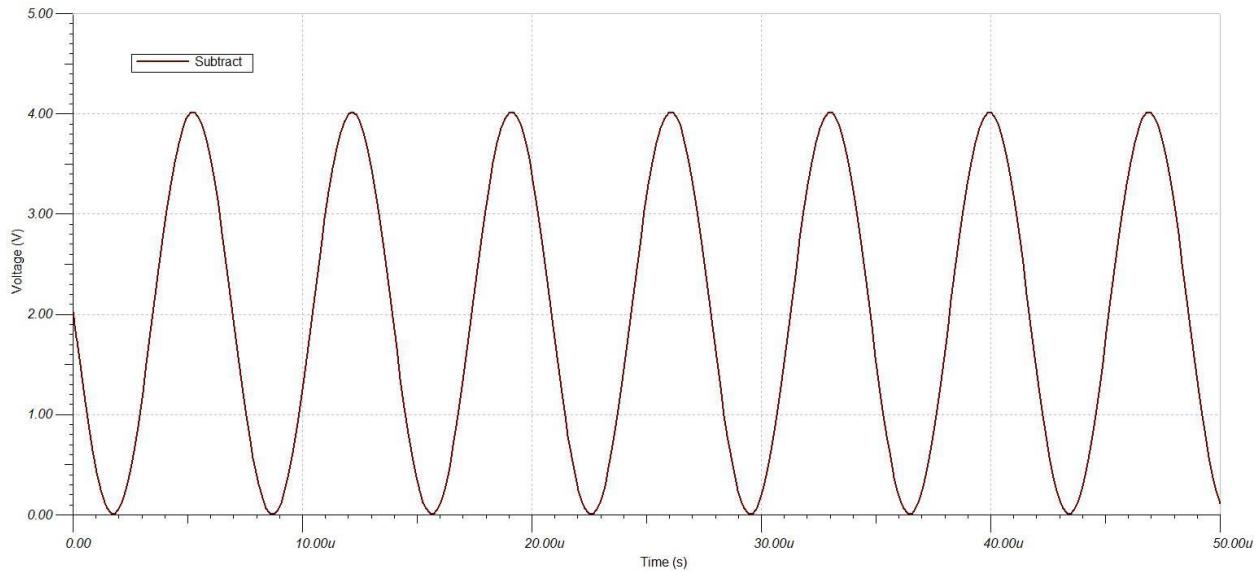


Figure 34. Output of Difference Amplifier

The difference signal was observed to be a negative sine wave with an amplitude of  $2V$  with a DC offset of  $2V$ . The difference signal was concluded to be the difference of the DC offset in Channel 2 with the sine wave in Channel 1.

### 3.2.6 Derivative Operation Verification

The derivative operation was verified by observing the frequency response of all the differentiators in the designed differentiator equalizer. The differentiator equalizer was observed overall as the combination of the separate differentiators and each differentiator was individually analyzed.

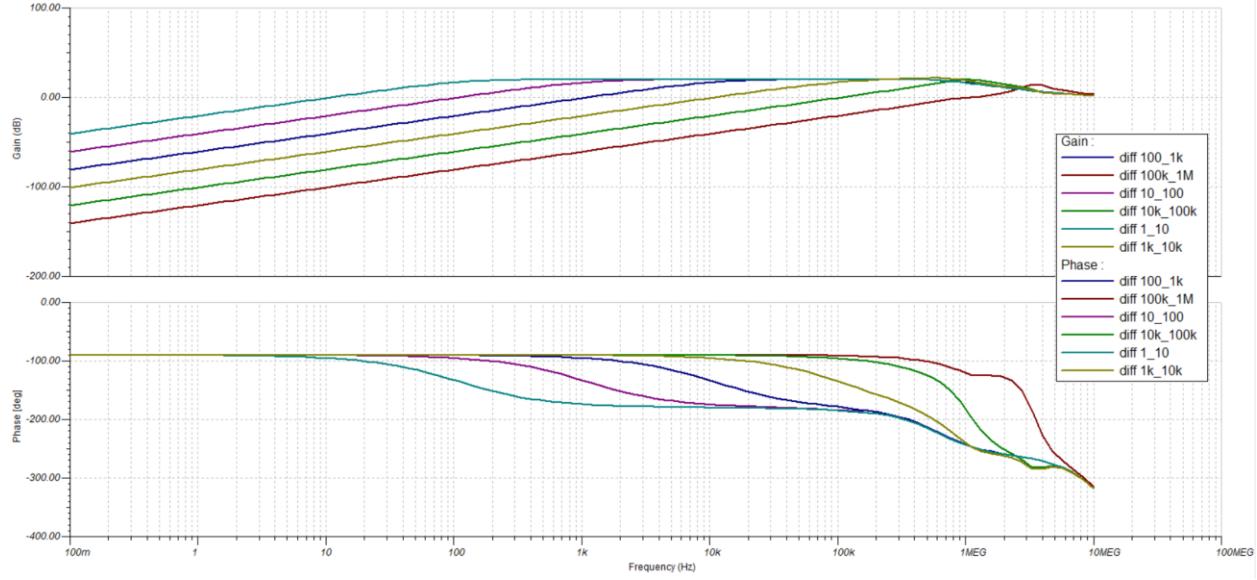


Figure 35. Overall Derivative Equalizer Frequency Response

The overall differentiator equalizer was observed to be multiple high pass filters. Each equalizer had only one decade of interest. The phase of differentiator was observed to be consistently around  $-90^\circ$ . The derivative of a sine wave was a positive cosine wave. A phase shift of  $-90^\circ$  shifted a sine wave to be a negative cosine wave. The result was inverted because the differentiators used negative feedback which inverted the signal.

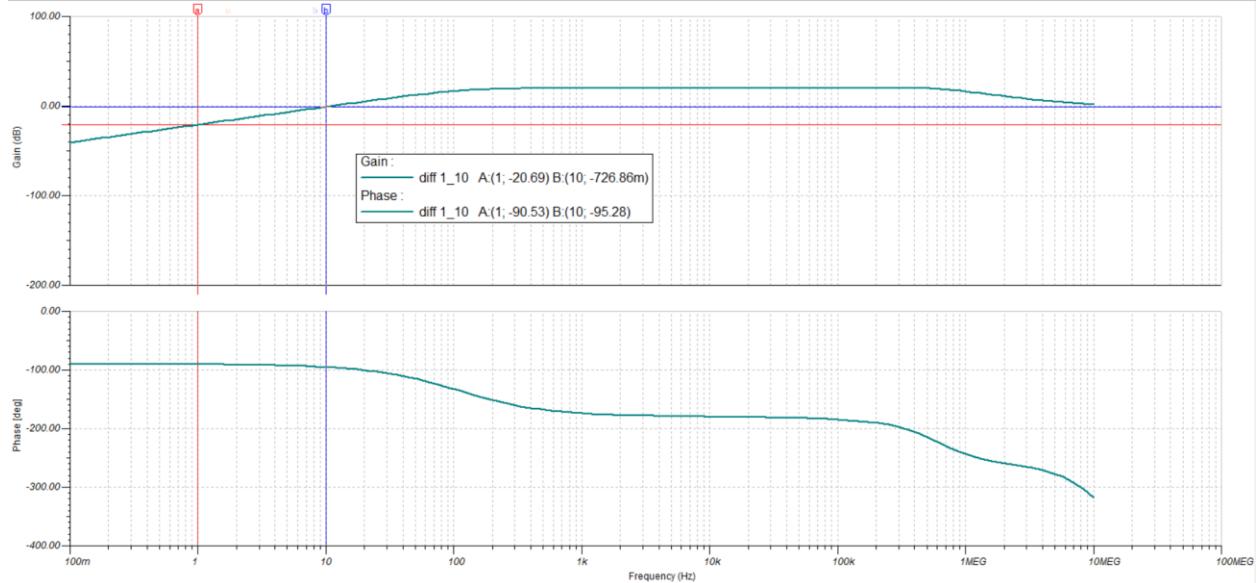


Figure 36. Differentiator 1Hz to 10Hz Frequency Response

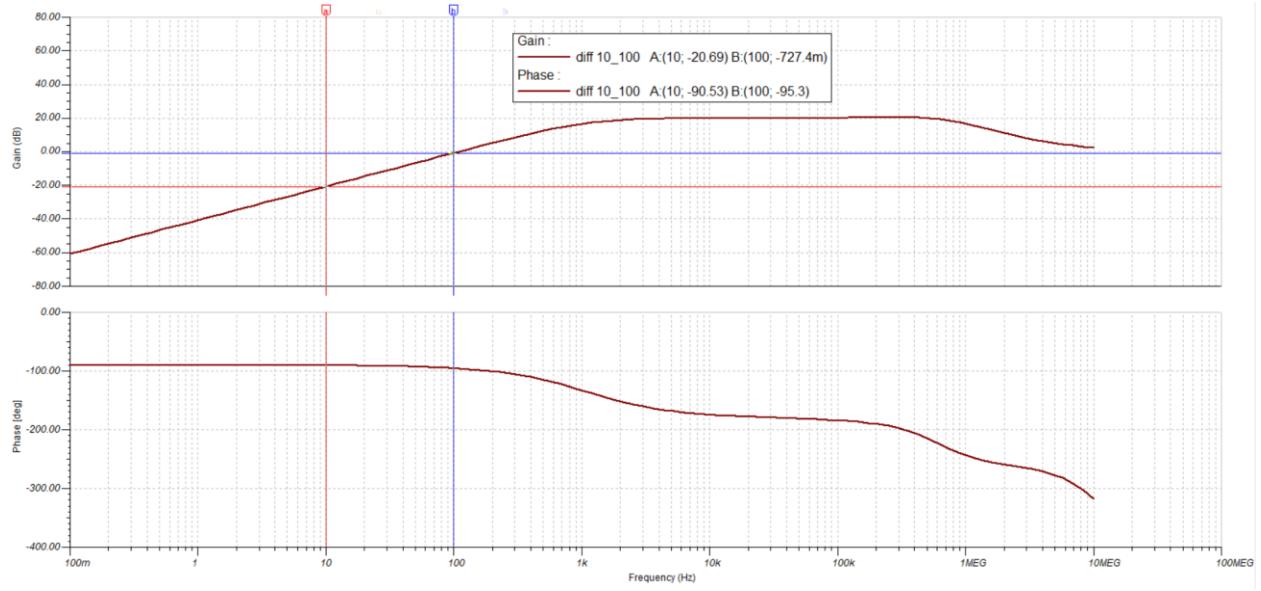


Figure 37. Differentiator 10Hz to 100Hz Frequency Response

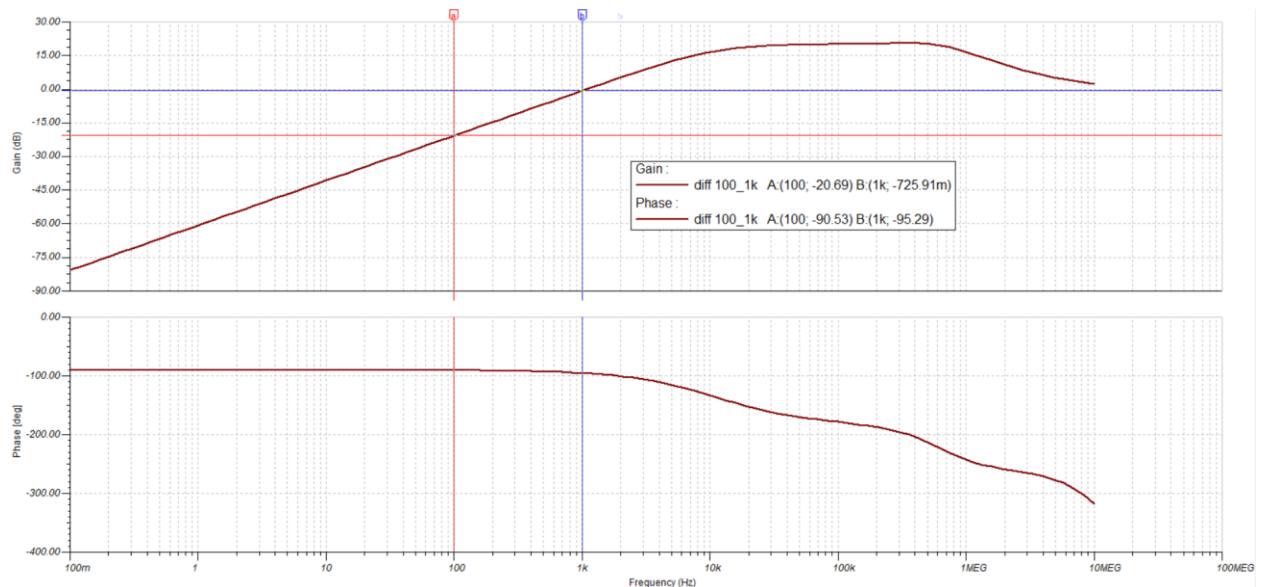


Figure 38. Differentiator 100Hz to 1kHz Frequency Response

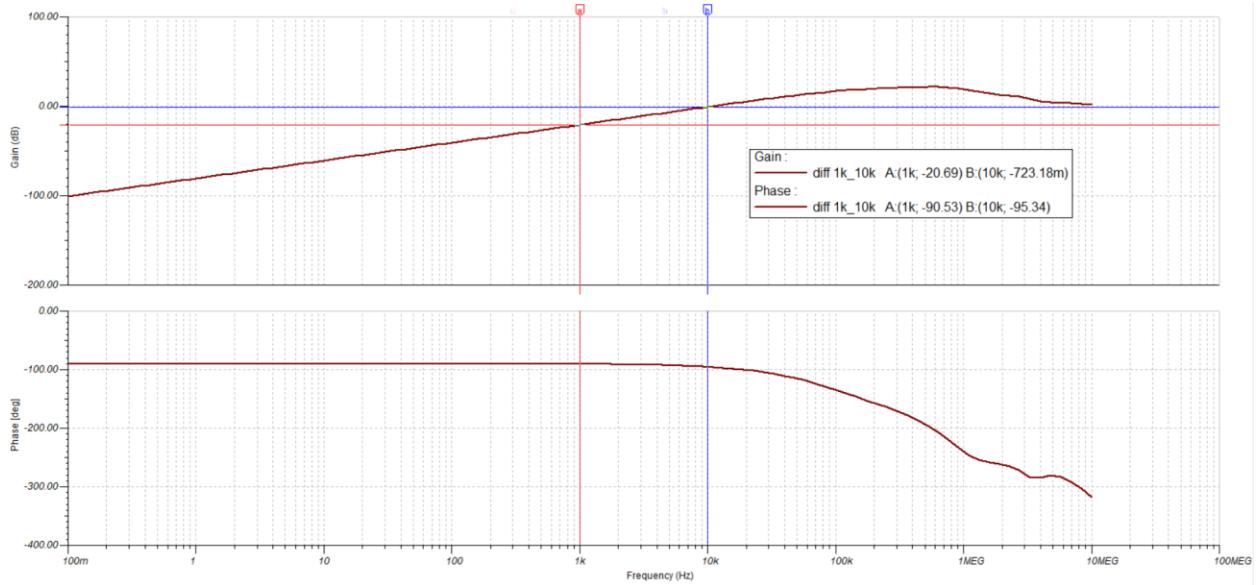


Figure 39. Differentiator 1kHz to 10kHz Frequency Response

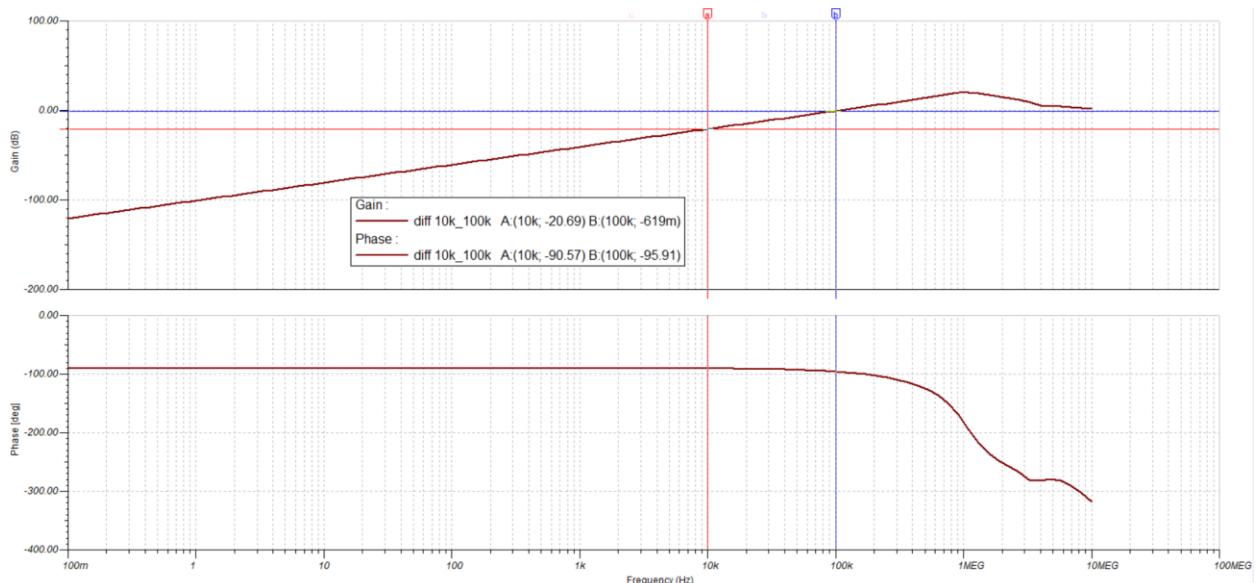


Figure 40. Differentiator 10kHz to 100kHz Frequency Response

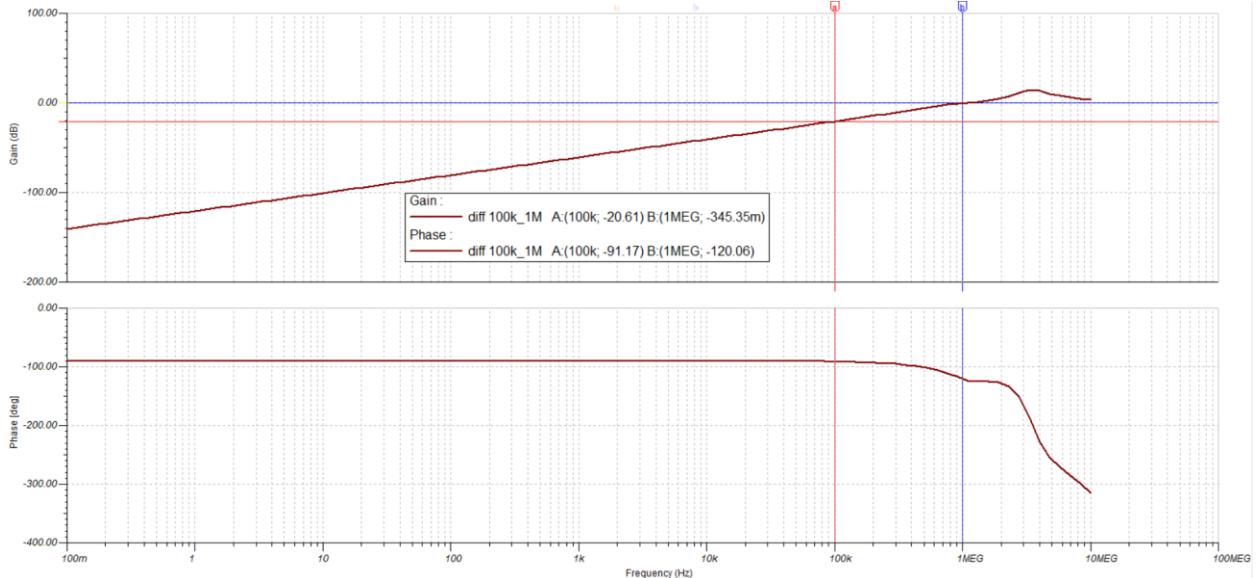


Figure 41. Differentiator 100kHz to 1MHz Frequency Response

The differentiators for each frequency range were analyzed in detail separately. The analysis showed that at the lower end of the frequency range of the differentiator, the signal was attenuated by approximately  $-20\text{ dB}$ . The signal was attenuated by approximately  $0\text{ dB}$  at the higher end of the frequency range. The phase shift at the lower end of the frequency range was approximately  $-90^\circ$  and the phase shift at the upper end of the frequency range was approximately  $-95^\circ$ . It was concluded that the differentiator attenuated signals more at the lower end of the frequency range but the signal was closer to a  $90^\circ$  phase shift for differentiation.

The differentiator from the range of  $100\text{ kHz}$  to  $1\text{ MHz}$  was observed to be different from the other differentiators. The differentiator for the highest frequency range was observed to have the same gain as the other differentiators, approximately  $-20\text{ dB}$  at the lower range and  $0\text{ dB}$  at the upper range. The phase of the differentiator was observed to not be consistent at the highest range. The phase shift at the lower range was  $-91.17^\circ$  which was still approximately  $-90^\circ$ . The phase shift at the upper range was  $-120.06^\circ$ . An additional phase shift of around  $-30^\circ$  was observed at the output. The additional phase shift will cause the differentiator to be out of phase of the measured probe signal.

### 3.2.7 Integration Operation Verification

The integration operation was verified by observing the frequency response of all the integrators in the designed integration equalizer. The integration equalizer was observed overall as the combination of all the integrators and each integrator was individually analyzed.

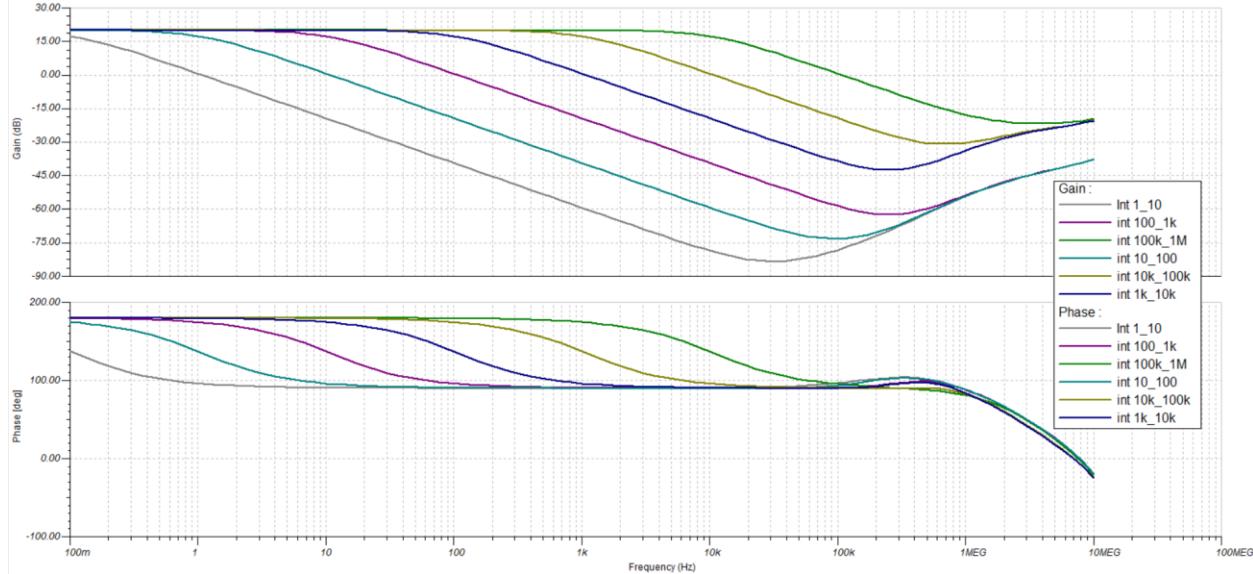


Figure 42. Overall Integration Equalizer Frequency Response

The overall integration equalizer was observed to be low pass filters. Each integrator had only one decade of interest. The phase of differentiator was observed to be consistently around  $90^\circ$ . The integral of a sine wave was a negative cosine wave. A phase shift of  $90^\circ$  shifted a sine wave to be a positive cosine wave. The result was inverted because the differentiators used negative feedback which inverted the signal. The signal will be inverted to the correct signal when it was conditioned for the microcontroller.

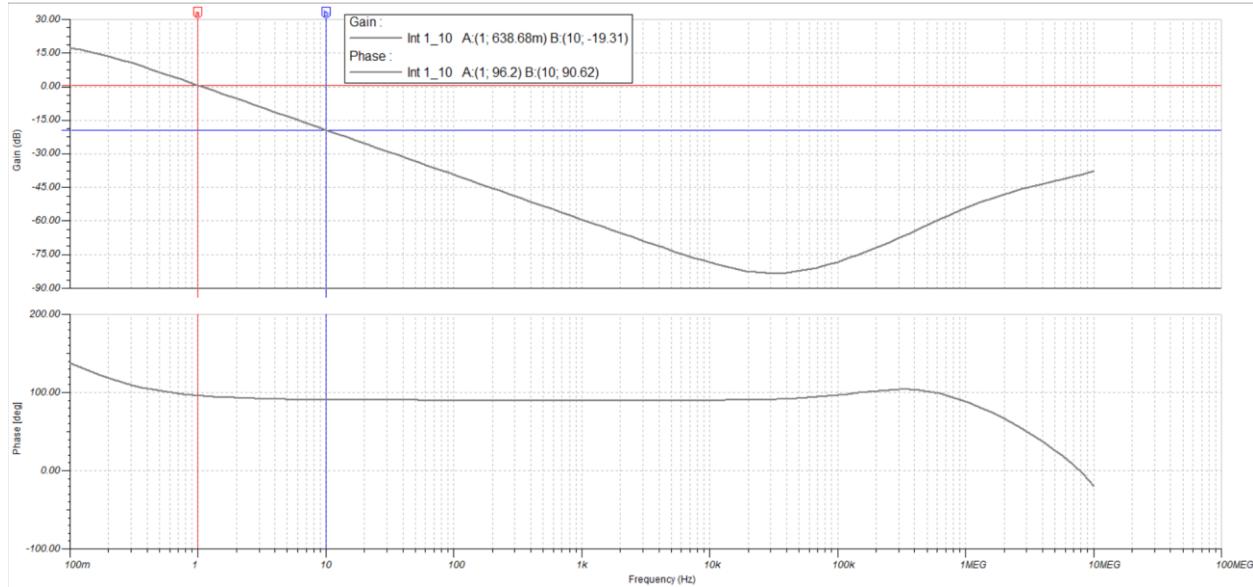


Figure 43. Integrator 1Hz to 10Hz Frequency Response

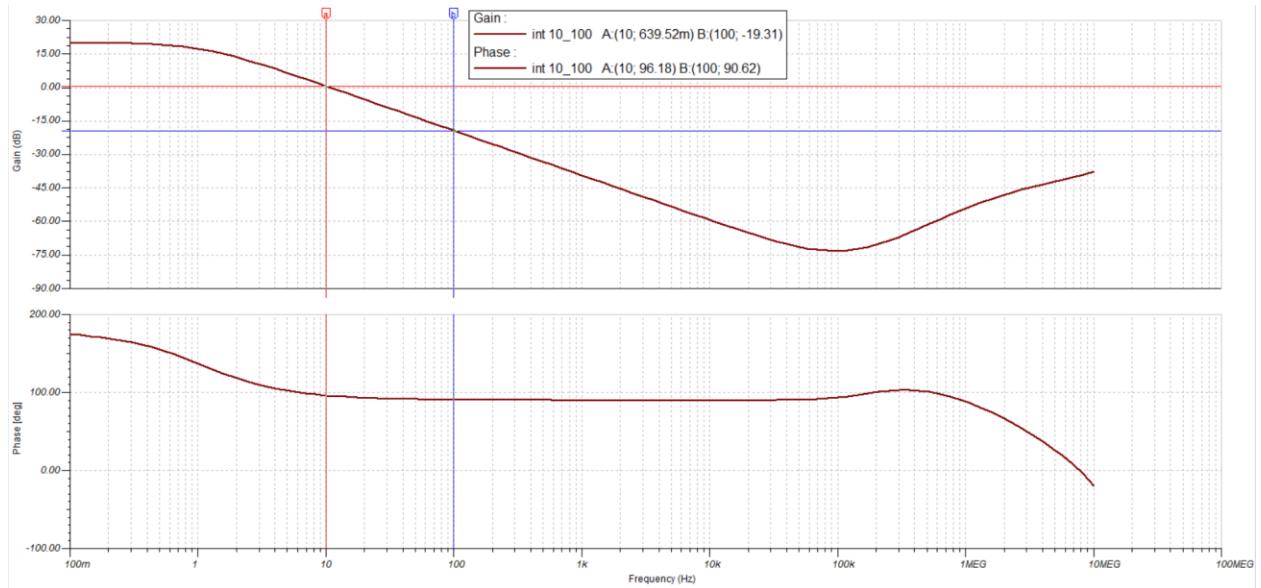


Figure 44. Integrator 10Hz to 100Hz Frequency Response

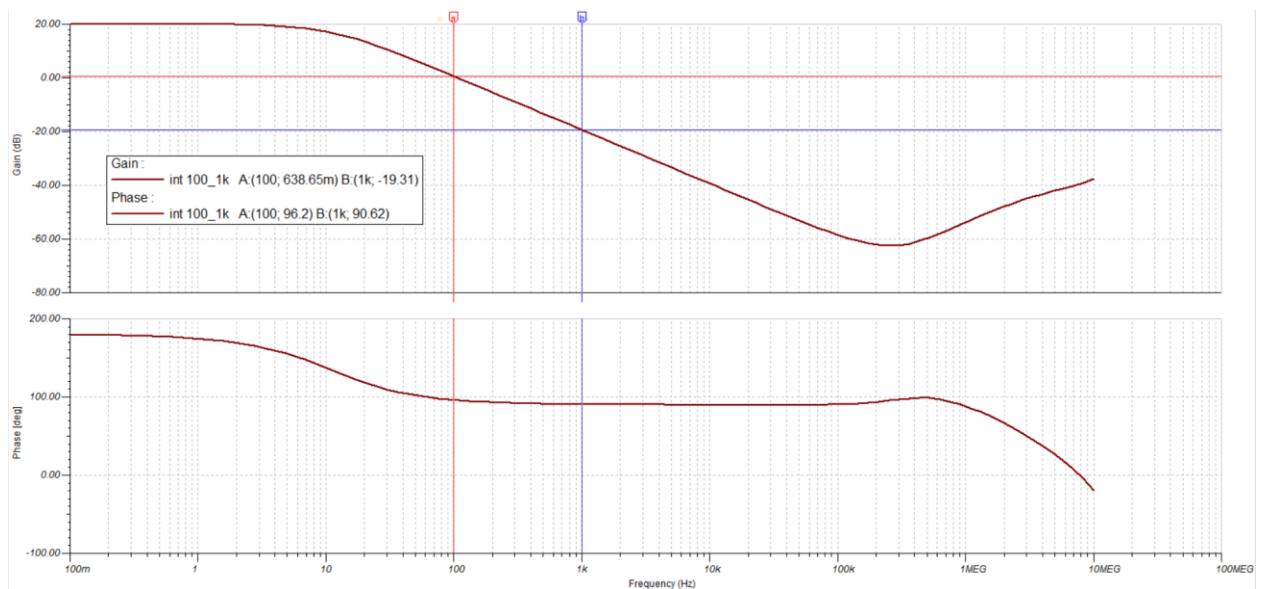


Figure 45. Integrator 100Hz to 1kHz Frequency Response

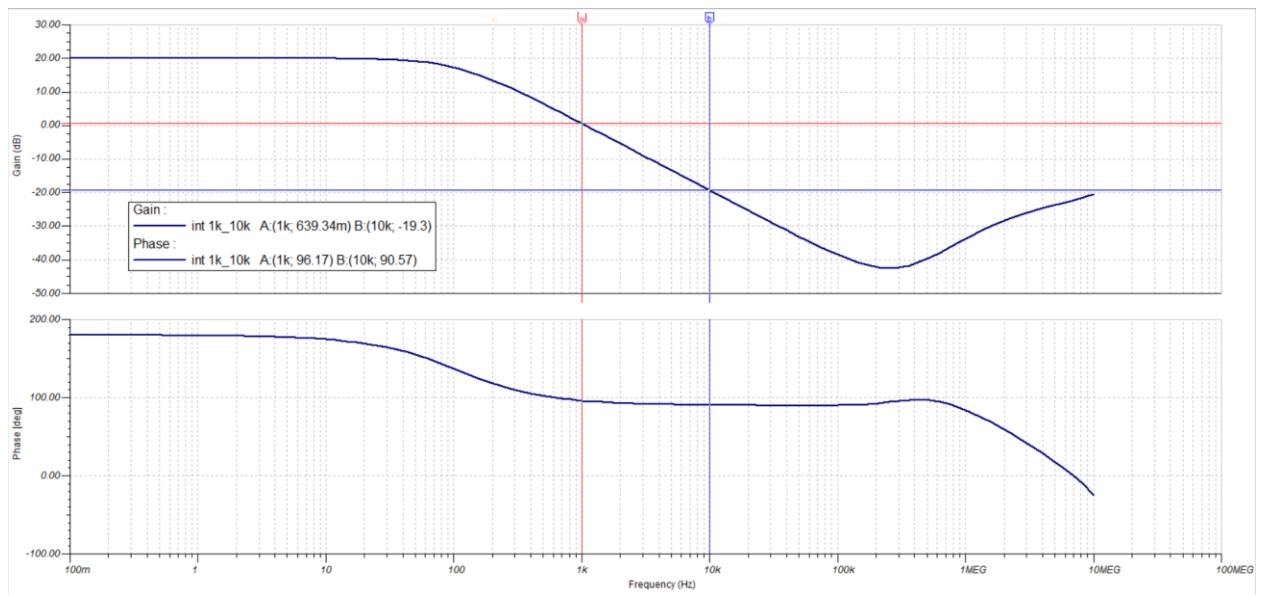


Figure 46. Integrator 1kHz to 10kHz Frequency Response

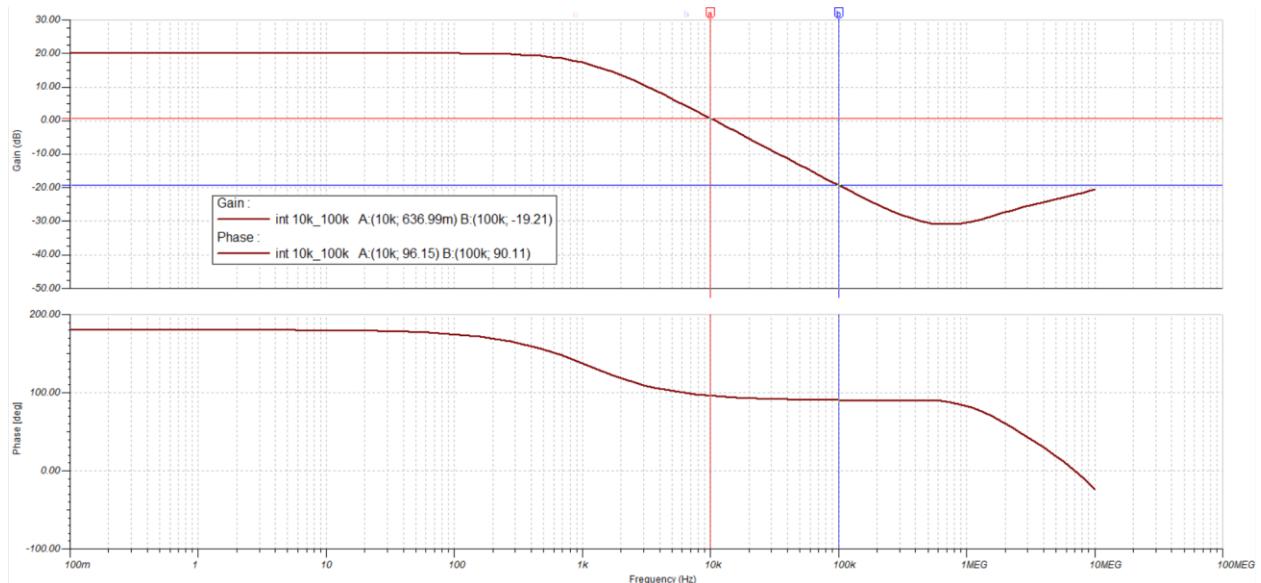


Figure 47. Integrator 10kHz to 100kHz Frequency Response

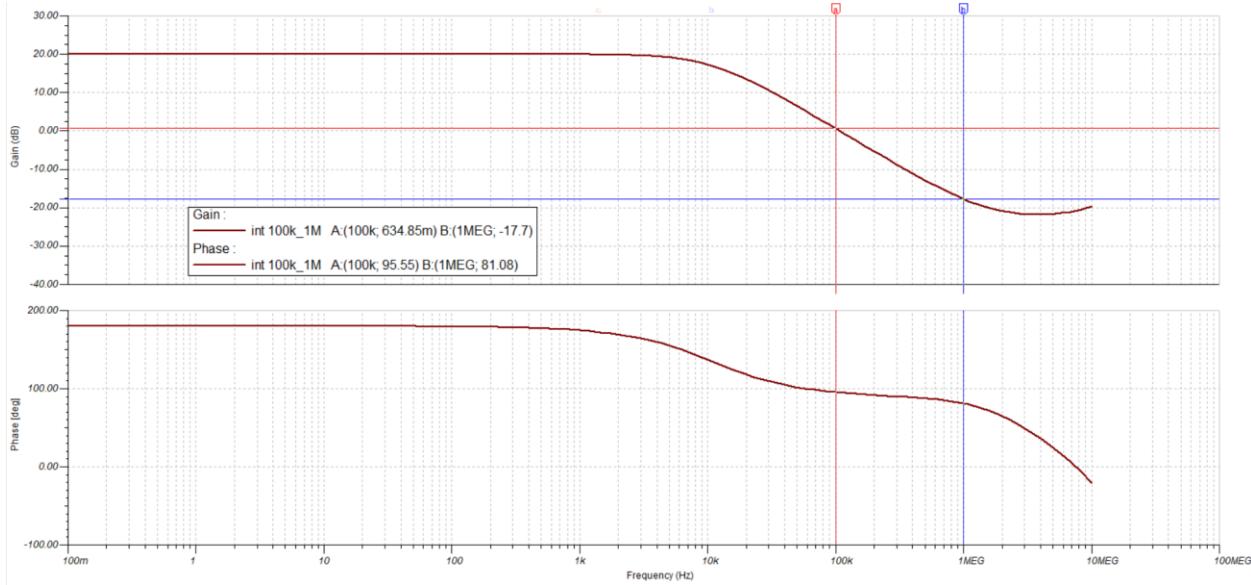


Figure 48. Integrator 100kHz to 1MHz Frequency Response

The integrators for each frequency decade were analyzed in detail separately. The analysis showed that at the lower end of the frequency range of the differentiator, the signal was attenuated by approximately 0 dB. The signal was attenuated by approximately  $-20\text{dB}$  at the higher end of the frequency range. The phase shift at the lower end of the frequency range was approximately  $95^\circ$  and the phase shift at the upper end of the frequency range was approximately  $90^\circ$ . It was concluded that the integrator attenuated signals more at the higher end of the frequency range but the signal was closer to a  $90^\circ$  phase shift for integration.

The integrator from the range of  $100\text{ kHz}$  to  $1\text{ MHz}$  was observed to be different from the other differentiators. The integrator for the highest frequency range was observed to attenuate the signal by 0 dB at the lower range but attenuated the signal by only  $-17.7\text{ dB}$  at the upper frequency range. The phase of the integrator was also observed to not be consistent at the highest range. The phase shift at the lower range was  $95.55^\circ$  which was still approximately  $90^\circ$ . The phase shift at the upper range was  $81.08^\circ$ . The integrator did not shift the signal by a complete  $90^\circ$  to integrate the signal. The different phase shift will cause the differentiator to be out of phase of the measured probe signal.

### 3.2.8 Microcontroller Conditioning Verification

The microcontroller conditioning circuit was verified by performing a transient analysis on a sine wave generated by a waveform generator. The sine wave had an amplitude of  $2V$  and a frequency of  $144\text{ kHz}$ . The simulated sine wave represented a typical signal the microcontroller conditioning circuit operated on within the range of  $\pm 5V$  with a frequency up to  $1\text{ MHz}$ .

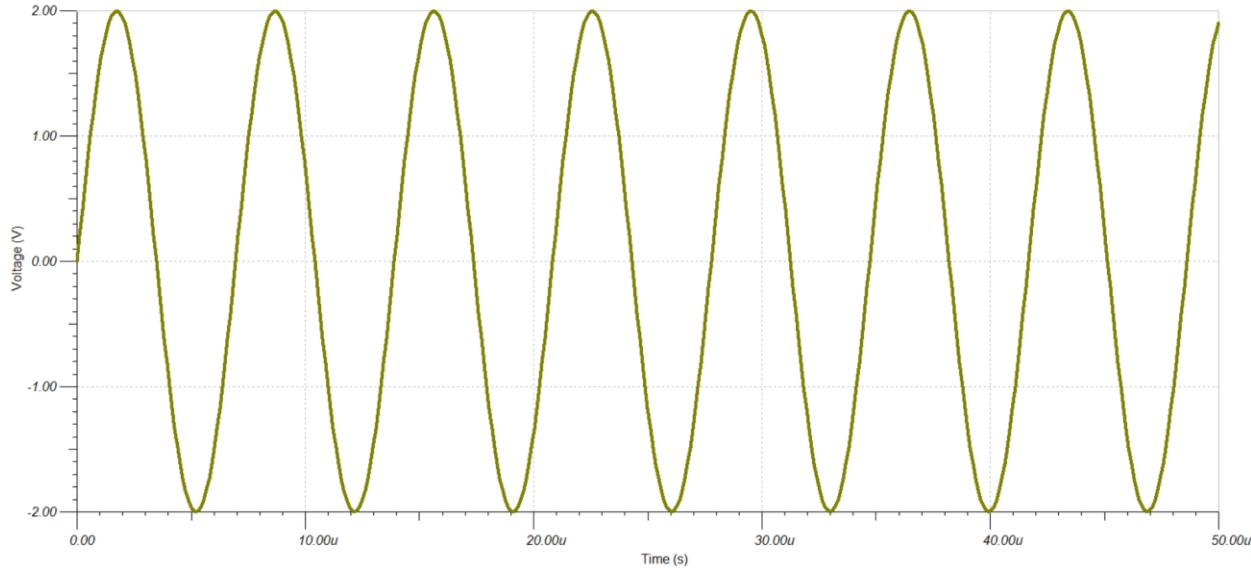


Figure 49. Operation Select Signal for Microcontroller Conditioning

The offset signal represented the tested signal after applying the  $-5V$  offset using an inverting summing amplifier. The waveform was observed to be offset by a positive  $5V$  because the offset was inverted. The sine wave was observed to be negative because of the inverting summing amplifier. The inverting summing amplifier had a gain of one, so the amplitude of the sine wave did not change. The signal was observed to have a large magnitude that the microcontroller cannot read.

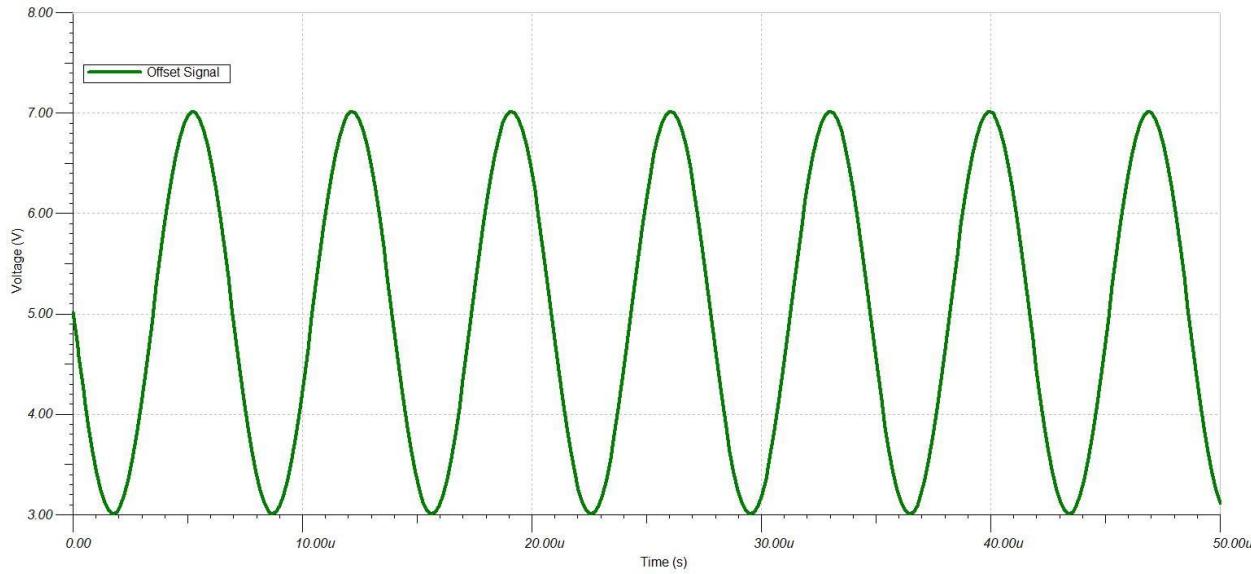


Figure 50. Offset Signal for Microcontroller Conditioning

The scaled signal represented the tested signal after applying a scaling factor of 0.1 using an inverting amplifier. The waveform was observed to be between 0 and  $-1V$ . The magnitude of the signal was correct but the signal was negative because of the inversion caused by the inverting amplifier. The sine wave was observed to be positive again after being inverted.

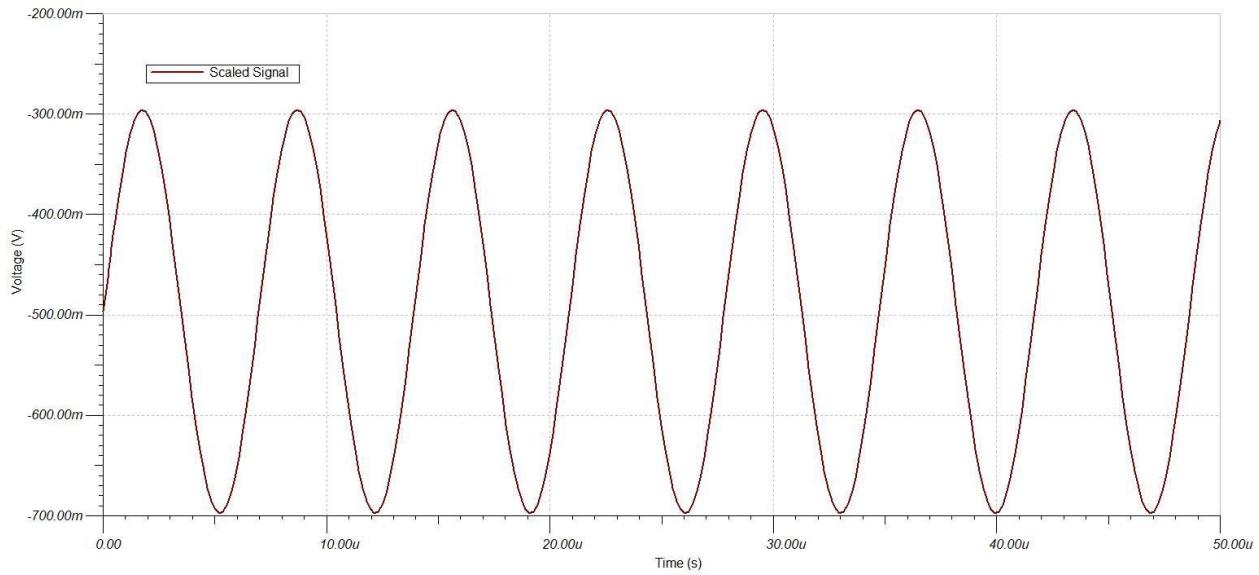


Figure 51. Scaled Signal for Microcontroller Conditioning

The microcontroller signal represented the tested signal after it was inverted using an inverting buffer with a gain of one. The waveform was observed to be within the microcontroller voltage range from  $0V$  to  $2V$ , so the signal can be read by the microcontroller. The sine wave itself was observed to be inverted from the original sine wave input. The microcontroller conditioning circuit will invert the signal at the output, so all the operations performed by the analog DAQ system left the output inverted so that it will be corrected by the microcontroller conditioning circuit.

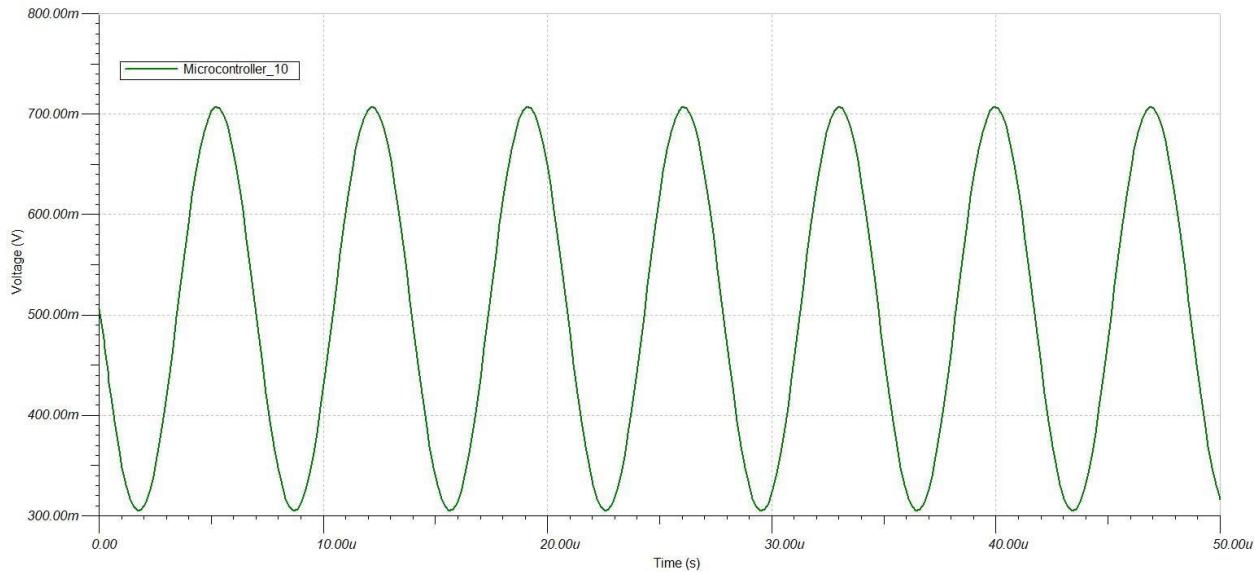


Figure 52. Output Signal for Microcontroller Conditioning

### 3.2.9 Digital Probe Verification

The digital input of the DAQ system was verified by performing a transient response test using a square wave from a waveform generator to simulate a digital signal. The square wave used to simulate a digital signal was a non-return to zero wave (NRZ) that alternated between  $\pm 20V$  at a frequency of  $88\text{ kHz}$ .

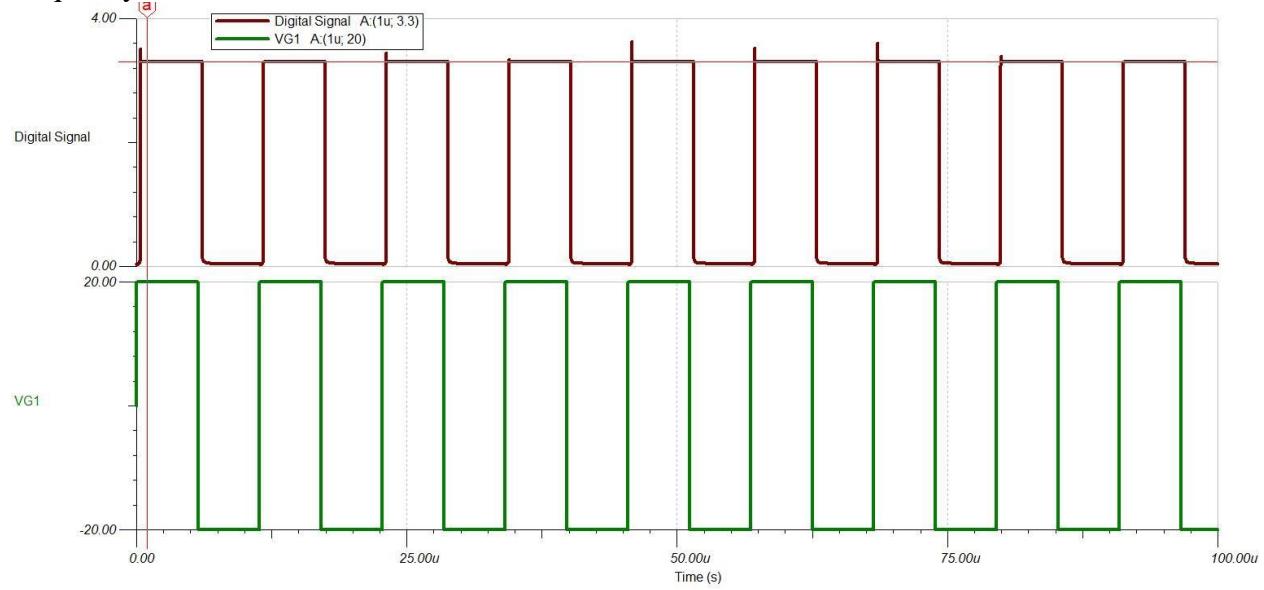


Figure 53. Digital Input Signal Conditioning

The input square wave was observed to have an amplitude larger than the system voltage of  $\pm 12V$ . The digital signal observed at the output was a return to zero wave (RZ) with an amplitude of  $3.3V$ . The digital input circuit was observed to regulate the high voltage digital signal and convert it to a low voltage signal that the microcontroller can read. A small delay was observed between the input signal and the digital signal.

### 3.2.10 Test Procedure

The DAQ system was tested for a variety of different signals at different amplitudes and frequencies. The digital input circuit was a stand-alone circuit, so it was tested for during the individual circuit verification. The analog input section was a system of individually tested circuits. The analog system was verified by measuring a signal and exporting and importing the signal through all of the circuits to observe how the signal was operated by the DAQ analog system.

The signals were measured in the analogue input circuit. Here is where the signal gets generated from. The signal for our purposes was set to Triangle, Sine, and DC. Triangle and sine waves were tested at 1k, 10k and 253k Hz, each with the voltages at 10, 20, and 50 volts. Once the source was set to the desired simulation parameters the signal was measured using three voltage division circuits. The voltage division circuits divided the input circuit by 5, 10, and 20. The sample analog probe circuit showed two of the four analog probes so a total of 6 voltage waveforms, 3 from each probe, were observed at the output. The waveforms were exported as a text file to be imported to the next circuit. Before the text file was imported into the next circuit, it was formatted using an Excel macro. The excel macro split the file so that each voltage

waveform was saved as a separate file to be imported. TINA can only read tab delimited files, so the files must be saved as tab delimited files to be imported.

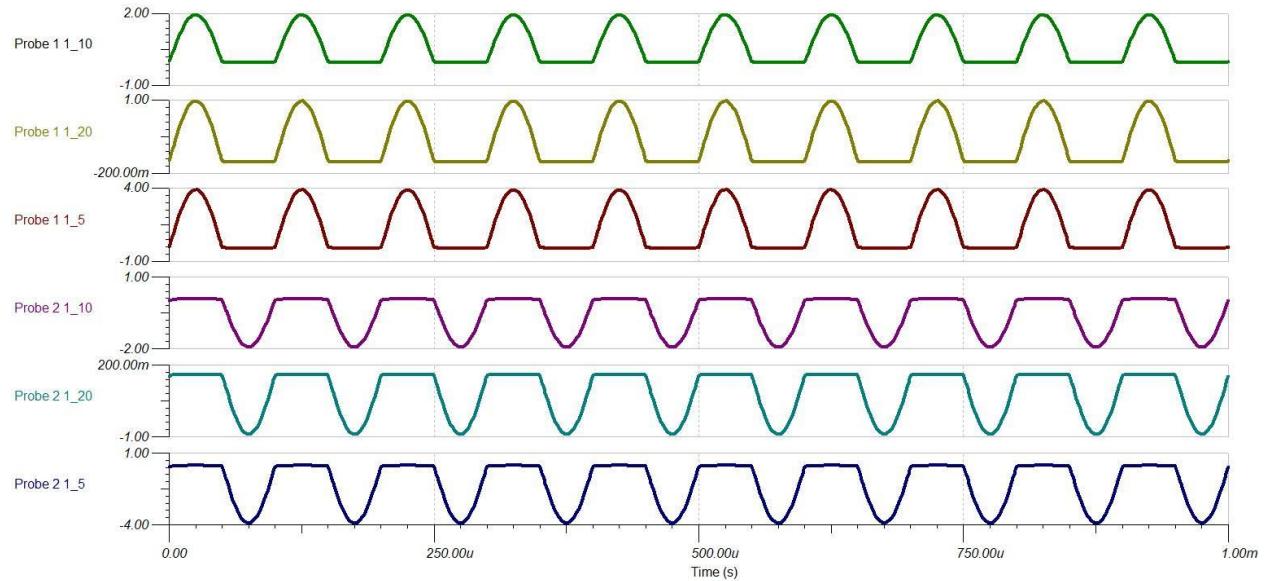


Figure 54. Voltage Probe Outputs

The voltage select stage will select which of the voltage divider waveforms to measure. The voltage select stage will select the same voltage division for both probes in the circuit. The voltage division was selected from divide by 5, 10, or 20 by using an 8 to 1 analog mux for each probe. The outputs of the analog probe were exported as a text document, the TINA simulation always generate 10 times as many output points as input points. A macro was run to split the voltage divider for each probe into separate files and decrease the number of samples by a factor of 10 so that the number of output points equaled the number of input points.

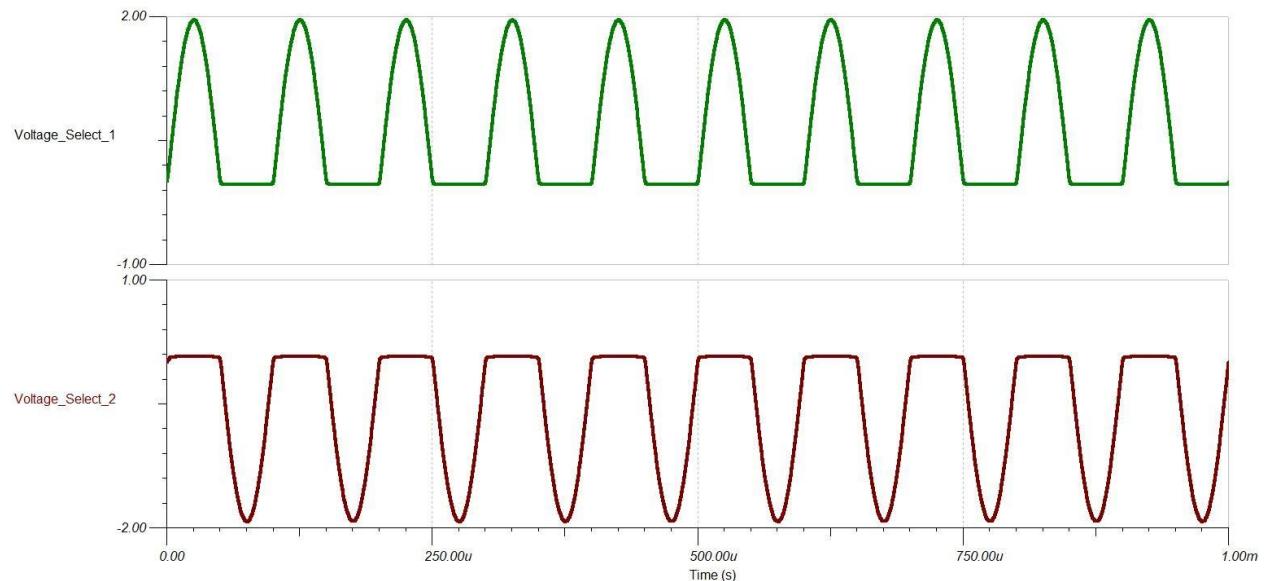


Figure 55. Voltage Select Outputs

The DAQ system was capable of measuring 4 different analog signals with 4 different analog probes, but was only able to operate on two probes at a time. The channel select circuit was designed to select which signals to use. The circuit generated two outputs: one for channel 1 and one for channel 2. The probe selected for each channel was independent, so the same probe can be selected for both channels if desired. The two selected probes were exported as text files. The Excel macro was run to split the two channel signals into separate files and reduce the number of samples by 10.

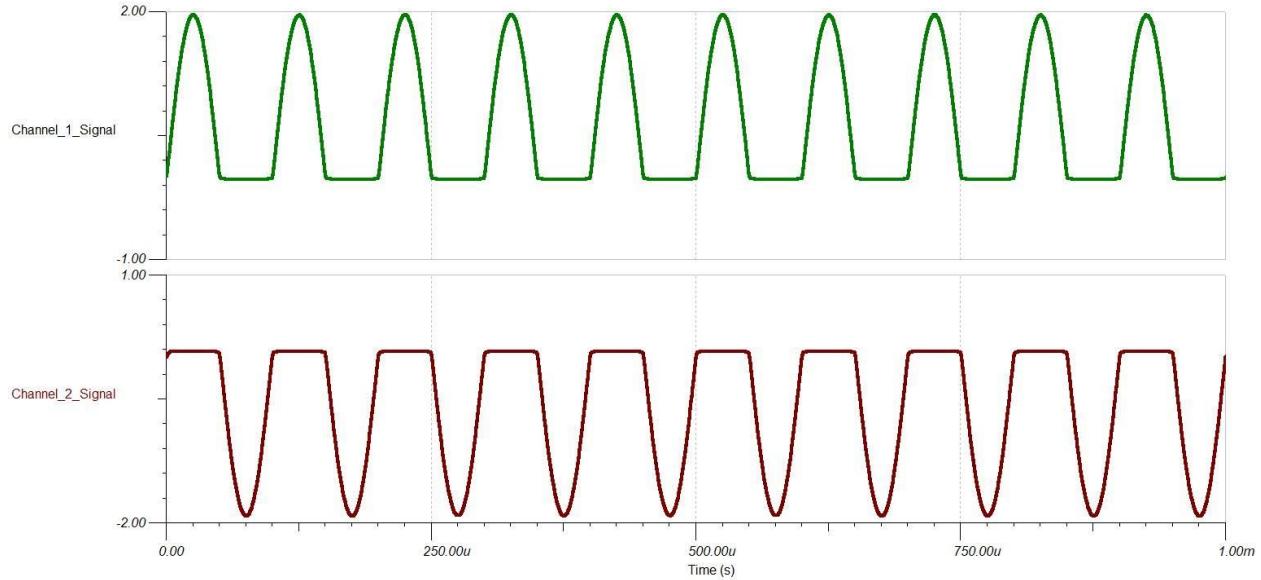


Figure 56. Channel Select Outputs

The DAQ performed all operations in parallel using analog circuits. The desired operation was selected using an analog multiplexer. The different operations included pass and invert operations, addition, subtraction, differentiation, and integration. The add and subtract operations required both channel signals. The other operations required only one signal. The signal selected for channel 1 was used for the signal channel operations.

The pass and inversion operation would simply let the signal through or invert it. Looking at the circuit itself, the operations would look reversed. The signal will be inverted at the end, so they will be corrected. The channel signals were imported into the waveform generators and the circuit was simulated. The circuit generated four output waveforms for the different pass and invert operations on both channels. The signals were exported as text files and the macro was run to split the waveforms and reduce the number of samples by 10.

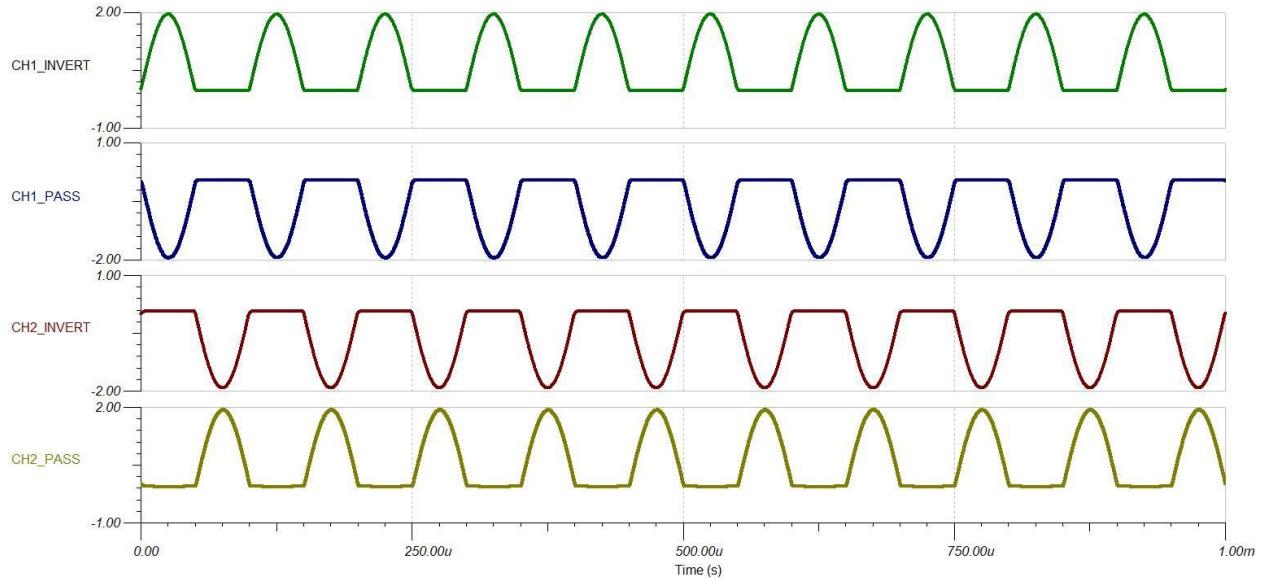


Figure 57. Pass and Invert Outputs

The addition and subtraction circuits were two separate files but operated similarly. Both operations were two signal operations so the signals in channel 1 and channel 2 were used. The addition circuit was an inverted summing amplifier which added and inverted the two signals. The subtraction circuit was a difference amplifier, where channel 2 was subtracted from channel 1. It appeared backwards but the subtraction signal will also be inverted at the end to correct the signal. The addition and subtraction circuits only generated one signal, but the signals must still be exported as text files. The filter macro must still be run to reduce the number of samples by 10 even if there were no signals to split.

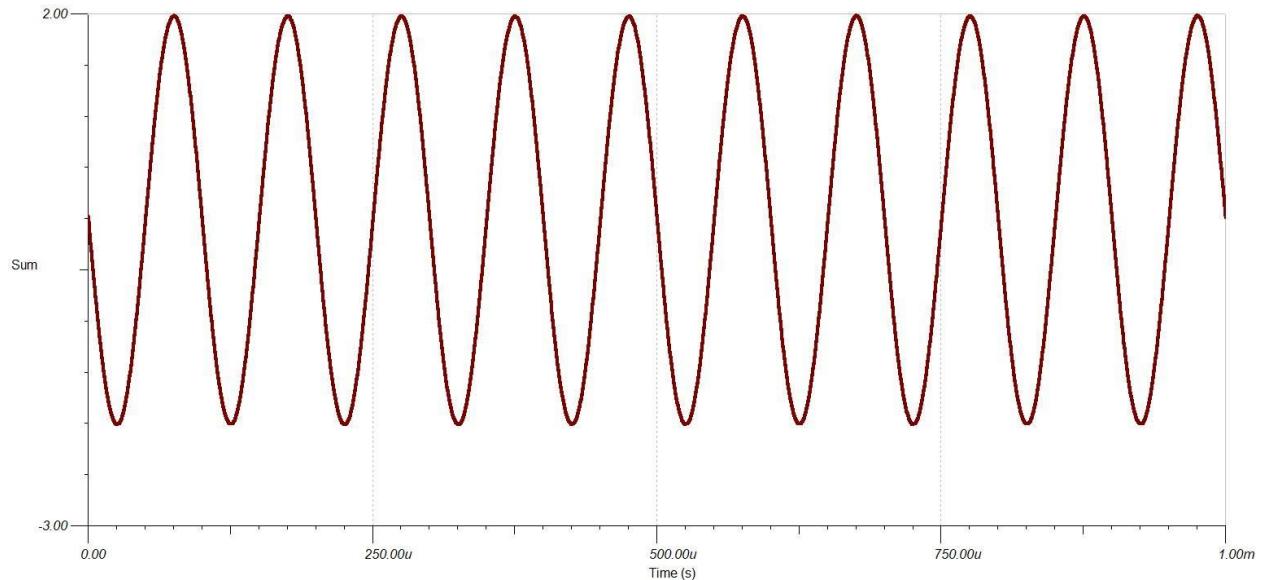


Figure 58. Addition Output

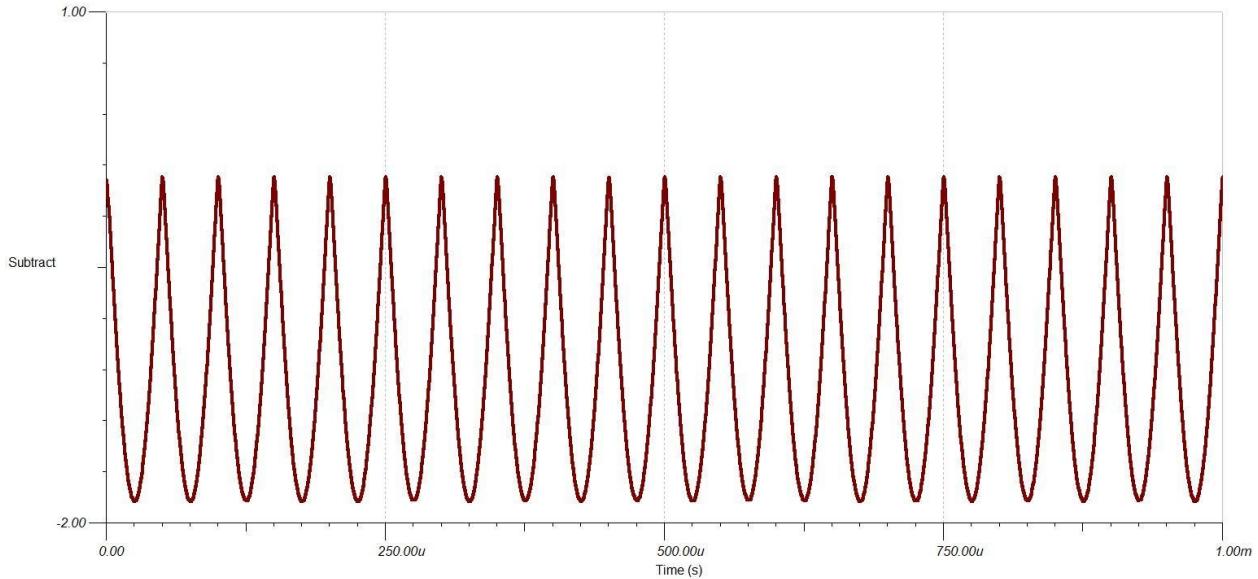


Figure 59. Subtraction Output

The differentiation and integration operations were separate TINA files but also operated similarly. The differentiation and integration operations only operated on one signal. The channel signal was imported as the input to the differentiation and integration circuits. The differentiation and integration circuits each had six filters in the equalizer. Two buffers were implemented to feed three of the filters each to prevent fan-out. The differentiation and integration operations performed all six differentiations and integrations in parallel. The circuits generated six differentiation and six integration signals that were exported as text files. The filter macro was used to split the six outputs into separate files and reduce the number of samples by 10. The separate differentiation and integration signals were then imported into the differentiation and integration select circuits. The select circuits contained an analog multiplexer used to choose which integration and differentiation signal to use based on the frequency of the signal. A single output was produced from the differentiation and integration select circuits, but the circuits still had to be exported as text files. The filter macro was run on them to reduce the number of samples by 10.

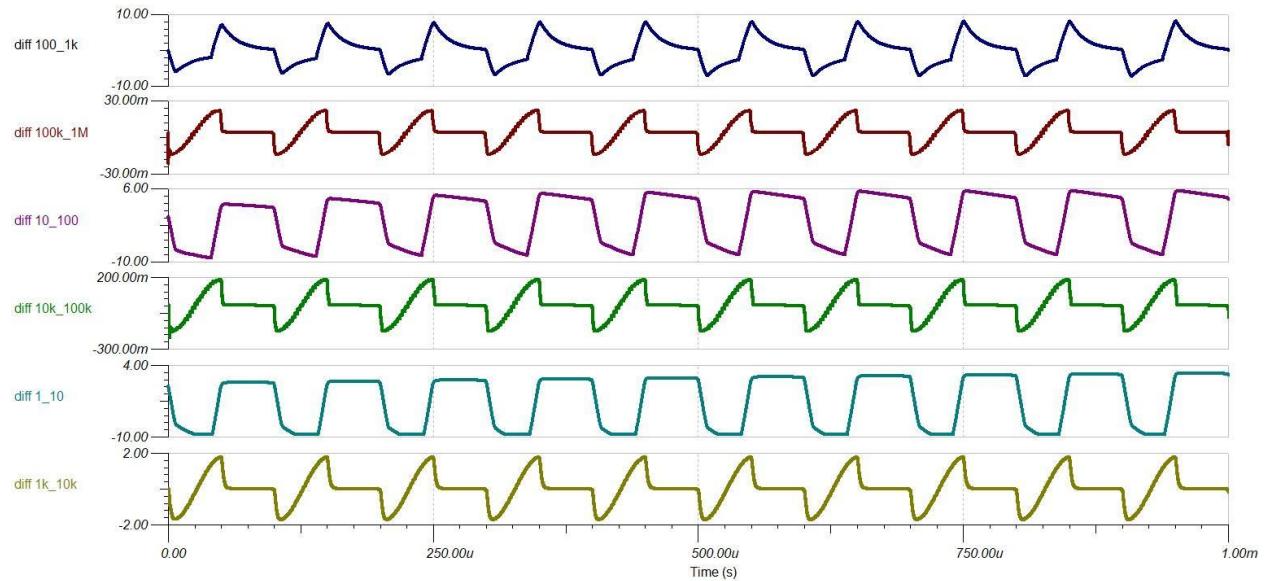


Figure 60. Differentiation Equalizer Output

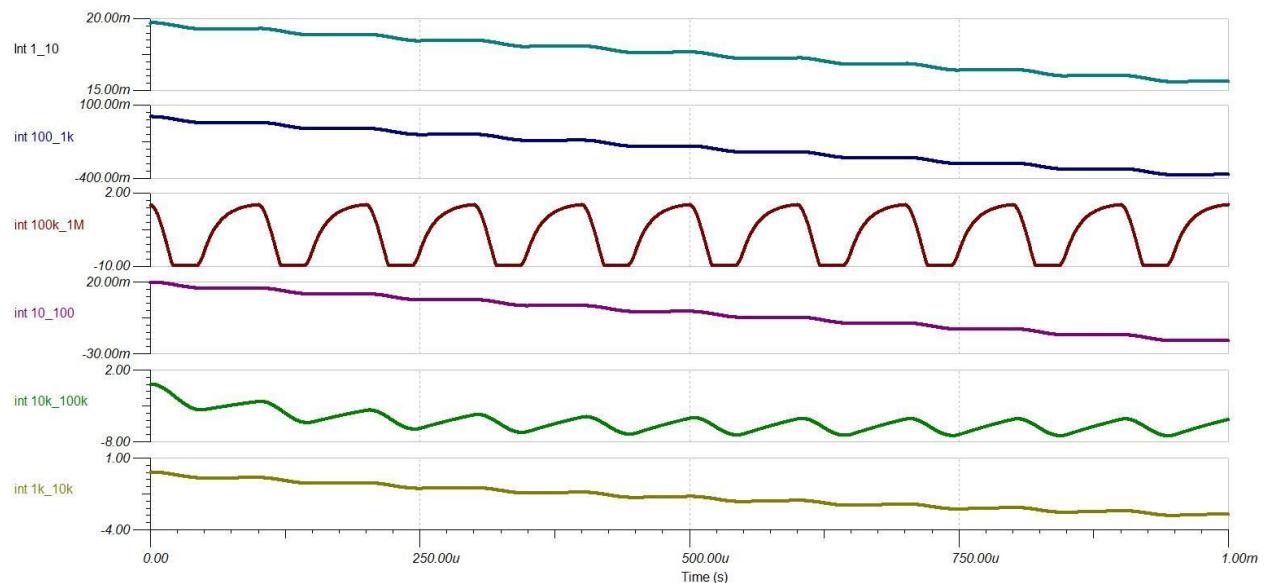


Figure 61. Integration Equalizer Output

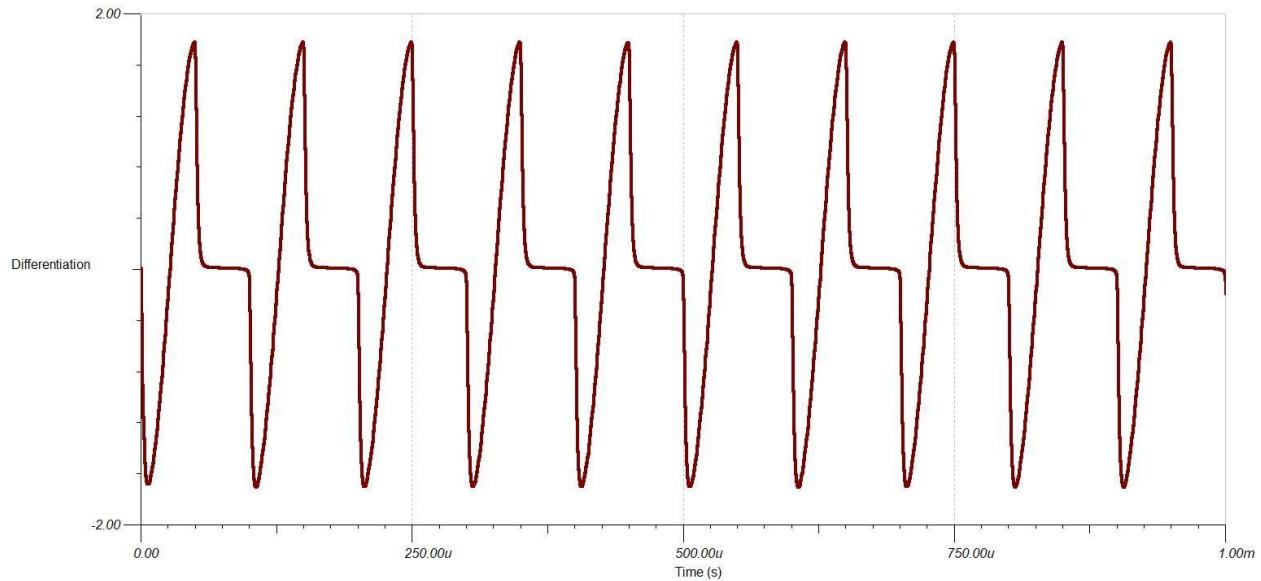


Figure 62. Differentiation Select Output

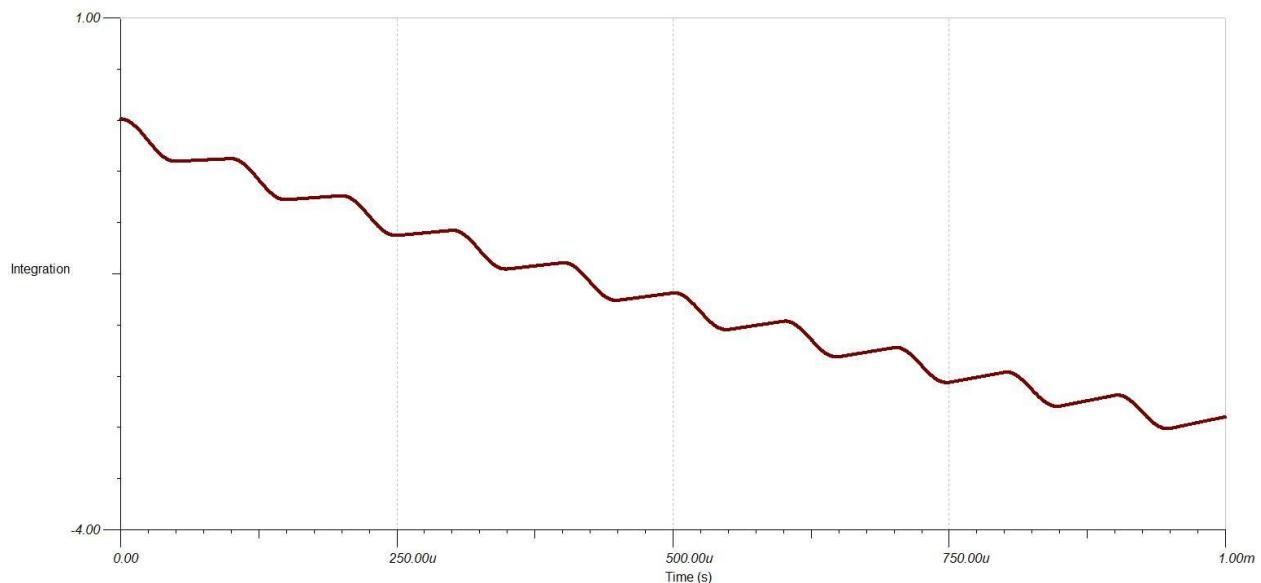


Figure 63. Integration Select Output

The operation select circuit included an analog multiplexer used to select which operation to output to the microcontroller. The output for all of the operation circuits were imported into the different inputs of the circuit. A complete simulation was performed so each of the operations was selected and outputted to the microcontroller. The analog multiplexer was controlled using analog switches.

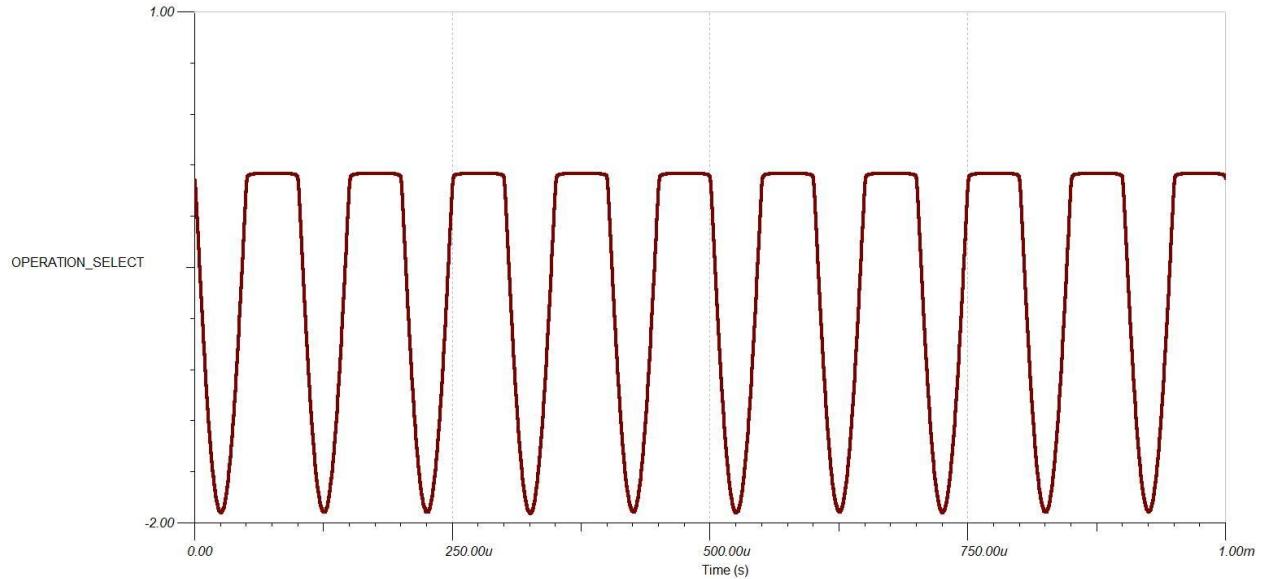


Figure 64. Operation Select Output Channel 1 Pass

The last circuit used for the analog input simulation was the microcontroller conditioning circuit. The microcontroller only reads positive voltage. The operation selected from the operation select circuit was imported and the circuit transformed the signal into a signal readable by the microcontroller. The microcontroller offset and scaled the voltage so that the voltage signal was between 0V and 1V and was inverted to correct the inverted operations. The microcontroller conditioning circuit had three outputs. The output corresponding to the voltage division used by the voltage select circuit was selected to output the signal. The other outputs were set to the negative supply voltage to indicate that they were not used. The microcontroller conditioning circuit was used 8 times to prepare all 8 possible operations for a complete simulation. The conditioned signal was exported as a text file. A different macro was used to format the data to a CSV that can be read by LABVIEW. It was noted that the conditioning circuit was not necessary since the data was read through LABVIEW. The microcontroller was used in simulation to parallel the physical implementation of the DAQ system.

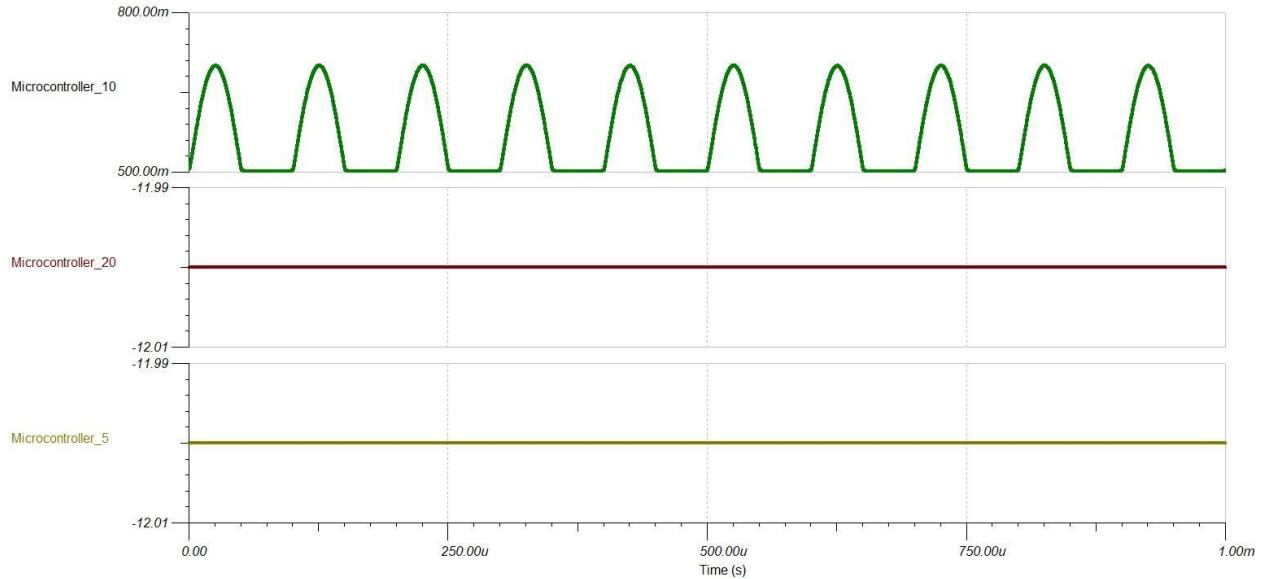


Figure 65. Microcontroller Conditioning Output for Channel 1 Pass

Test procedure for the digital side was a two step process. First the real time signal was acquired and observed based off of a known comparison. The signal received and recreated was observed in comparison to values received by an oscilloscope. Second, the digital signal exported from TI-TINA was read via a CSV file and then observed using labVIEW. This signal was compared to the original signal as viewed using TI TINA.

### 3.2.11 Design Discussion

The DAQ analog system had minor attenuation inconsistencies and noticeable phase shifts near the frequency limit. It was recommended that even though the system was designed for signals up to 1 MHz, that the DAQ system not be used for signals with a frequency near 1 MHz. The effect limit of the DAQ system was approximated at 500 kHz, half a decade less than the absolute limit.

The simulated DAQ system does a poor job at demonstrating the communication between the different parts of the system. The analog and digital sections of the DAQ system were independent on each other and the only interaction between the two systems was the CSV files. The digital side of the DAQ system was unable to control the different analog multiplexers in the digital section to select voltage levels or operations. The sampling and measuring was performed by TINA simulations and was not controlled by the digital system. The simulation files for the analog section were all independent TINA files that were unable to communicate with each other. The analog multiplexers in the analog section were controlled by manual switches. The lack of communication between digital and analog components in the DAQ system required the user to manually make connections through switches and import and export signals which caused the simulation time to increase significantly.

The DAQ system was composed of many separate TINA files that took a long time to simulate. The output from each circuit must be exported and then formatted by running the Excel macro. Demonstration videos for the DAQ system indicated that it can take around half an hour to one hour to simulate all the TINA files in the analog section of the DAQ system.

The digital section of the DAQ system read the data points from the CSV file and placed the points equidistant from each other in the time interval. The data points obtained from the TINA simulation were observed to not be sampled at consistent intervals. The waveforms displayed on the digital system were observed to appear stretched or compressed because the data points were forced to be equidistant when they were not measured at consistent intervals.

## 4 Management

### 4.1 Project Milestones

Table 1. Planned GANTT Chart

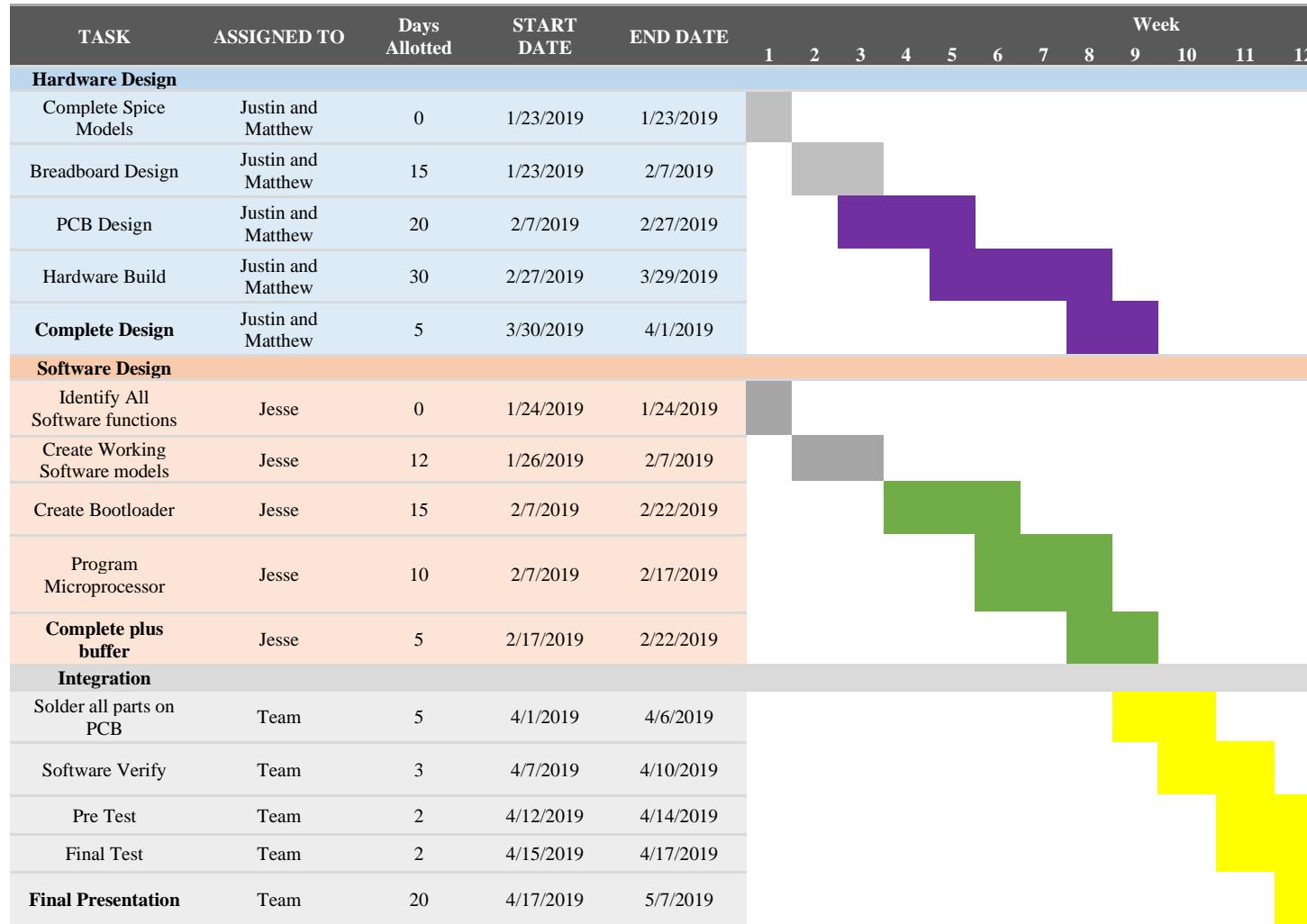


Table 2. Running GANTT Chart



<b>Analog Section Simulation</b>					
Create All Simulation Files in TINA	Justin and Matthew	13	4/3/2020	4/16/2020	
Integrate all the separate TINA Files to complete the analog system	Justin and Matthew	13	4/3/2020	4/16/2020	
Develop Tutorial Videos	Justin and Matthew	22	4/16/2020	5/8/2020	
Debug and Improve Analog Section Simulation	Justin and Matthew	22	4/16/2020	5/8/2020	
Prepare for Final Simulation Demonstration	Justin and Matthew	7	5/1/2020	5/8/2020	
<b>Software Design</b>					
Identify All Software functions	Jesse	0	1/24/2019	1/24/2019	
Create Working Software models	Jesse	12	1/26/2019	2/7/2019	
Create Bootloader	Jesse	15	2/7/2019	2/22/2019	
Program Microprocessor	Jesse	10	2/7/2019	2/17/2019	
<b>Complete plus buffer</b>	Jesse	5	2/17/2019	2/22/2019	
<b>Integration</b>					
Develop COVID 19 Response Plan	Team	14	3/20/2020	4/3/2020	
Software Demonstration	Team	6	4/10/2020	4/16/2020	
Final Software Demonstration	Team	7	5/1/2020	5/8/2020	
Final Presentation	Team	6	5/8/2020	5/14/2020	

The team was closely following schedule for the first half of the semester. The planned and GANTT charts were relatively together until the third week of March. During the third week of March the COVID-19 outbreak occurred. One week of senior design was considered optional as the school decided how to adapt senior design to the outbreak. The school decided to shift all projects from physical implementation to software demonstration. The original plan for the project was abandoned, and the team then had to design a detailed COVID-19 response plan and adapt the project to software demonstration. The COVID-19 response plan and adapting the project took another two weeks. A total of three weeks of senior design were lost to adjust to the COVID-19 outbreak. The objectives in the new GANTT chart were updated based on developed COVID-19 response plan.

## 1.

## **4.2 Encountered Challenges and Lessons Learned**

The outbreak of the COVID-19 pandemic forced the project to shift from a physical implementation to a simulation demonstration. The shift from physical to simulation caused all purchased physical components to be obsolete for the project. The original simulation files used in the design for the DAQ system were split between TI TINA files and PSpice files. It was decided to move the entire simulation to TI TINA for ease of importing and exporting signals. TI TINA also had the advantage of having spice files for many TI integrated circuits built into the simulator. The simulation files in PSpice were rebuilt in TINA.

Justin's main problem was designing and integrating the entire analog DAQ system in TINA. Originally the entire DAQ system was in one TINA simulation file, but the circuit diagram was difficult to read and had a long simulation time. Justin revised the design to split the analog system into multiple simulation files. Each simulation file performed one operation so that the circuits were simple to understand and the simulation time for each simple simulation file significantly decreased. The next problem Justin experienced was connecting the separate simulation files together to form the complete system. Justin developed the Excel macros to quickly format the data between exported and imported data to allow data to flow between simulation files as imported and exported data.

Matt's main problem was debugging the analog DAQ system. Justin had only initially tested the signals for low frequency inputs. Matt's robust testing showed that the Excel macro to format exported data did not work for high frequency values when the time values were written in scientific notation. The macro rounded the time values which caused repeated time values. Matt worked with Justin to find a way to update the macro so that it did not round the time values and was able to operate on high frequency signals.

## **4.3 Team Ethics Discussion**

The relative workload between the different team members was relatively balanced. It was decided that Justin and Jesse would lead the system design sections because they had more experience. Jesse led the digital system design. It was his responsibility to design a system in LABVIEW that was able to read a CSV and display the data. Jesse worked with Justin to agree on a format for the CSV file to be read by the digital system. Justin led the analog system design. Justin's primary focus was creating the circuit diagrams, verifying the circuit diagrams, and linking the different simulation files together to form a complete system. Justin ran only the initial test on the entire system. Matt worked with Justin to aid in designing the basic components for the analog system but mainly focused on debugging and running simulations. Matt was responsible for running almost all of the test case simulations and alerted Justin when any of the test cases caused problems in the system.

The team was forced to discontinue the physical implementation of the DAQ system and design a simulation demonstration due to the COVID-19 outbreak. The change was necessary because it was impossible to meet in person to work on the physical implementation due to the outbreak. The team had already purchased some of the physical components for the implementation. The team believed that they could still create a physical implementation despite the circumstances. However,

after planning out the simulation demonstration, the group realized it was not feasible to create the physical implementation and a robust demonstration with given circumstances and limited time. The group decided to discontinue the physical implementation and focus on the simulation demonstration. Even though the group unanimously decided to focus on the simulation demonstration, it was still disheartening to know that the physical implementation was discontinued.

The analog section of the DAQ system experienced two major specification changes. The first specification was the removal of the equalizer operation and the second was limiting the input voltage to  $\pm 50V$  instead of  $\pm 100V$ . The removal of the equalizer operation was proposed by Justin as the overall analog section designer. It took Justin longer than expected to design the differentiation and integration equalizers used in the system, and it would take him too long to design another equalizer. The group agreed with his decision since equalizer aspects were already included in the differentiation and integration equalizers. The limited input voltage was also proposed by Justin after noting the voltage division voltage would exceed the system voltage. The first proposed solution by the group was to raise the system voltage to  $\pm 24V$ , so that the system voltage was not exceeded. However, the team had already purchased the  $\pm 12V$  linear power supply. It would be a waste of funds to change the system voltage and purchase another power supply, so the group agreed to adjust the input voltage to work for the already purchased power supply.

#### 4.4 Budget

The original DAQ system required a microcontroller to process the analog signals from the analog section of the system to the Digital section. The STM3277 microcontroller was chosen because it had three parallel ADC channels which means that it was able to convert three different analog signals to digital signals without multiplexing. The DAQ system was designed to use two of the channels to display the channel signals and the last channel as used to display the selected operation. The operational amplifier LM318 was chosen because it was a commercial grade operational amplifier with a large bandwidth to operate on the entire selected frequency range. Most of the circuits in the analog section required operational amplifiers, so a bulk of operational amplifiers was purchased for a discount. The HBB15-1.5 AG power supply was purchased because it was a  $\pm 12V$  linear power supply. A linear power supply provided a smoother reference voltage than a switch mode power supply. Additional funds were set aside for passive components such as resistors and capacitors. Many coupling capacitors were needed for all of the integrated circuits used in the design. Funds were also set aside to purchase PCBs to place all of the circuits. The LABVIEW software was provided by the project team. The physical implementation was discontinued, so not all of the physical components were purchased and the components that were purchased were not used in the final demonstration.

**Project Budget**

	Items	Unit cost (\$)	Quantities	Total cost (\$)	Comments
Parts	LPC1769FBD100	\$2.77	1	\$11.75	Microcontroller

	THS4631	\$5.05	99	\$5.05	Operational Amplifier
	DG408LEDY-T1-GE3	\$1.67	3	\$5.01	Analog Multiplexer
	1N4728A	\$0.174	10	\$1.74	Zener Diode 3.3V
	1N4733A	\$0.165	10	\$1.65	Zener Diode 5.1V
	BZX79C2V0 R0	\$0.17	10	\$1.70	Zener Diode 2.0V
	HBB15-1.5-AG	\$83.11	1	\$83.11	Dual Voltage Linear Power Supply
	Passive Components	\$50.00	1	\$50.00	Additional Resistors, Capacitors, etc.
	PCBs	\$7.00	10	\$70.00	Order Printer Circuit Boards
Equipment		\$		\$	
		\$		\$	
		\$		\$	
Software	LABVIEW	\$0.00		\$0.00	Self-Provided
		\$		\$	
		\$		\$	
		\$		\$	
			<b>Total cost</b>	<b>\$230.01</b>	

## 4.5 Funding Source

The DAQ system was funded by the university by participating in community service projects. Each member will receive \$100 for their community service for a total of \$300. If the sponsored amount is insufficient, then the remaining costs will be self-funded by the project team. The physical implementation was discontinued, so not all the funds were used and any components purchased with funds were not used in the final simulation demonstration.

## 4.6 Human Safety Assessment

The project was shifted to a simulation demonstration, so there was no risk for physical safety. The simulation demonstration required Microsoft Excel, TI TINA, and LABVIEW to all be running at the same time to perform the demonstration. It is somewhat common that it may be too resource intensive for some computers to run all the programs at once. The simulation can be performed in parts to alleviate the stress on the computer. The analog section can be run first using Microsoft Excel and TI TINA to generate the output CSV file. The applications for the analog section can then be closed and the digital section can be run using LABVIEW and the CSV file. Another solution that was used in the demonstration was to run the analog section on one computer and then transfer the files to another computer to run the digital section.

The analog simulation required many files to be created for importing and exporting waveforms between the different simulation files. It is somewhat likely that imported and exported signal files may become lost due to poor organization and confusion. It is recommended to create separate folders to organize all the files used in the simulation to prevent files from being lost. It is also recommended to develop a naming convention for the different files, so that the contents and role of a file can easily be determined by the file name to prevent confusion.

Google drive was used to organize and share files. File sharing along with proper naming convention could be improved by using a file system such as subversion or Git. This allows for source control and version history along with the ability to revert files that may have caused an error.

## 4.7 Member Credentials and Responsibilities

Jesse Dengel is the leader of the project team and will be designing the digital section of the system. The digital system will include programming the microcontroller, developing the LABVIEW front panel and interfacing the microcontroller to the computer with LABVIEW.

Justin Chau is an electrical engineering student with experience designing and building complex electronic circuits. He designed the analog section of the DAQ system. He focused on designing the simulation files and verifying the simulation files. Justin also designed the macros used to link the different simulation files through exporting and importing files.

Matt Mutarelli is an electrical engineering student. He helped Justin design basic component for the analog section of the DAQ system. He focused on testing the overall analog system. Matt performed the analog demonstration multiple times for different signals at different magnitudes and frequencies.

### 4.7.1 Teamwork

#### 4.1.1 Jesse Dengel ([jad6nc@umsystem.edu](mailto:jad6nc@umsystem.edu), EE major):

**Member profile:** Jesse Dengel served as our team leader. His leadership role included writing status reports and setting up meetings. His involvement in the project focused on the digital section of the DAQ system. He designed an interface on LABVIEW that can read and display the signal stored in the CSV file generated from the analog section of the DAQ system. He also designed the display to measure different properties of the displayed signal. Jesse has worked for John Deere in the engineering department for the last seven years and has used LABVIEW during his work which gave him practical experience using LABVIEW. Jesse's work experience also gave him exposure to many aspects of DAQ systems in a real-world environment.

#### 4.1.2 Justin Chau ([jc2w4@umsystem.edu](mailto:jc2w4@umsystem.edu), EE major CPE minor):

**Member profile:** Justin Chau is involved in the analog section of the project. Justin is the lead designer for the analog section of the DAQ system. Justin has taken Electronics II

EE3120 and has experience modeling and designed complex electronic circuits. His main role was to design the different circuit files used in the simulation demonstration and integrate the circuit files to create a complete system. Justin has worked at Toth & Associates for around three years. During his work experience, Justin has developed experience using VBA to design macros in Excel to operate and format data in Excel. Justin's experience in VBA was used to design macros to format imported and exported signals to link separate CSV files in TINA.

#### **4.1.3 Matthew Mutarelli ([mattmutarelli@gmail.com](mailto:mattmutarelli@gmail.com) EE major):**

**Member profile:** Matt Mutarelli is involved in the analog section of the project and works closely with Justin. Matt helped Justin design some of the components used in the analog section of the DAQ system. Matt's main role was to test and debug the analog section designed by Justin. Matt tested the system for different signals at different frequencies and magnitudes.



## 5 Conclusions and Future Work

### 5.1 Conclusions and Lessons Learned

The project provided real application for circuit design and implementation before the physical implementation was discontinued. Basic circuit design practices such as coupling capacitor and measuring techniques were learned and applied throughout the project when the physical implementation was not discontinued. The practical experience of circuit implementation was gained from the project even if the physical implementation was discontinued.

It was also noted that the ability to condition circuits was important for many applications not just in DAQ systems. Often integrated circuits only work for specific ranges, so it is necessary to condition the signals so that they can be operated on by the integrated circuit. Signal conditioning must be effective for all signal types and include protection to prevent damage to the integrated circuit. The project emphasized the need for signal conditioning because signals were conditioned twice for the different sections of the DAQ system. The analog probe circuits condition the input circuit so that the analog DAQ system can operate on the signal. The analog section of the DAQ system then conditioned the output signal again so that the signal can be read and displayed by the digital section of the DAQ system.

It was concluded from the project that it was difficult to design DAQ systems that were able to measure a wide range of frequencies and voltages. The voltage range of the DAQ system was controlled by the voltage divisions used and the system voltage. A small voltage division level was necessary to measure smaller voltage. The input voltage range was controlled mainly by the system voltage, a larger system voltage allowed for a higher voltage. The components of the DAQ system must be designed to work at a higher voltage to implement the DAQ system at a higher voltage. The frequency range of the DAQ system was also dependent on the components used in the DAQ system. Components such as operational amplifiers and other integrated circuits must be able to operate at high frequencies for the system to allow high frequency signals. The integration and differentiation operations were noted to be particularly difficult to implement in analog over a large frequency range. The existing DAQ systems observed by the team were observed to have a limited frequency and voltage range because of the difficulty in implementing wide frequency and voltage ranges.

From the digital perspective, it was learned that hardware and software integration is more difficult than often expected. Substantial effort was made to integrate the microcontroller with the software, before we had to move to a different data acquisition system. The microcontroller could have been integrated but due to time constraints and external constraints we were forced to go another direction.

## 5.2 Suggested Improvements

The main improvement suggested by the team was to continue and finish the physical implementation of the DAQ system. The designed project did a poor job of demonstrating the communication between the different analog and digital components in the system. The simulations were disjointed from each other and the analog simulation had to manually set all the control switches. The physical implementation would show how the digital system was able to automatically control all of the switches in the analog section.

Another suggested improvement was the addition of additional operations. The analog section could have implemented a multiplication operation using a mixer. The equalizer operation that was removed from the final design could also be added.

The operational amplifier used in the simulation demonstration was an LM318 operational amplifier by TI. It was observed that the DAQ system was not as effective as it reached the frequency limit of  $1MHz$ . It was suggested that a different operational amplifier was used with a higher gain bandwidth product, so that the DAQ system was still effective at the frequency limit of  $1MHz$ .

Due to restraints in resources from the COVID-19, a change in the data acquisition had to be made to the NI6501. This device has a much lower sampling rate than the planned ST Micro discovery board (claimed sampling rate at 1.5 MSPS). The NI6501 still provided an adequate real world example of data acquisition from -10 to +10 volts. The NI6501 also integrated well with LabView and was chosen because Jesse already had resources available for this device.



## **6 References**

- [1] DATAQ Instruments, “DI-1100 Low-Cost USB Data Acquisition (DAQ) System,” DI1110 datasheet, 2017
- [2] Measurement Computing “USB-1608FS-Plus Simultaneous USB DAQ Device,” USB-1608FS-Plus datasheet, 2018
- [3] National Instruments, “NI 9381,” NI 9381 datasheet, March 2016



## 7 Appendix

### 7.1 DAQ System Analog Section Files

Double click the icon to open the folder.



Analog Section Files.zip

### 7.2 YouTube Video Demonstrations

#### 7.2.1 DC Signal Demonstration by Matt Mutarelli

<https://www.youtube.com/playlist?list=PLprNBGzKJZ5-qo0smdbsvNuR0kEpkaQKc>

#### 7.2.2 Sine Wave Demonstration by Matt Mutarelli

<https://www.youtube.com/playlist?list=PLprNBGzKJZ58zX44O1euLMAXybKAS54OX>

#### 7.2.3 Triangle Wave Demonstration by Justin Chau

[https://www.youtube.com/playlist?list=PLprNBGzKJZ5\\_rulC4Ug4Usi0gwLMkeOE7](https://www.youtube.com/playlist?list=PLprNBGzKJZ5_rulC4Ug4Usi0gwLMkeOE7)

### 7.3 Data Sheet for Key Components

Double click the icon to open the folder.



Data Sheets.zip