Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 2, 13:59

Student ID:

Student Name:

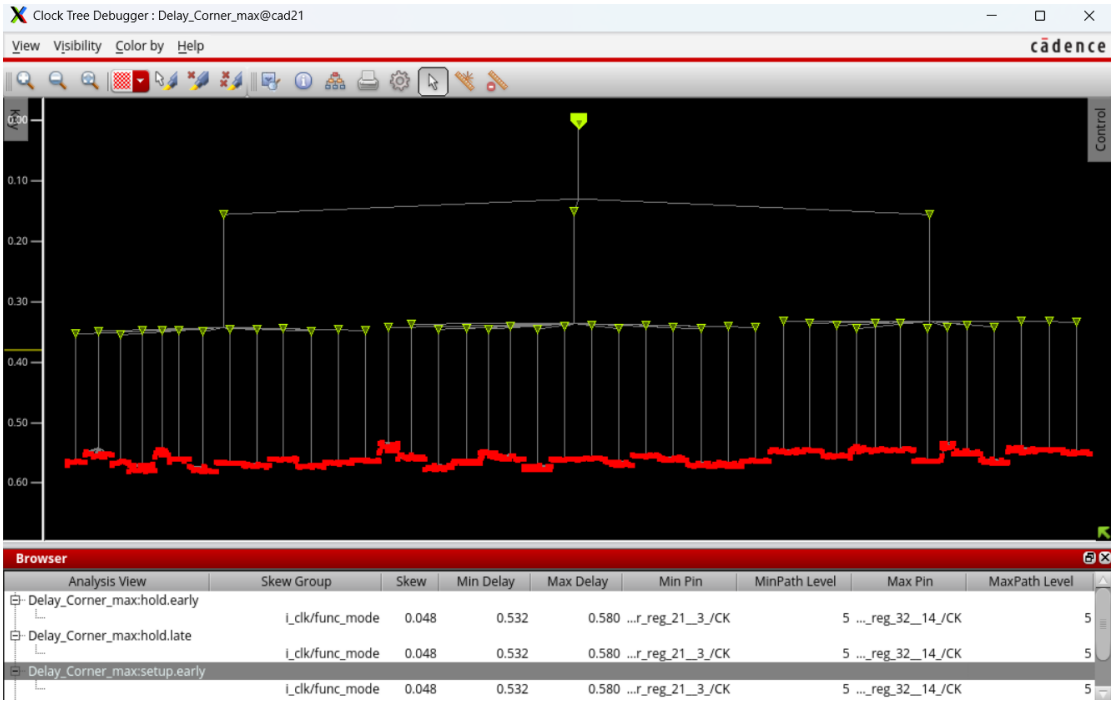
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	1182449.39
	Core Area (um^2)	859337.61
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	10ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		From TA

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 1453.7) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 182.240 182.240} 1 of 36
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 0.000 364.480 182.240} 2 of 36
 VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 0.000 546.720 182.240} 3 of 36
 VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 0.000 728.960 182.240} 4 of 36
 VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 0.000 911.200 182.240} 5 of 36
 VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 0.000 1087.900 182.240} 6 of 36
 VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 182.240 182.240 364.480} 7 of 36
 VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 182.240 364.480 364.480} 8 of 36
 VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 182.240 546.720 364.480} 9 of 36
 VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 182.240 728.960 364.480} 10 of 36
 VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 182.240 911.200 364.480} 11 of 36
 VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 182.240 1087.900 364.480} 12 of 36
 VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 364.480 182.240 546.720} 13 of 36
 VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 364.480 364.480 546.720} 14 of 36
 VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 364.480 546.720 546.720} 15 of 36
 VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 364.480 728.960 546.720} 16 of 36
 VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 364.480 911.200 546.720} 17 of 36
 VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 364.480 1087.900 546.720} 18 of 36
 VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 546.720 182.240 728.960} 19 of 36
 VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 546.720 364.480 728.960} 20 of 36
 VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 546.720 546.720 728.960} 21 of 36
 VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 546.720 728.960 728.960} 22 of 36
 VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 546.720 911.200 728.960} 23 of 36
 VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 546.720 1087.900 728.960} 24 of 36
 VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 728.960 182.240 911.200} 25 of 36
 VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 728.960 364.480 911.200} 26 of 36
 VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 728.960 546.720 911.200} 27 of 36
 VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 728.960 728.960 911.200} 28 of 36
 VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 728.960 911.200 911.200} 29 of 36
 VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 728.960 1087.900 911.200} 30 of 36
 VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 911.200 182.240 1086.910} 31 of 36
 VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {182.240 911.200 364.480 1086.910} 32 of 36
 VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {364.480 911.200 546.720 1086.910} 33 of 36
 VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {546.720 911.200 728.960 1086.910} 34 of 36
 VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {728.960 911.200 911.200 1086.910} 35 of 36
 VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {911.200 911.200 1087.900 1086.910} 36 of 36
 VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:08.5  ELAPSED TIME: 8.00  MEM: 0.0M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Nov 30 22:55:50 2025

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1087.9000, 1086.9100)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 22:55:51 **** Processed 5000 nets.
**** 22:55:51 **** Processed 10000 nets.
**** 22:55:52 **** Processed 15000 nets.
**** 22:55:52 **** Processed 20000 nets.
**** 22:55:52 **** Processed 25000 nets.
**** 22:55:52 **** Processed 30000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Nov 30 22:55:53 2025
Time Elapsed: 0:00:03.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:03.1  MEM: 26.312M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.651  |  2.800  |  3.420  |  0.651  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  7690   |  3841   |  3763   |   86    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 57.814%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.476  |  0.476  |  4.965  |  5.678  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|  7690   |  3841   |  3763   |   86    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 57.814%
       (100.000% with Fillers)
------------------------------------------------------------
```

4. Show the critical path after post-route optimization. What is the path type? (10%)
(The slack of the critical path should match the smallest slack in the timing report)

```
Path 1: MET Late External Delay Assertion
Endpoint:   o_out_valid2       (^) checked with  leading edge of 'i_clk'
Beginpoint: U2/state_r_reg_1_/Q (v) triggered by  leading edge of 'i_clk'
Path Groups: {reg2out}
Analysis View: av_func_mode_max
Other End Arrival Time          0.000
+ Network Insertion Delay       0.500
- External Delay                5.000
+ Phase Shift                  10.000
+ CPPR Adjustment               0.000
= Required Time                 5.500
- Arrival Time                  4.849
= Slack Time                    0.651
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  0.480
     = Beginpoint Arrival Time       0.480
     +-------------------------------------------------------------------------------+
     |        Instance         |      Arc       |   Cell   | Delay | Arrival | Required |
     |                         |                |          |       |  Time   |   Time   |
     |-------------------------+----------------+----------+-------+---------+----------|
     | U2/state_r_reg_1_       | CK ^           |          |       |   0.480 |    1.131 |
     | U2/state_r_reg_1_       | CK ^ -> Q v    | DFFRX1   | 0.685 |   1.165 |    1.816 |
     | U2/U297                 | A v -> Y ^     | NAND2X1  | 0.289 |   1.455 |    2.106 |
     | U2/U201                 | A ^ -> Y v     | NAND2X1  | 0.163 |   1.618 |    2.269 |
     | U2/U30                  | A v -> Y ^     | NAND2X4  | 0.337 |   1.955 |    2.606 |
     | U2/FE_OFC192_n40        | A ^ -> Y ^     | BUFX4    | 0.591 |   2.546 |    3.197 |
     | U2/FE_DBTC14_n40        | A ^ -> Y v     | INVX6    | 0.475 |   3.020 |    3.671 |
     | U2/FE_OFC222_conv_valid | A v -> Y v     | CLKBUFX6 | 0.674 |   3.694 |    4.345 |
     | U2/U229                 | A v -> Y ^     | NOR2X1   | 0.540 |   4.233 |    4.884 |
     | U2/U438                 | B ^ -> Y ^     | OR2X2    | 0.606 |   4.840 |    5.491 |
     |                         | o_out_valid2 ^ |          | 0.009 |   4.849 |    5.500 |
     +-------------------------------------------------------------------------------+
```

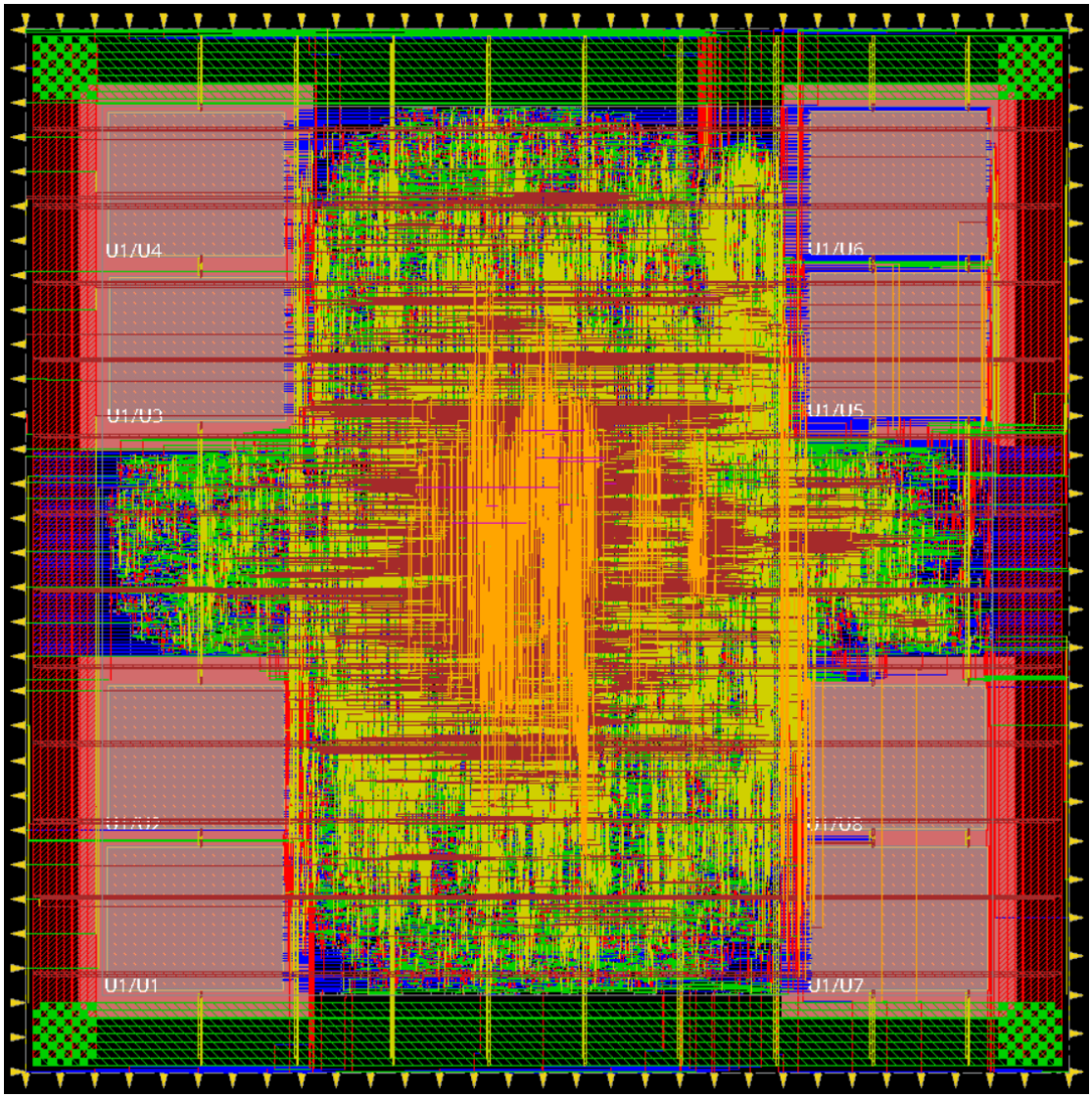
5. Attach the snapshot of GDS stream out messages. (10%)

```
Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/sram_512x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/sram_512x8.gds ......
        ****** Merge file: library/gds/sram_512x8.gds has version number: 5.
        ****** Merge file: library/gds/sram_512x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
************************ Analyze Floorplan ************************
    Die Area(um^2)             : 1182449.39
    Core Area(um^2)            : 859337.61
    Chip Density (Counting Std Cells and MACROs and IOs): 64.695%
    Core Density (Counting Std Cells and MACROs): 89.021%
    Average utilization        : 100.000%
    Number of instance(s)      : 69454
    Number of Macro(s)         : 8
    Number of IO Pin(s)        : 121
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
innovus 21>
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   SRAMs are large macro blocks that can block routing resources if placed in the

middle of the chip, so I lacing SRAMs in the corners avoids occupying the central area, providing more routing space for standard cells.