CSE 140
Computer Architecture

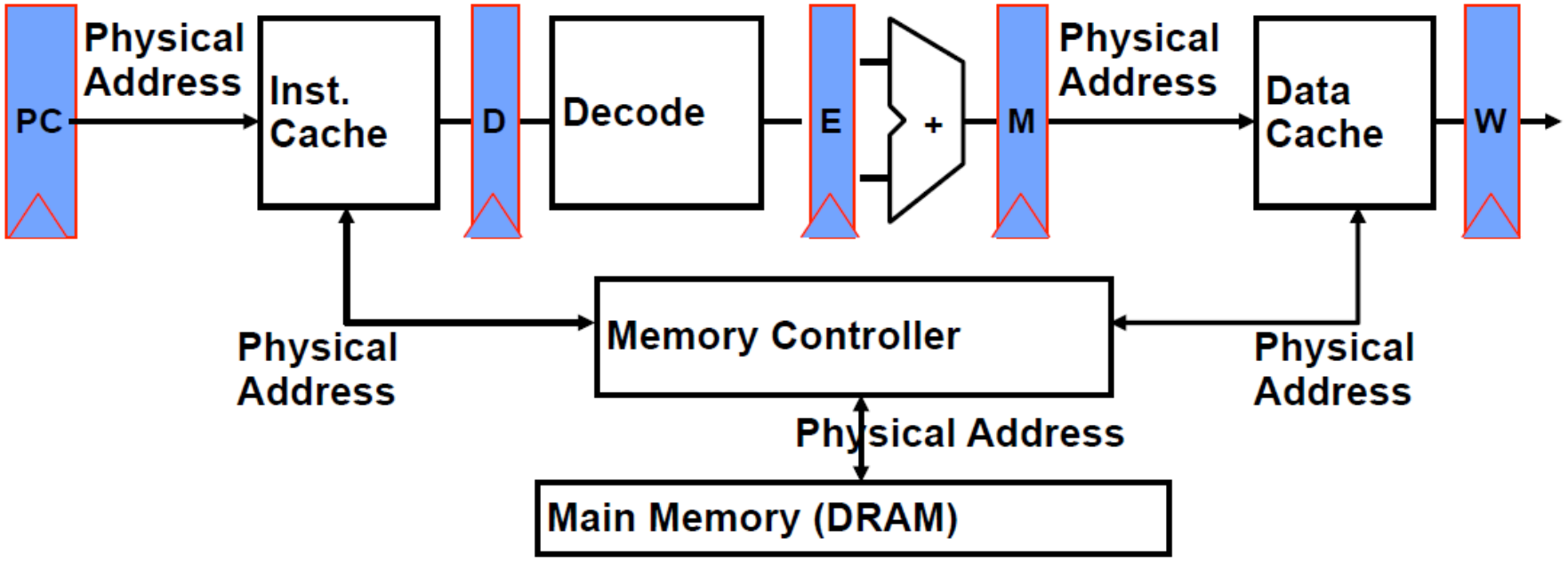
Lecture 10 – Memory Architecture
(Enhancing Performance)

Announcement

- HW #3
  - Due in 1 week (same as HW #3a)
- Project #1
  - Due 10/11 (Friday) at 11:59pm
- Midterm #1
  - 10/17, during lecture (not 10/10)
  - Lectures #1 - #8 (No virtual memory)
  - HW #1 - #3
  - Review on 10/15

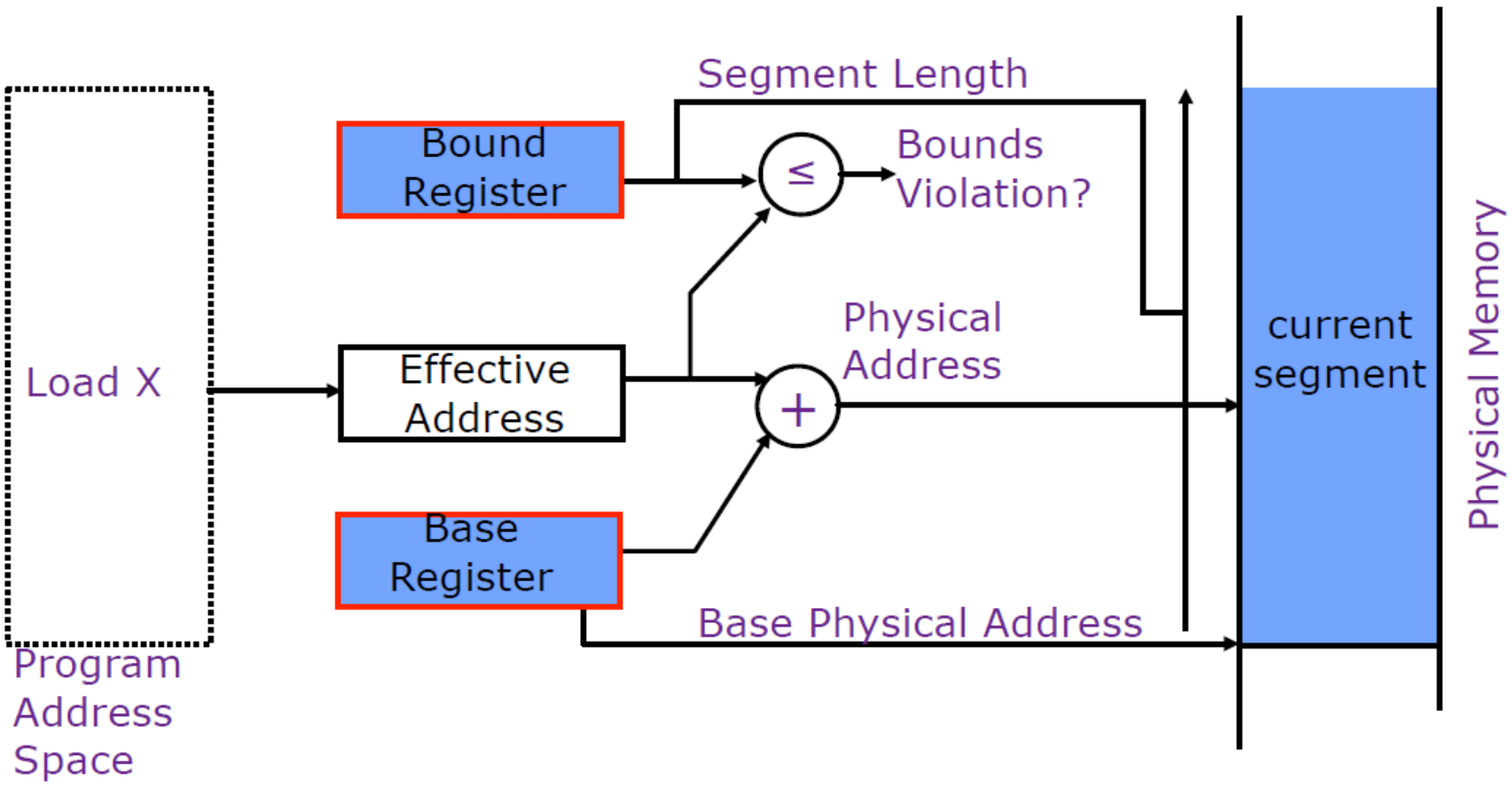
Bare Machine

- In a bare machine, the only kind of address is a physical address



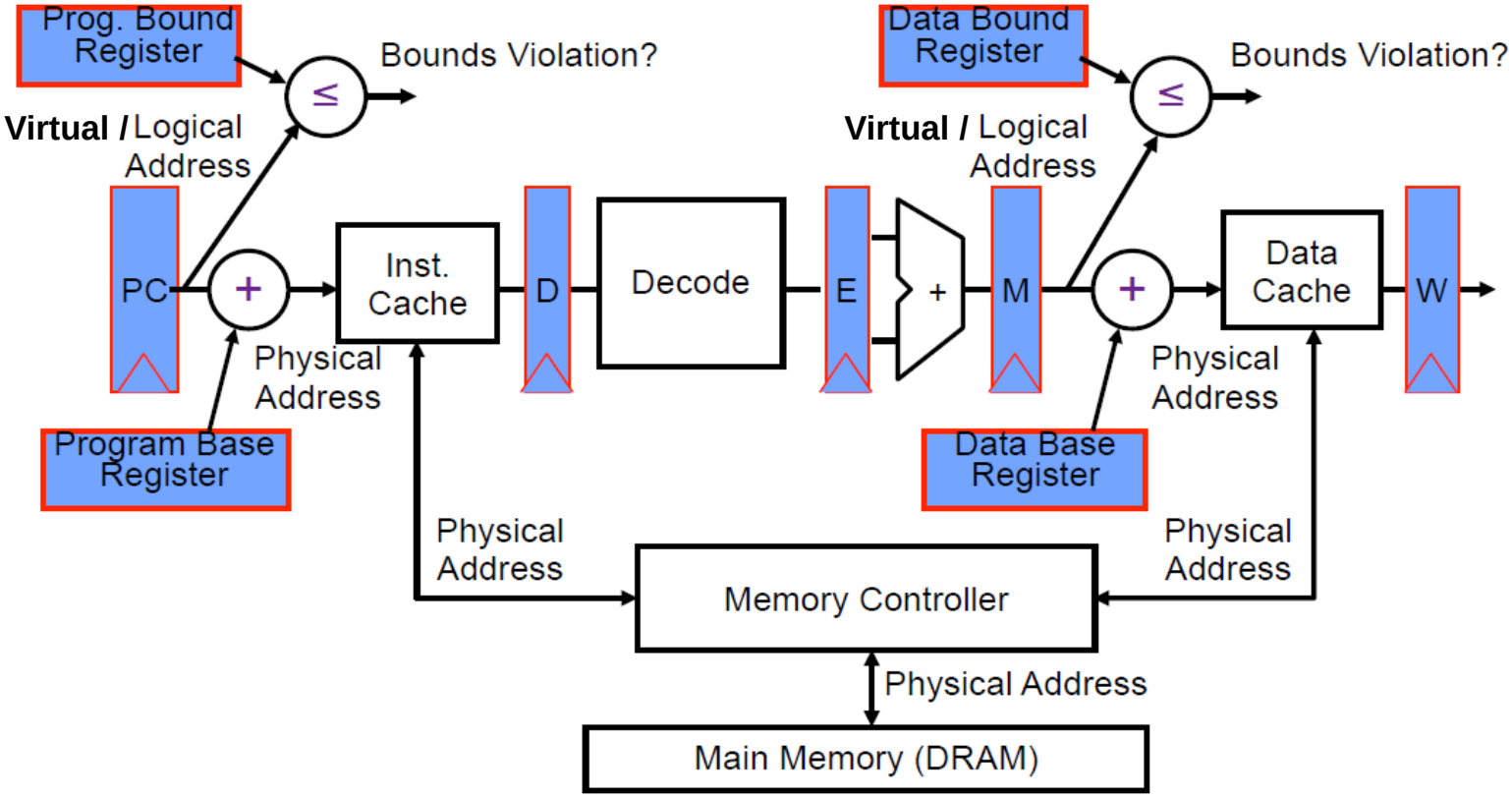
What if there are multiple processes or users?

Simple Base and Bound Translation



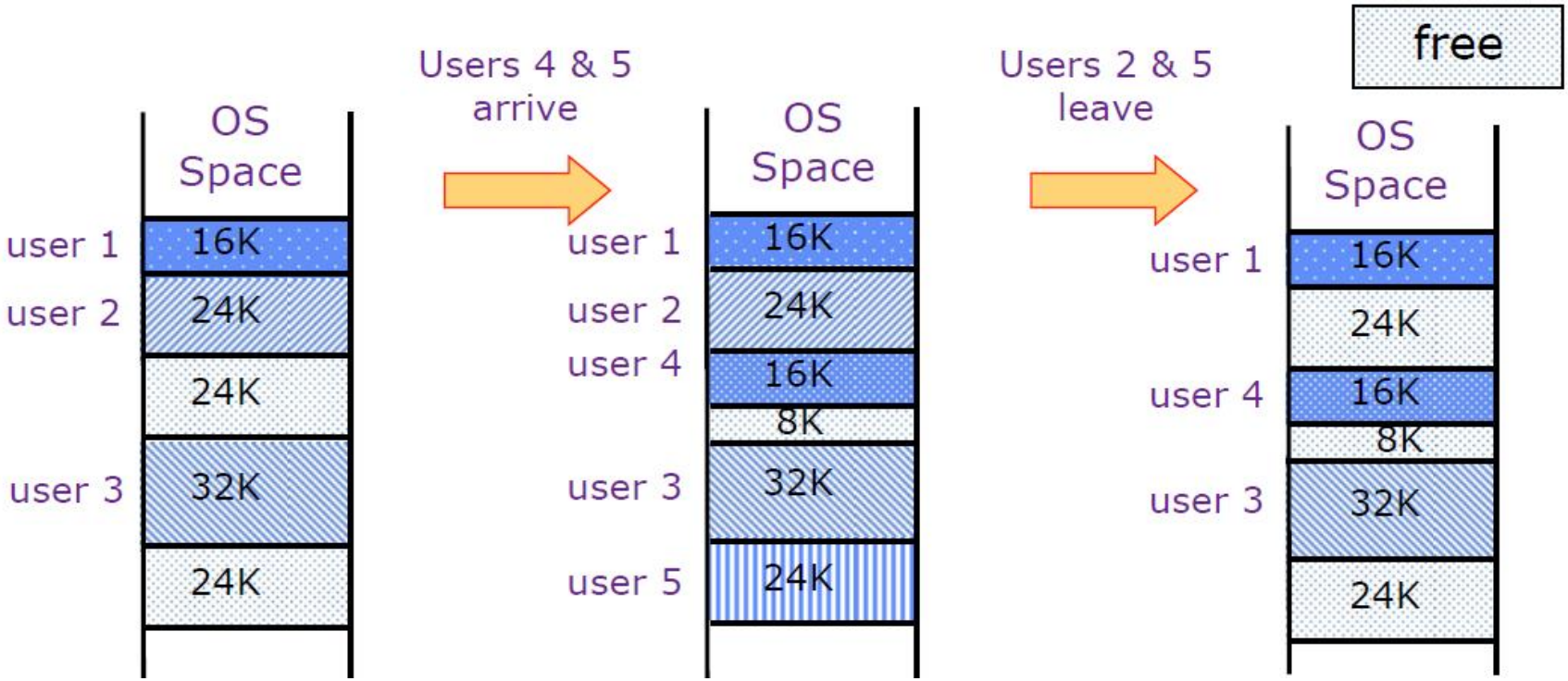
Base and bounds registers are visible/accessible only when processor is running in the *supervisor mode*

Base and Bound Machine



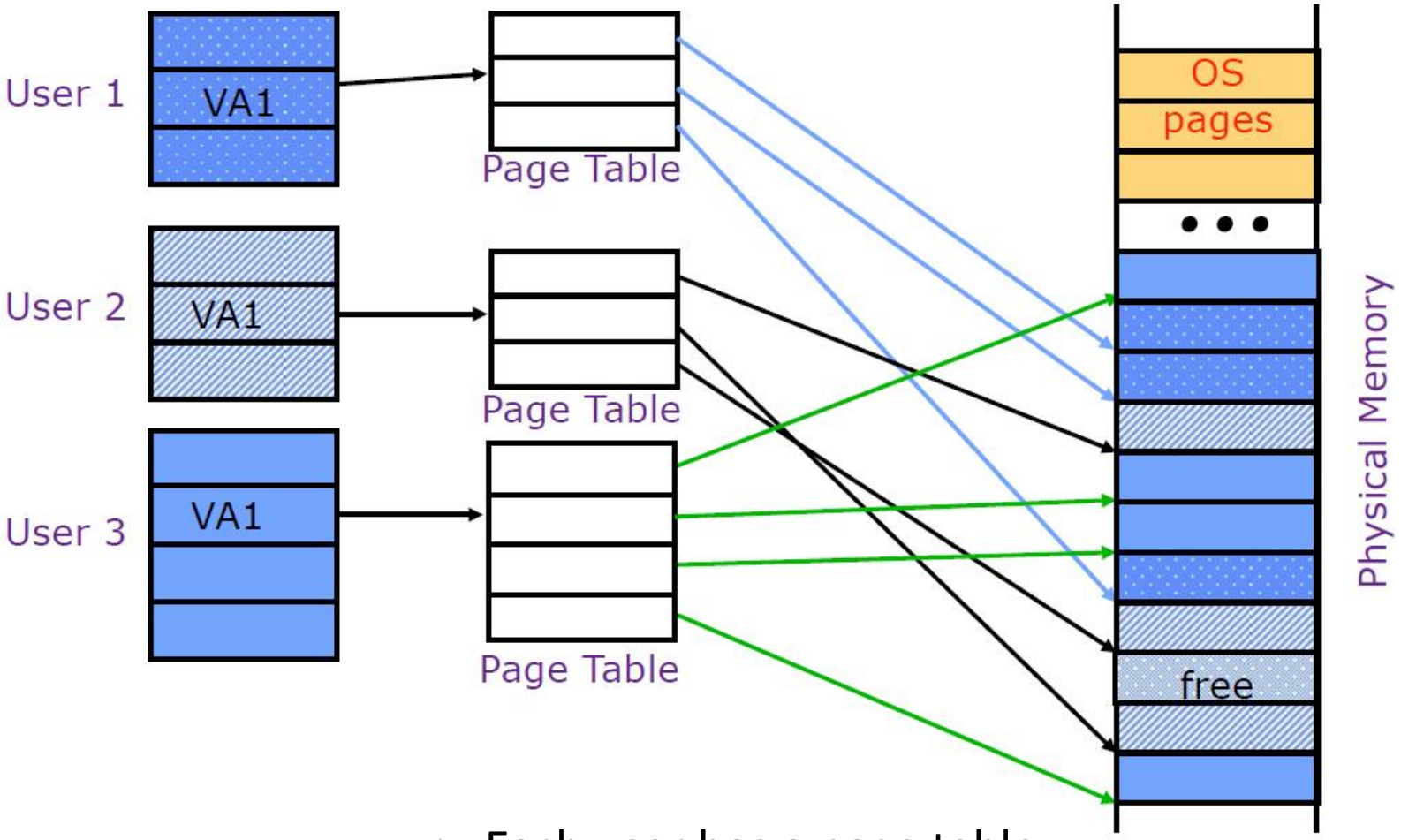
Can fold addition of base register into (base+offset) calculation using a carry-save adder (sums three numbers with only a few gate delays more than adding two numbers)

Memory Fragmentation



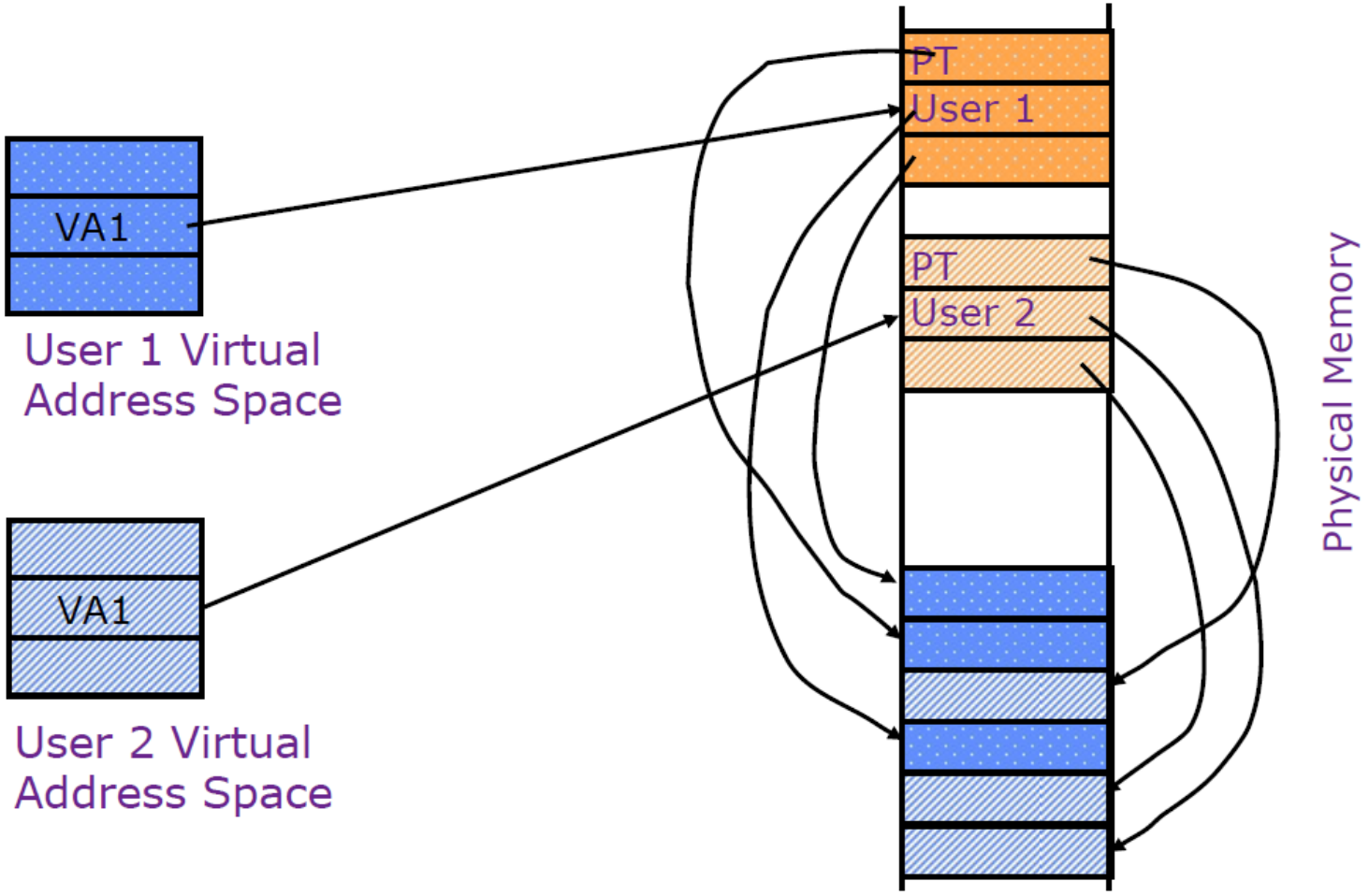
As users come and go, the storage is “fragmented”. Therefore, at some point programs have to be moved around to compact the storage.

Private Address Space per User



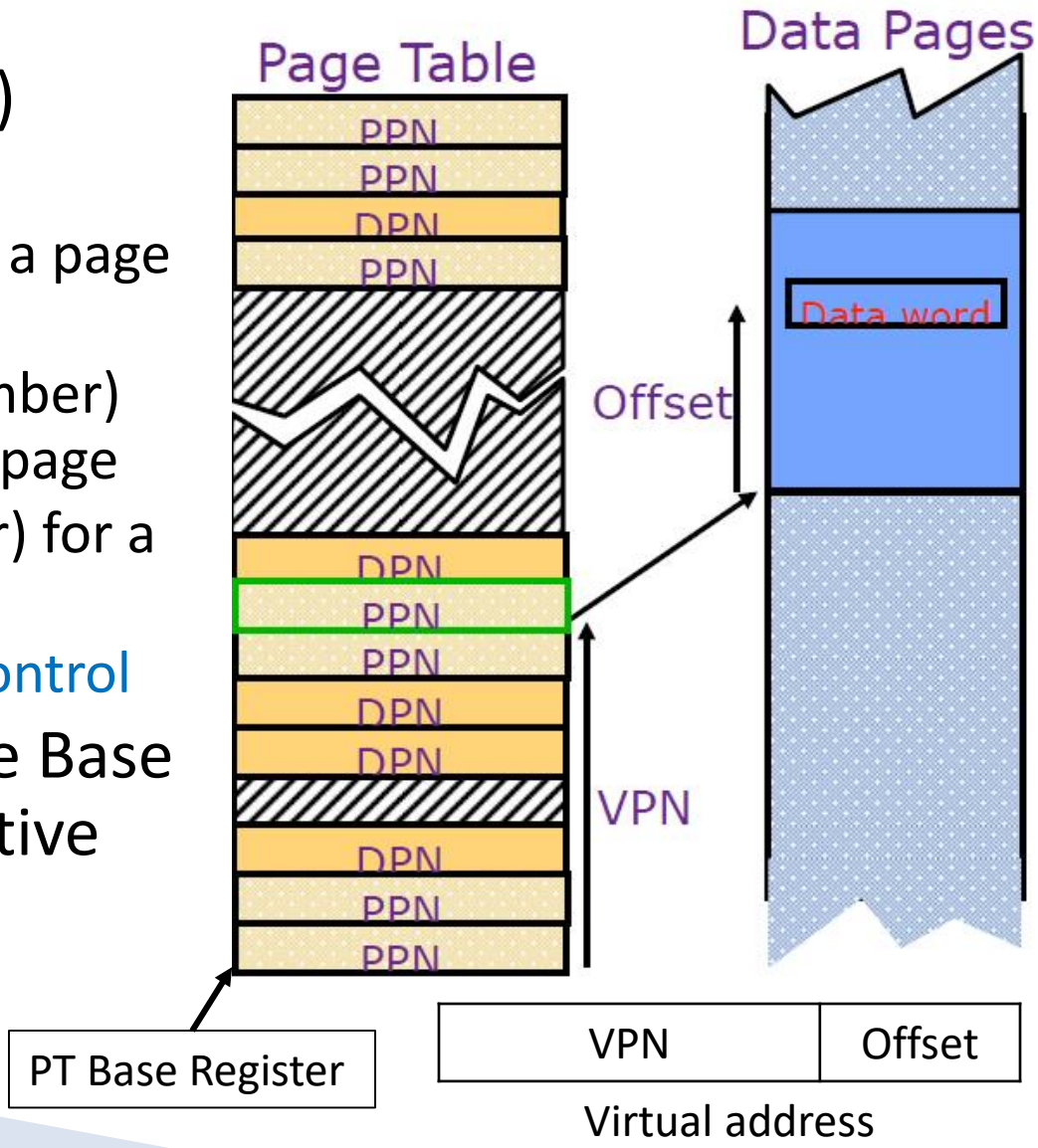
- Each user has a page table
- Page table contains an entry for each user page

Page Tables in Physical Memory

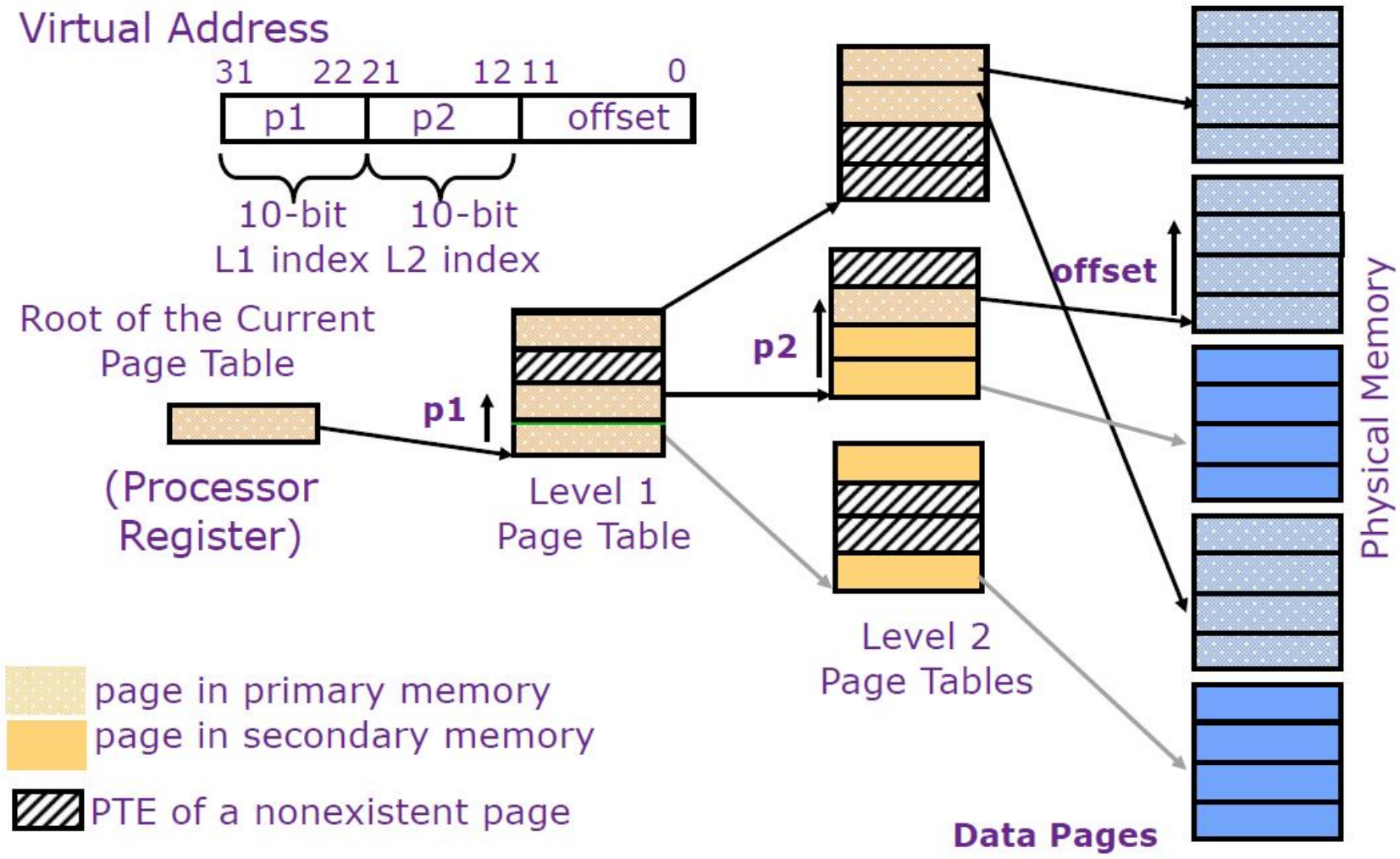


Linear Page Table

- Page Table Entry (PTE) contains:
  - A valid bit to indicate if a page exists
  - PPN (physical page number) for a memory-resident page
  - DPN (disk page number) for a page on the disk
  - Status bits for access control
- OS sets the Page Table Base Register whenever active user process changes

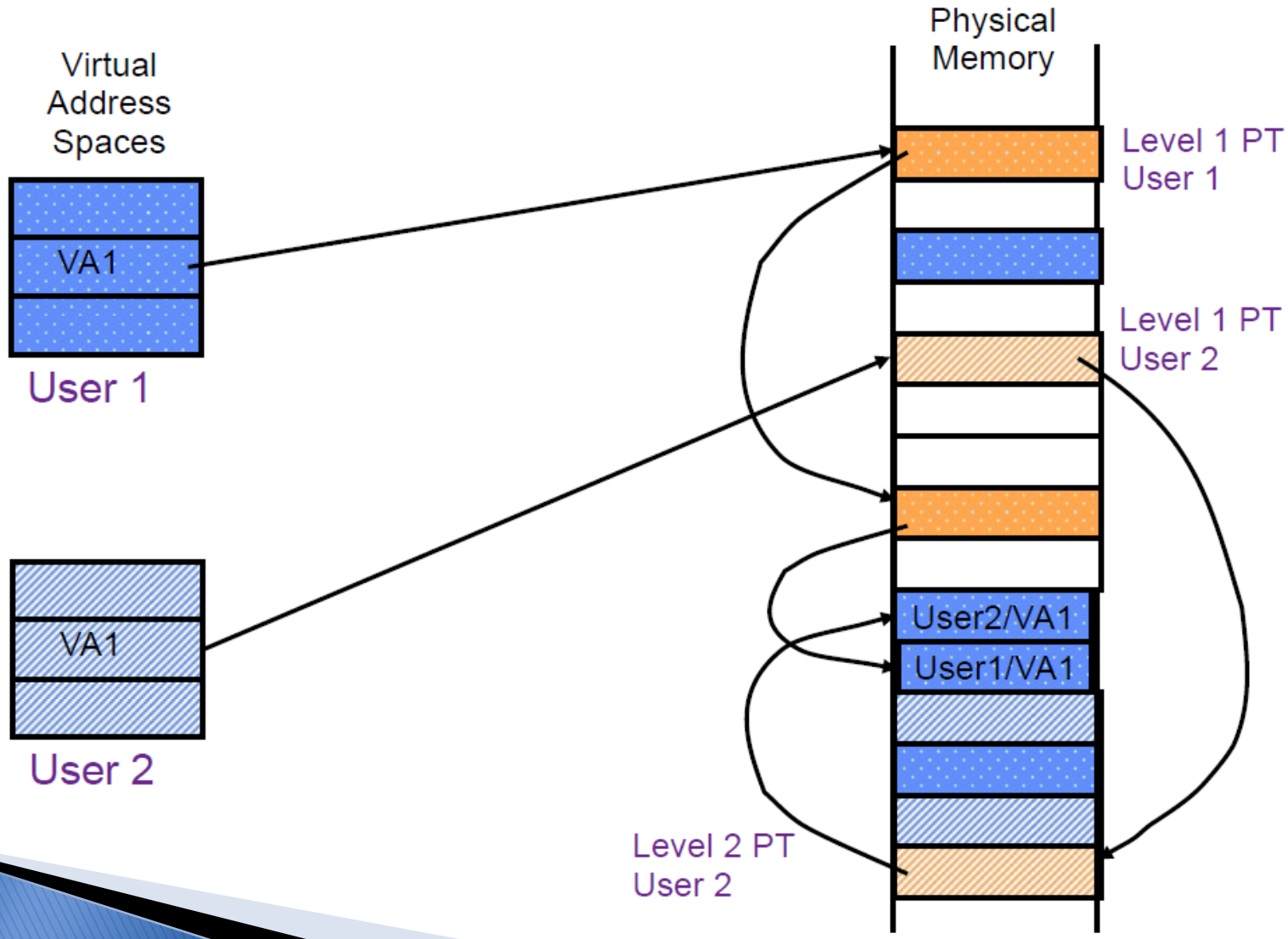


Hierarchical Page Table

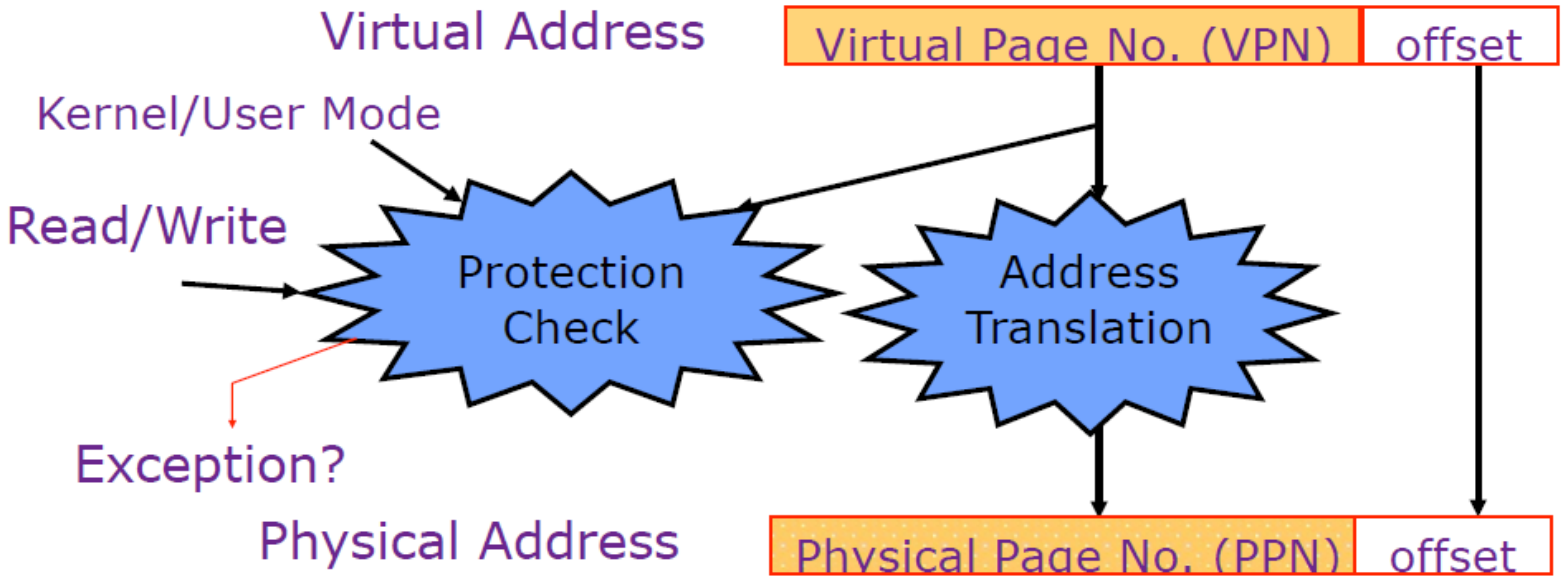


Think of multi-level cache!

Two-Level Page Tables in Physical Memory

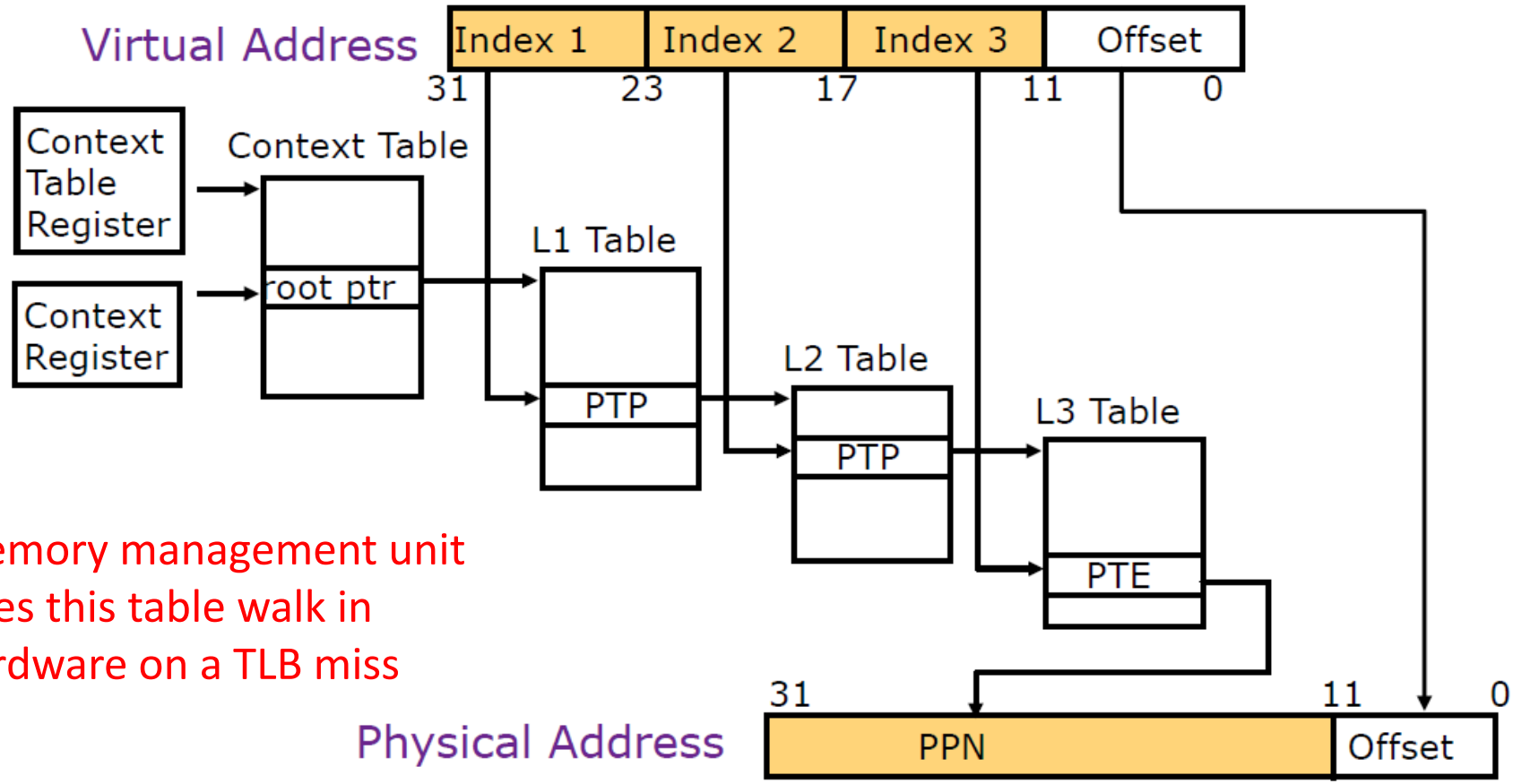


Address Translation & Protection



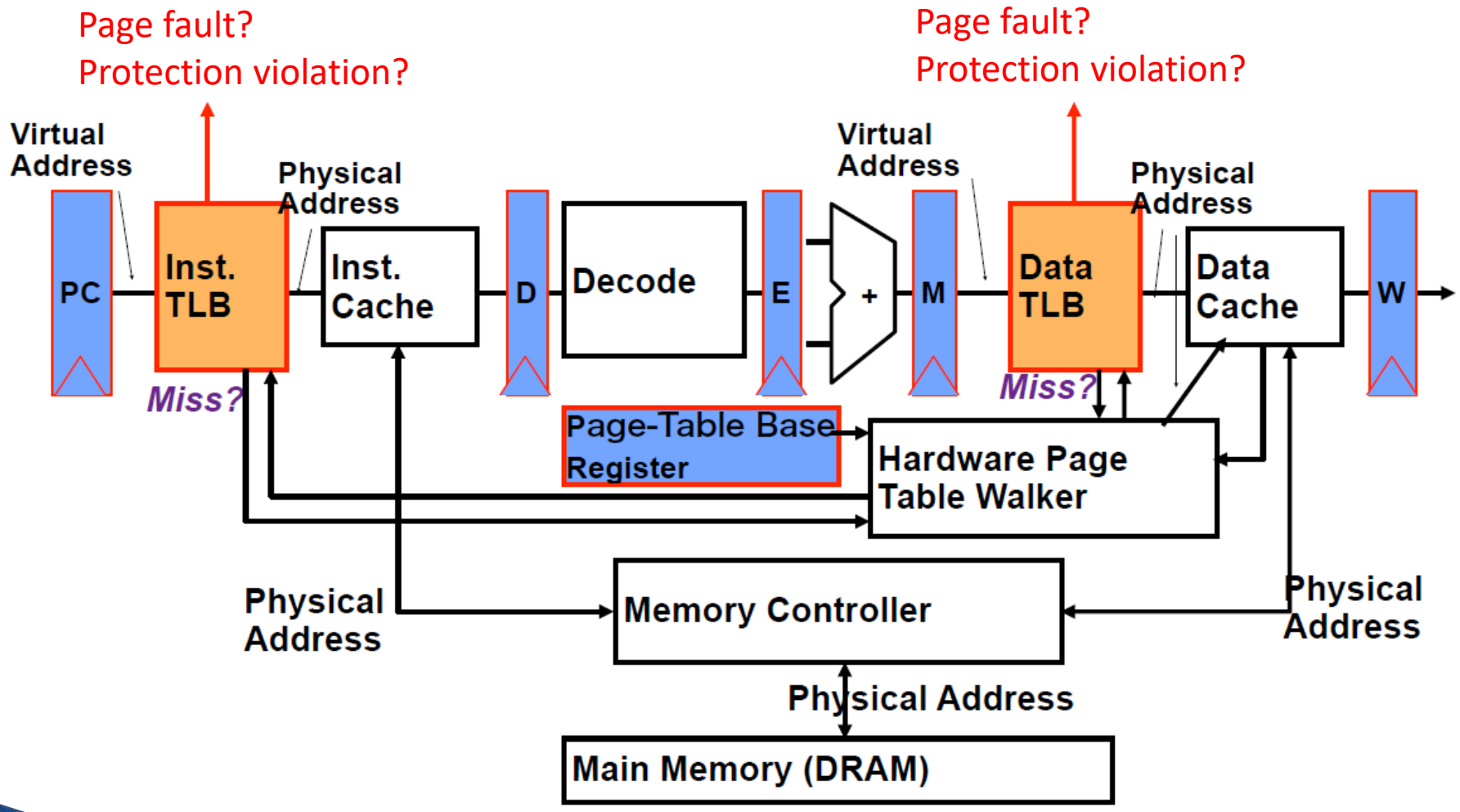
- Every instruction and data access needs address translation and protection checks
- A good VM design needs to be fast (~ one cycle) and space efficient

Hierarchical Page Table Walk: SPARC v8



Memory management unit does this table walk in hardware on a TLB miss

Page-Based Virtual-Memory Machine



Assumes page tables held in untranslated physical memory