ALU test specification

Justyna Rudnicka 303291

1. General test specification

The testbench is to be written in such a way, that all lines of code are executed (coverage close to 100%). It needs to test all lines of the DUT.

2. List of tests

1. Execute all of the following commands:

Name	CMD_CODE	description
CMD_NOP	8'b00000000	Do nothing
AND	8'b00000001	logic AND of all inputs
OR	8'b00000010	logic OR of all inputs
XOR	8'b00000011	logic XOR of all inputs
ADD	8'b00010000	sum of all inputs
SUB	8'b00100000	Difference between the first input and the others

2. Execute each command twice in a row
3. Execute all operations after reset
4. Execute reset after all operations
5. Execute a multi-cycle operation after a single-cycle operation (and vice versa) Note: as of lab01 no multicycle operations
6. Test random combinations of commands and reset
7. Test corner combinations: all zeros and all ones for all operations, both for maximum and minimum amount of data
8. Test all status flags:

Name	STATUS_CODE	description
S_NO_ERROR	8'b00000000	Data processed correctly
S_MISSING_DATA	8'b00000001	Not enough input data
S_DATA_STACK_OVERFLOW	8'b00000010	Exceeded max no of arguments
S_OUTPUT_FIFO_OVERFLOW	8'b00000100	Result not possible to process
S_DATA_PARITY_ERROR	8'b00100000	Data parity bit error
S_COMMAND_PARITY_ERROR	8'b01000000	Command parity bit error
S_INVALID_COMMAND	8'b10000000	Unknown command