CPSC 359 – Digital Logic Tutorial #3

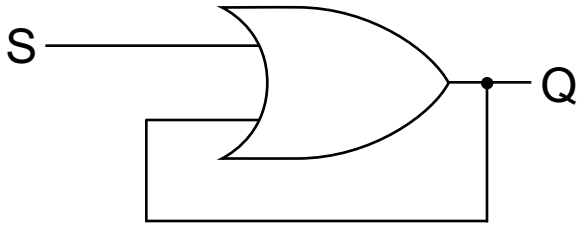
Latches and Flip-Flops

Andrew Kuipers

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$



Latches

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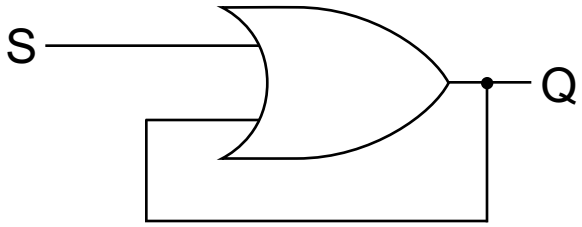
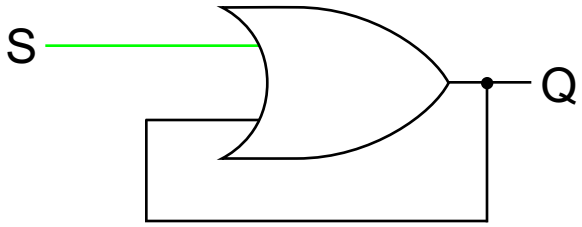


t	S	Q
0	0	0
1		
2		

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$

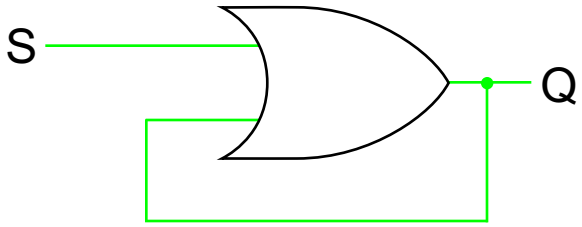


t	S	Q
0	0	0
1	1	
2		

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$

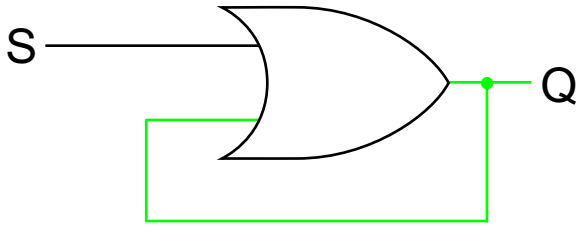


t	S	Q
0	0	0
1	1	1
2		

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$

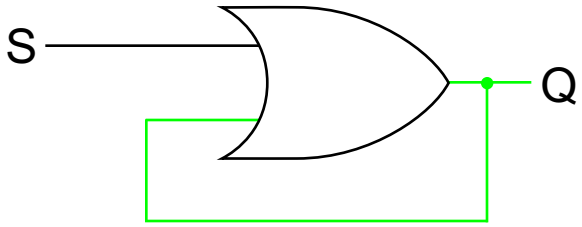


t	S	Q
0	0	0
1	1	1
2	0	

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$

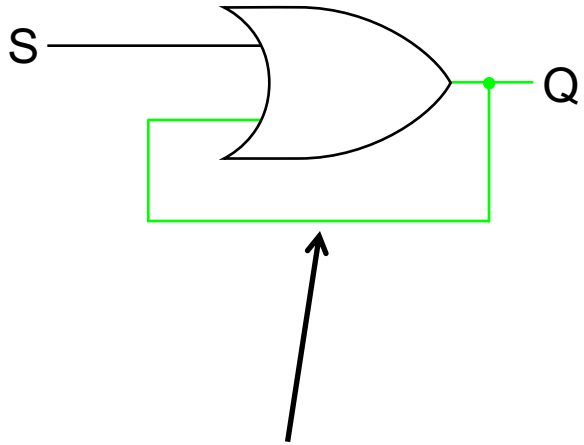


t	S	Q
0	0	0
1	1	1
2	0	1

Latches

Feedback and Latching

$$Q_t = S \vee Q_{t-1}$$



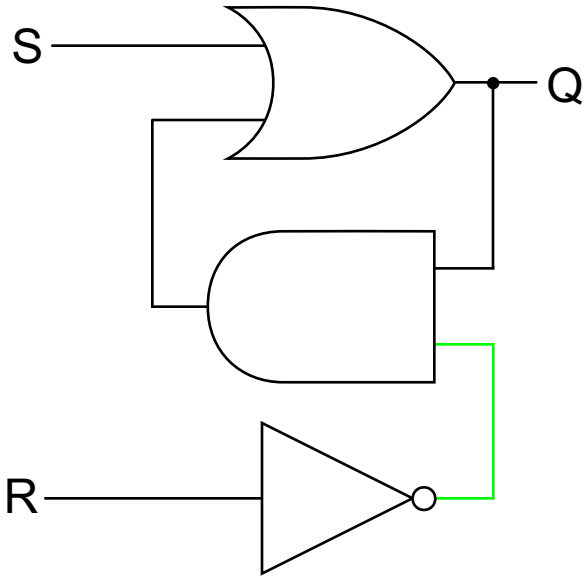
t	S	Q
0	0	0
1	1	1
2	0	1

How can we turn off this line?

Latches

Feedback and Latching

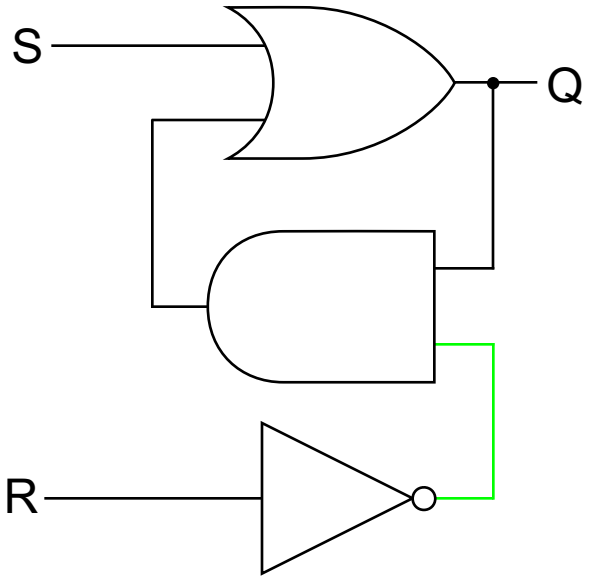
$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$



Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

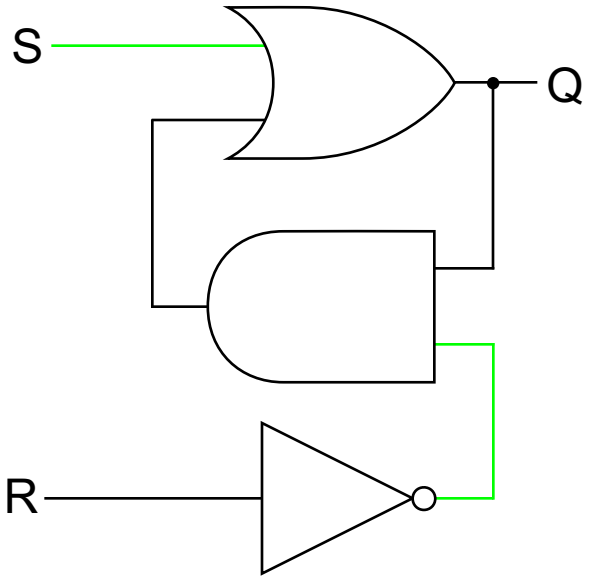


t	S	R	Q
0	0	0	0
1			
2			
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

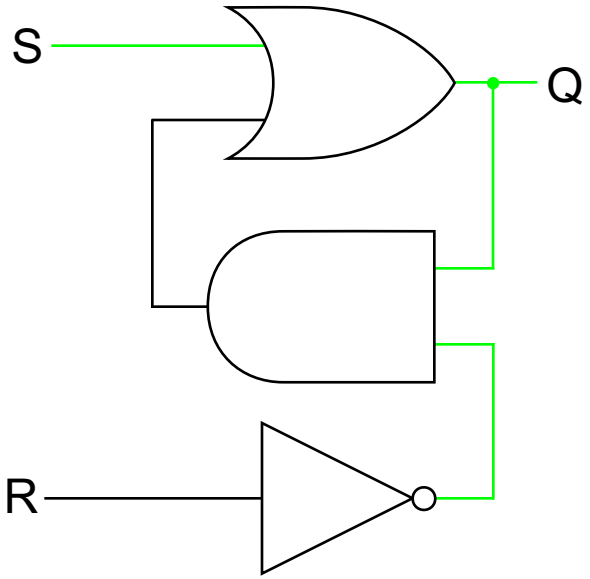


t	S	R	Q
0	0	0	0
1	1	0	
2			
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

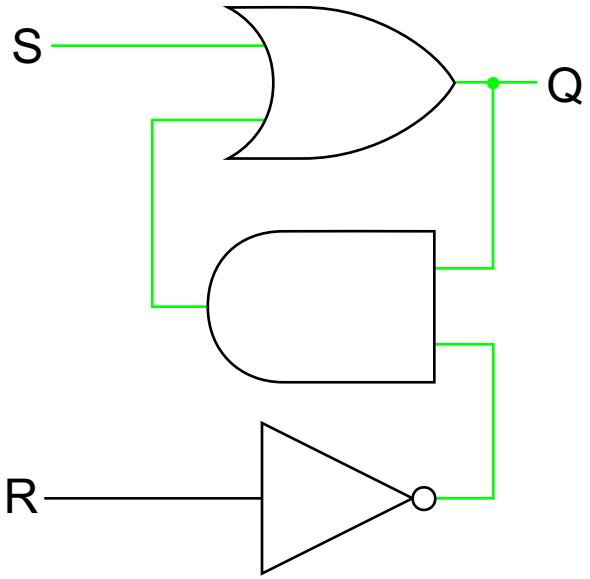


t	S	R	Q
0	0	0	0
1	1	0	1
2			
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

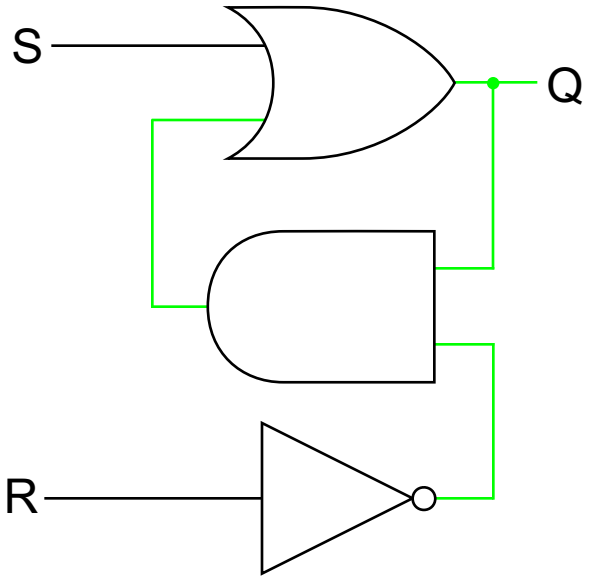


t	S	R	Q
0	0	0	0
1	1	0	1
2			
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

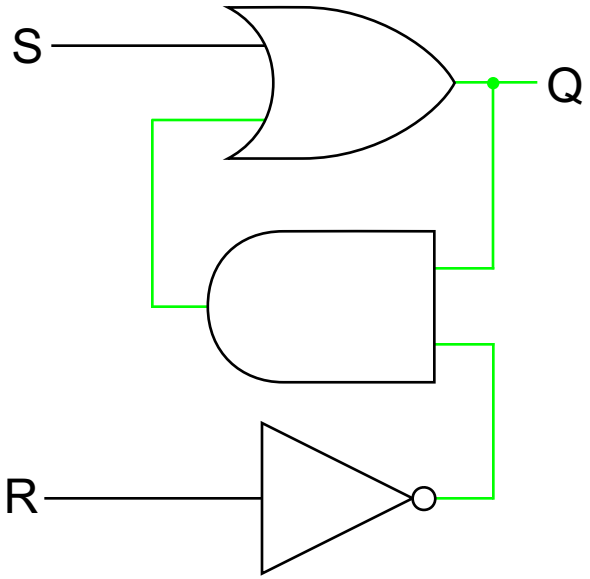


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

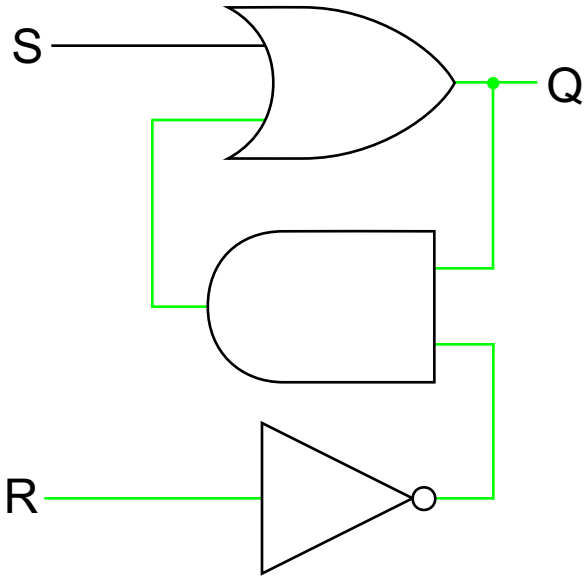


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3			
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

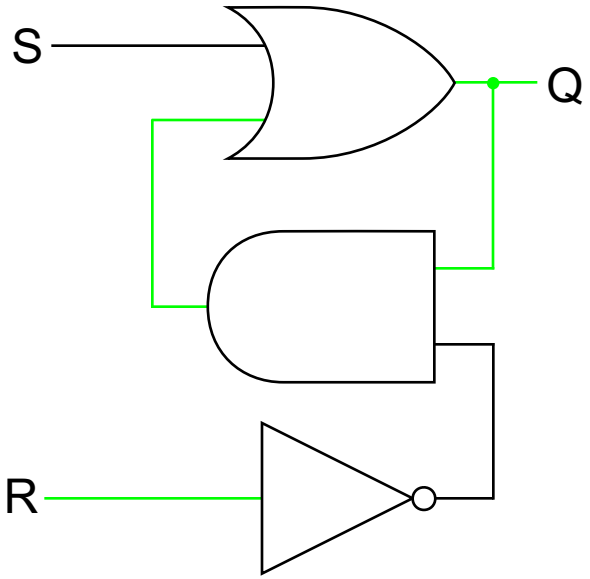


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

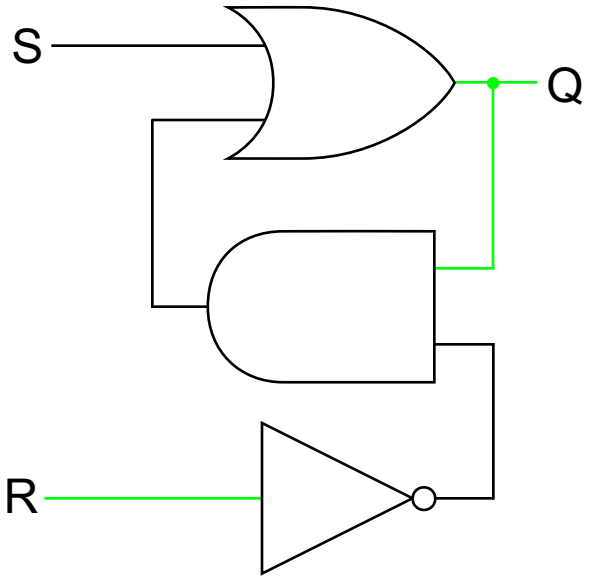


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

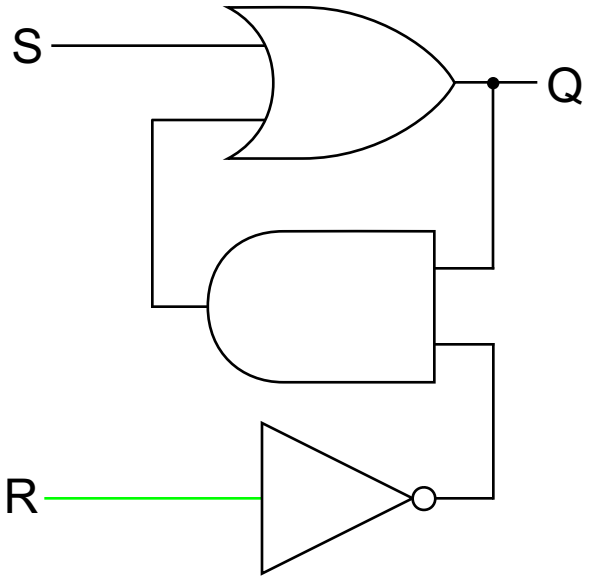


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

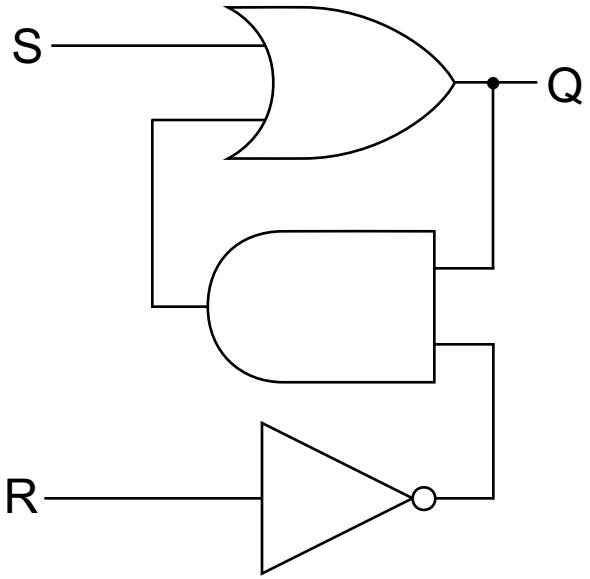


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	0
4			

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

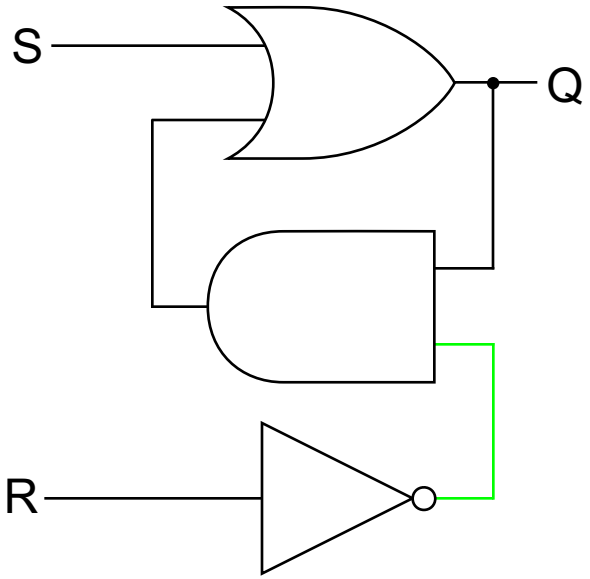


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	0
4	0	0	

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

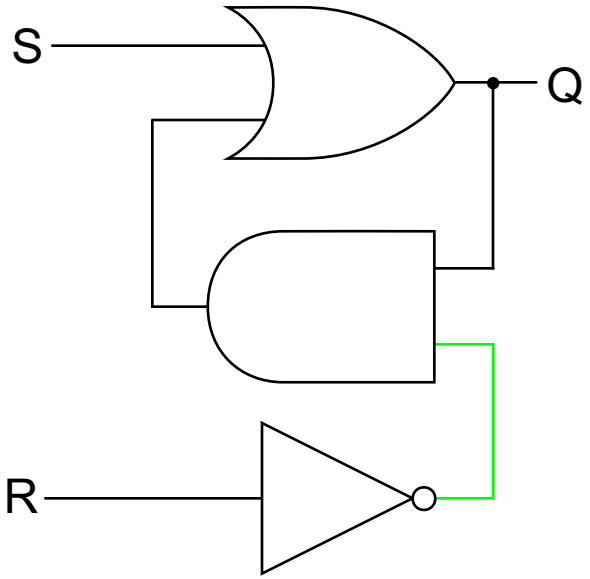


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	0
4	0	0	

Latches

Feedback and Latching

$$Q_t = S \vee (Q_{t-1} \wedge \neg R)$$

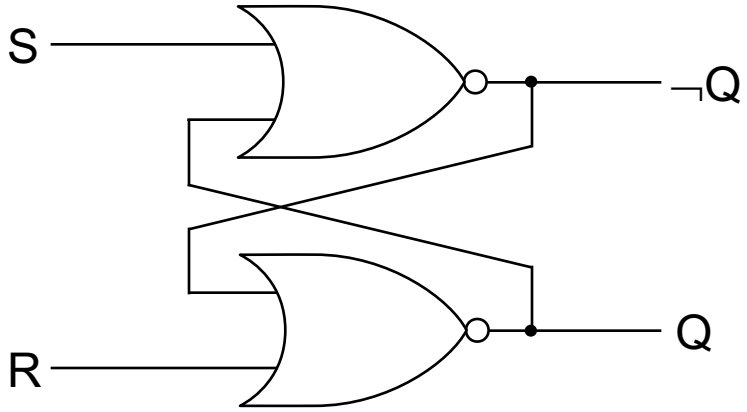


t	S	R	Q
0	0	0	0
1	1	0	1
2	0	0	1
3	0	1	0
4	0	0	0

Latches

SR Latch

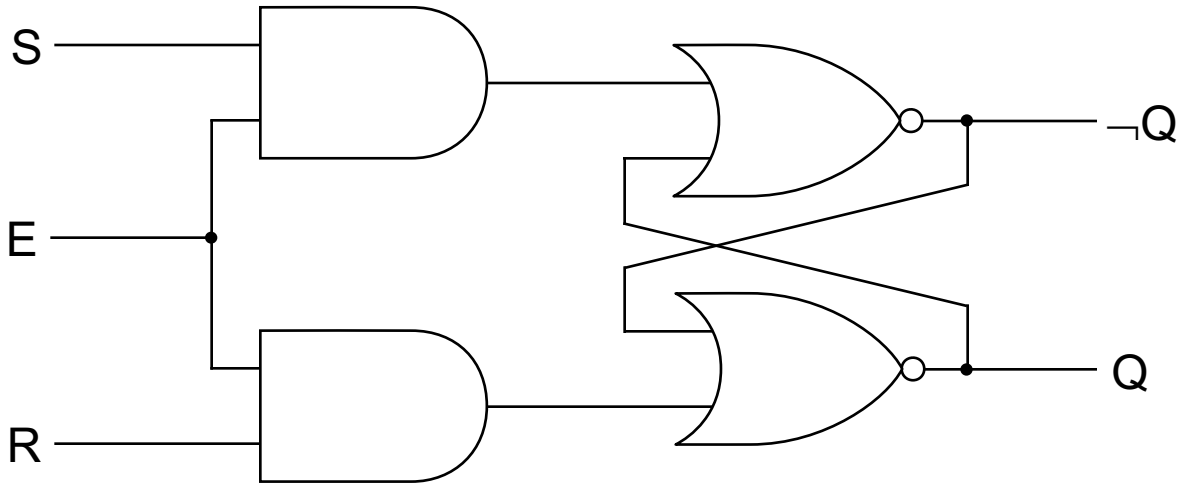
$$Q = \neg(R \vee \neg Q)$$
$$\neg Q = \neg(S \vee Q)$$



Latches

Gated SR Latch

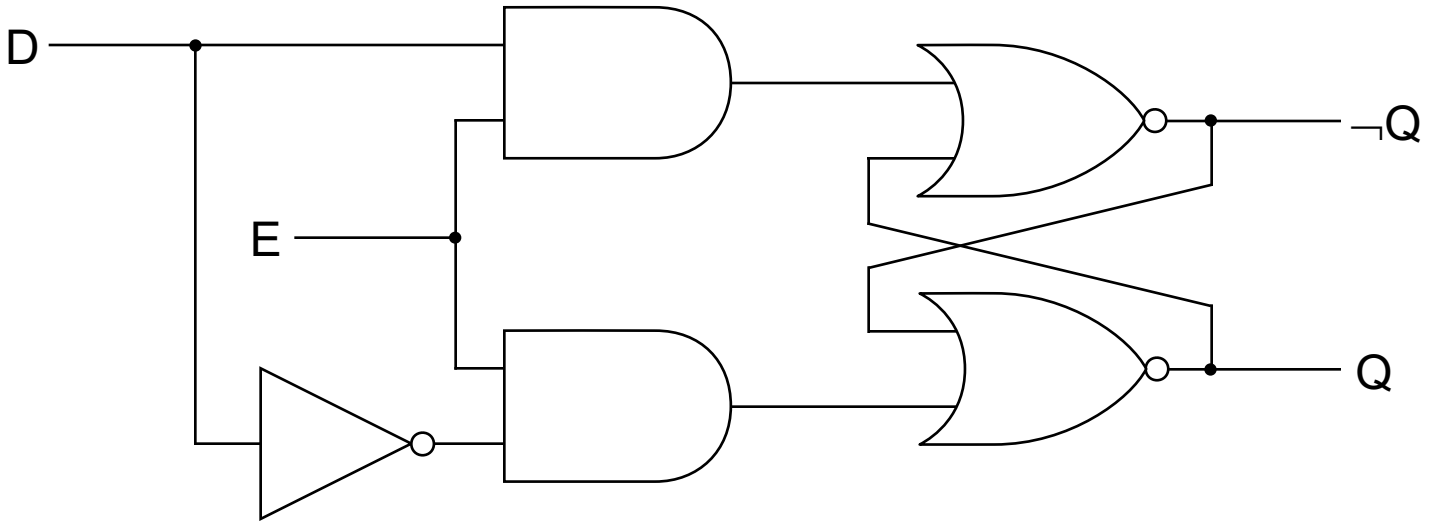
$$Q = \neg((R \wedge E) \vee \neg Q)$$
$$\neg Q = \neg((S \wedge E) \vee Q)$$



Latches

Gated D Latch

$$Q = \neg((\neg D \wedge E) \vee \neg Q)$$
$$\neg Q = \neg((D \wedge E) \vee Q)$$



Latches

Exercise

1. Create a new circuit with 4 D Latches (as imported modules)

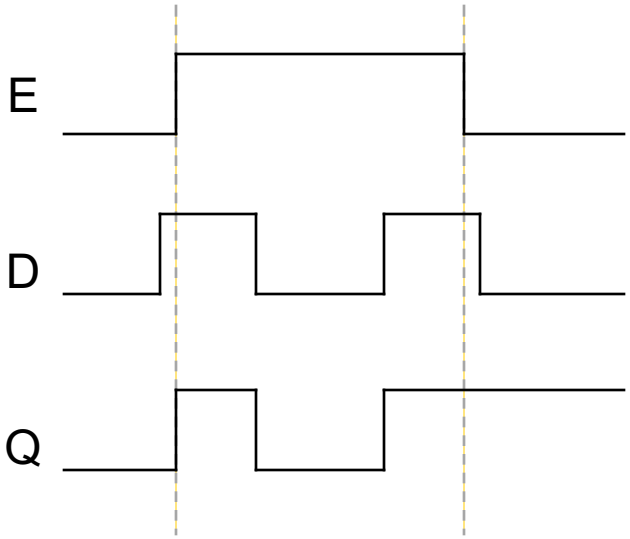
2. Use an Input component to select which D Latch is enabled
   - Only use the two least significant bits
   - Can use the 2bit Decoder circuit from previous tutorial

3. Selectively set and clear different D Latches

Flip-Flops

Level Trigger vs Edge Trigger

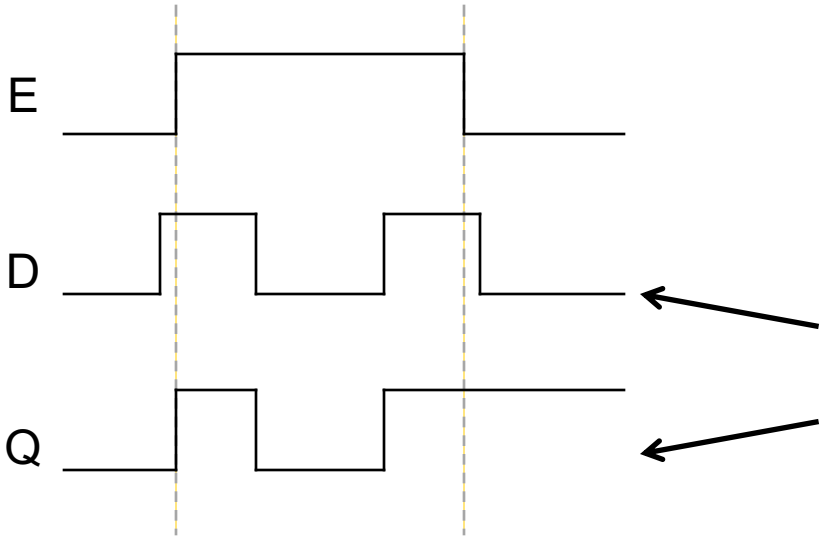
Level Trigger



Flip-Flops

Level Trigger vs Edge Trigger

Level Trigger



Changes in D create changes in Q at any point while E is high

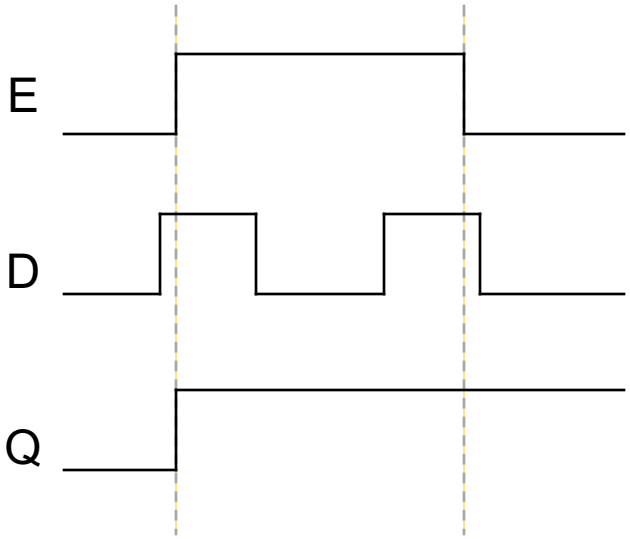
Flip-Flops

Level Trigger vs Edge Trigger

Flip-Flops

Level Trigger vs Edge Trigger

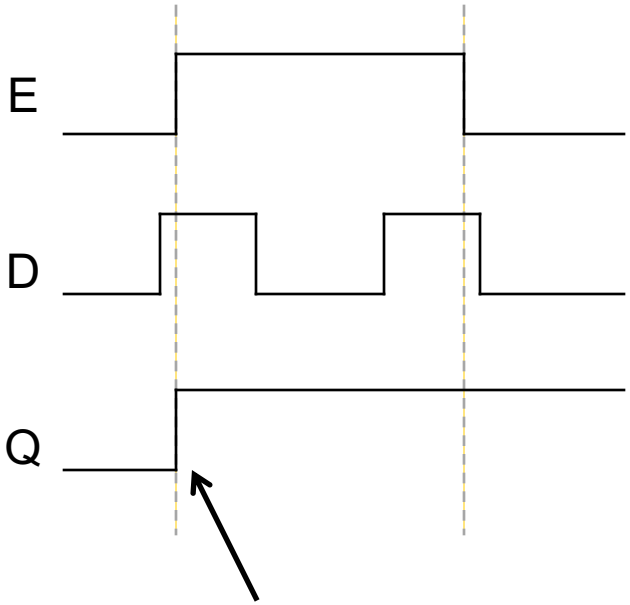
Positive Edge Trigger



Flip-Flops

Level Trigger vs Edge Trigger

Positive Edge Trigger

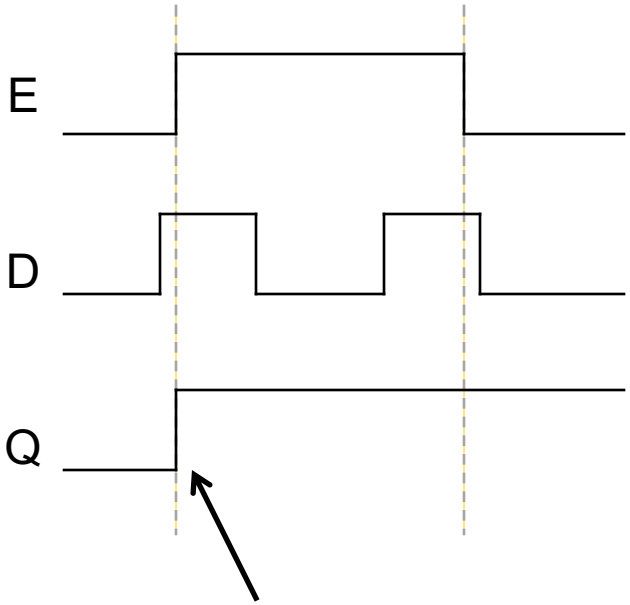


Only change on rising edge of E

Flip-Flops

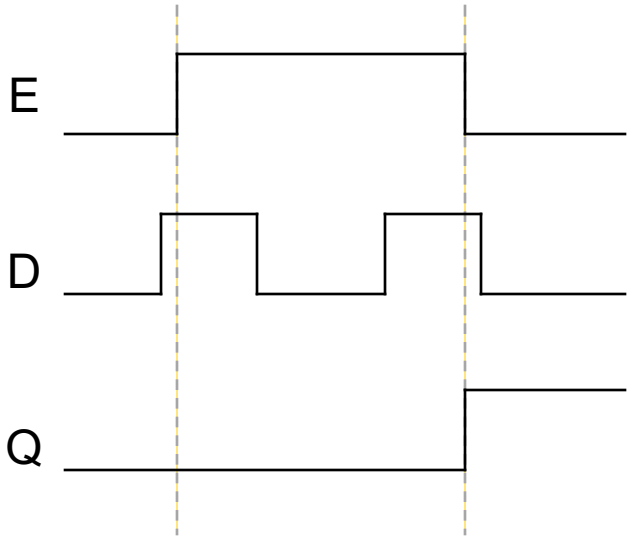
Level Trigger vs Edge Trigger

Positive Edge Trigger



Only change on rising edge of E

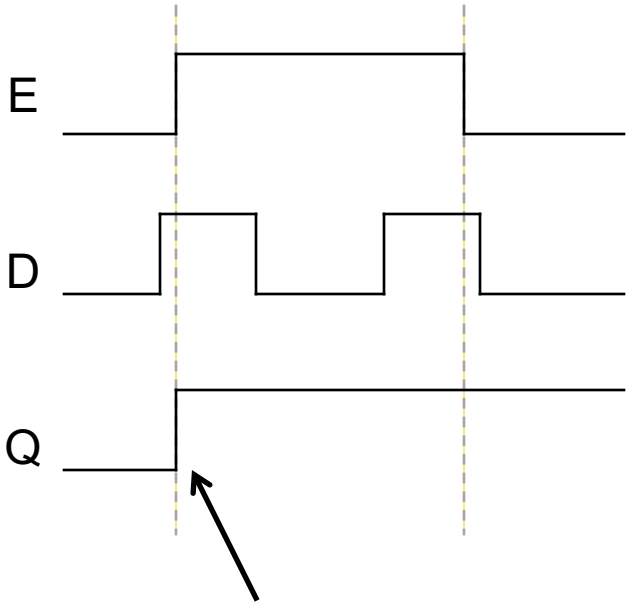
Negative Edge Trigger



Flip-Flops

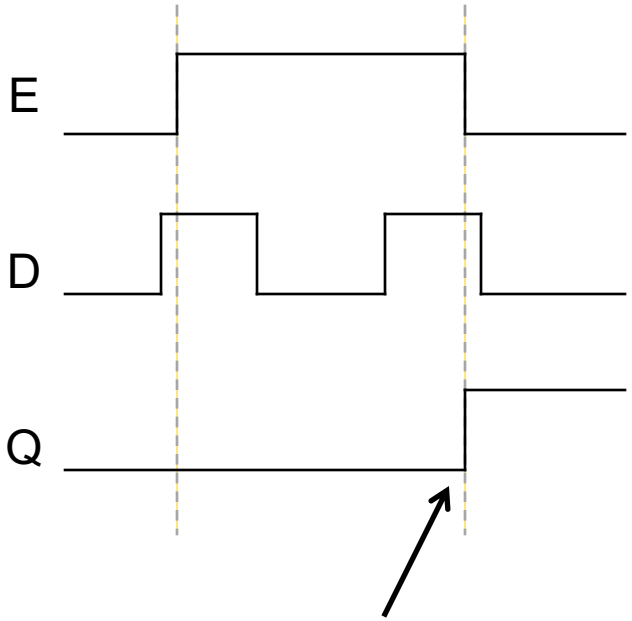
Level Trigger vs Edge Trigger

Positive Edge Trigger



Only change on rising edge of E

Negative Edge Trigger



Only change on falling edge of E

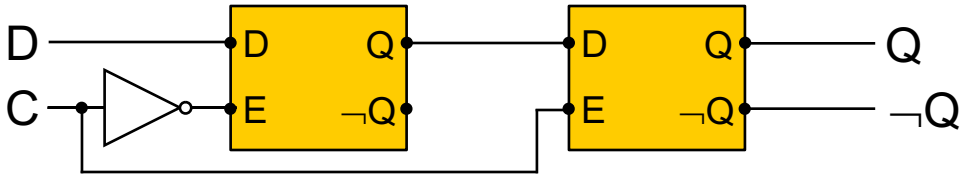
Flip-Flops

Master-Slave D Flip-Flop

Flip-Flops

Master-Slave D Flip-Flop

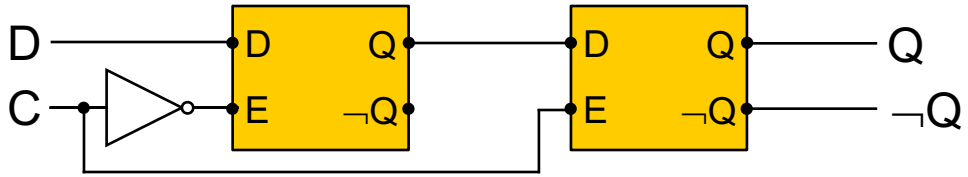
Positive Edge Triggered



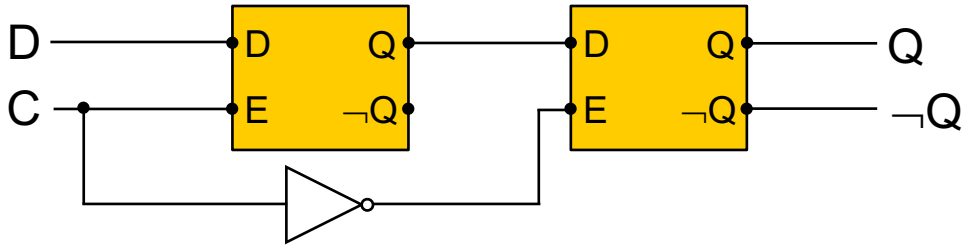
Flip-Flops

Master-Slave D Flip-Flop

Positive Edge Triggered

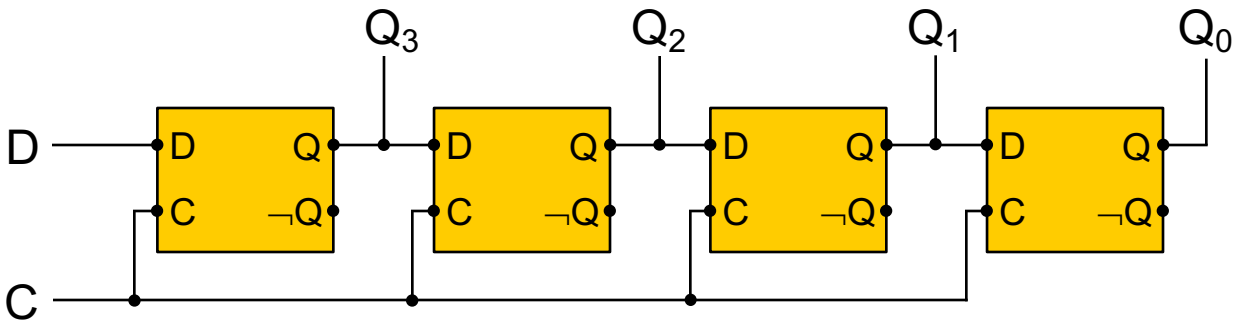


Negative Edge Triggered



Flip-Flops

Example – Shift Register



Data is right-shifted through the register on each triggering edge (neg. or pos.)

Flip-Flops

Exercise

1. Create a 4bit register using D Flip-Flops
   - 4 input “load” lines
   - 4 output “value” lines
   - 1 load enable line (clock line)

2. Create a new circuit, add 4 of these registers as modules

3. Combine with 2bit Decoder to select which register is enabled

4. Load different values into these registers using an Input component

Flip-Flops

Challenge

Create a simple adding machine:

- Select input values from two of four 4bit registers
  - Need to be able to load the registers with values as well
- Store sum of input values in any of the four registers
  - Monitor values (inputs, output) for operation