Mapúa Institute of Technology at Laguna
Malayan Colleges Laguna

ECE101-1L – FUNDAMENTALS OF ELECTRONIC CIRCUITS (LAB)

Activity #7: JFET Fundamentals and Application

Objectives:

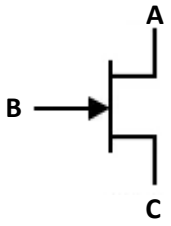
- Describe the effects of drain voltage on drain current at zero gate bias.
- Describe the effect of gate bias on pinch-off
- Observe the drain-to-source current-voltage family of curves
- Measure JFET amplifier dc operating voltages.

Procedures:

A. Multisim

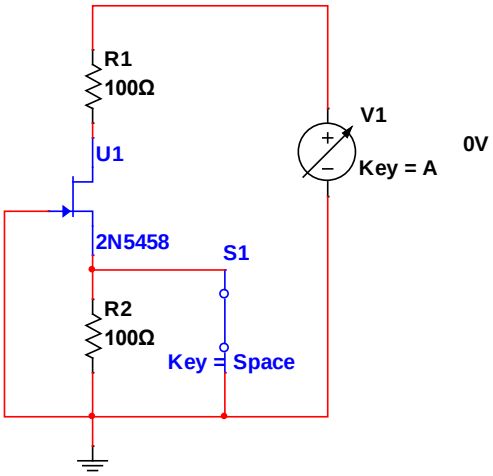
DC Characteristics of JFET

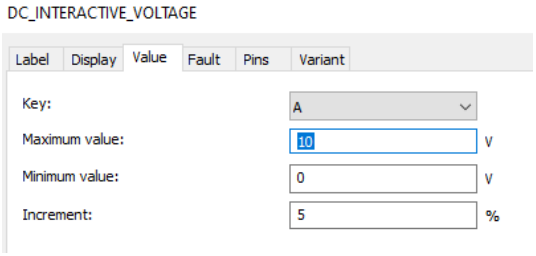
1. Identify the PIN Name of the JFET



2. Identify the Type of JFET shown below

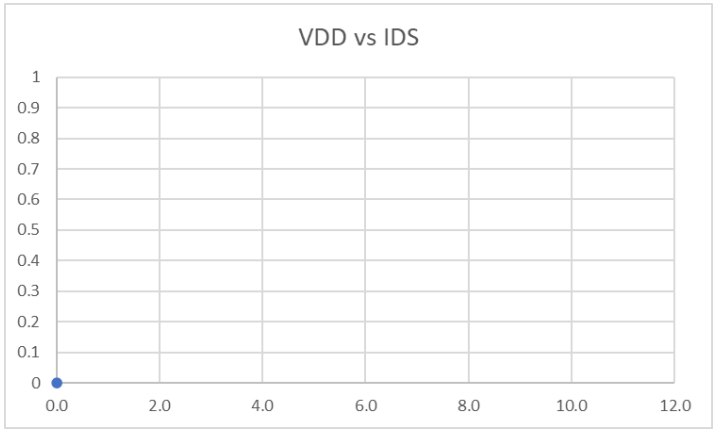
3. Create the circuit below using Multisim, and change the DC INTERACTIVE VOLTAGE Settings shown below





4. Adjust the V1 Voltage base on the table below and measure the Current flowing through R2 *(make sure Ammeter is not connected in parallel).*
   a. Complete the table below (*Make sure the units are correct*)
   b. Graph the values obtain (use MSEXCEL or any spreadsheet software)

VDD	IDS (A)
0.0	0
0.5	
1.0	
1.5	
2.0	
2.5	
3.0	
3.5	
4.0	
4.5	
5.0	
6.0	
7.0	
8.0	
9.0	
10.0	



5. Base on the table does the value of drain current increase or decrease with drain voltage?

_____

_____

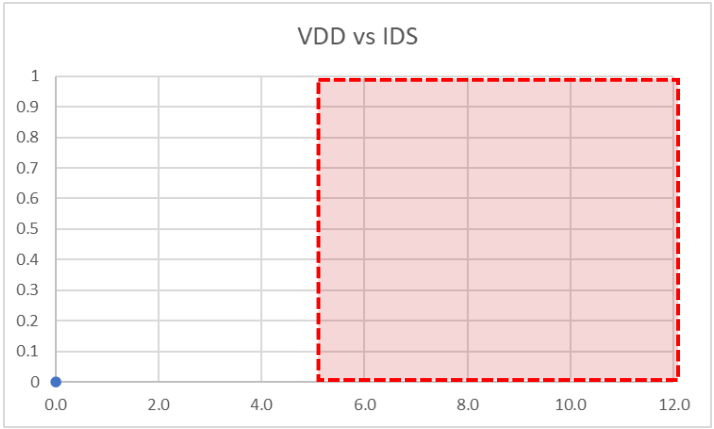
6. What gate bias is provided by your test circuit and why?

_____

_____

7. Base on your graph 2.b identify the transition point from ohmic region to the constant current region. Place a rectangle with Border to pinpoint *See sample below*

   To know more about ohmic region and Constant Current visit link:
   https://www.tutorialspoint.com/basic_electronics/basic_electronics_jfet.htm



8. Base on your answer in Q5 what is the value of pinch-off voltage?

   Vp = _____Vdc

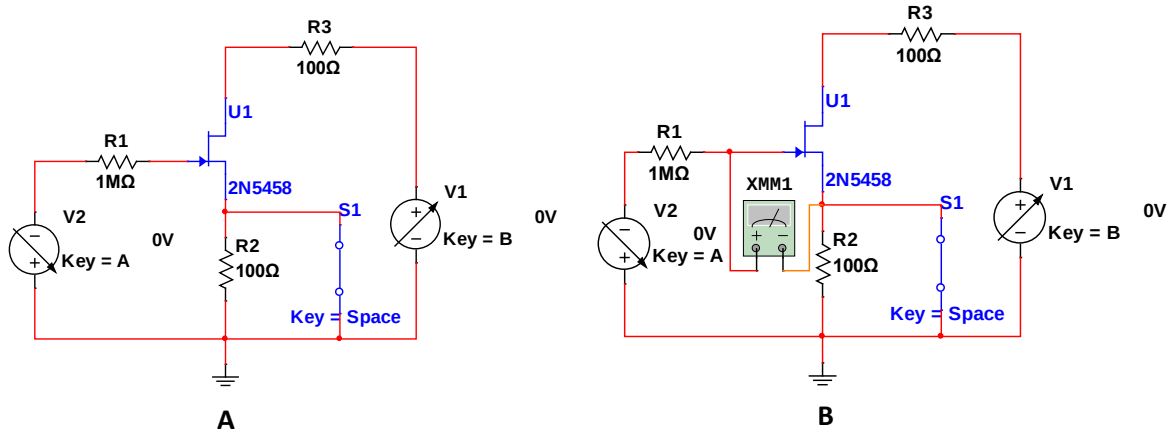
9. In the Ohmic region of you curve, does the drain current increase or decrease with drain voltage?

   _____

   _____

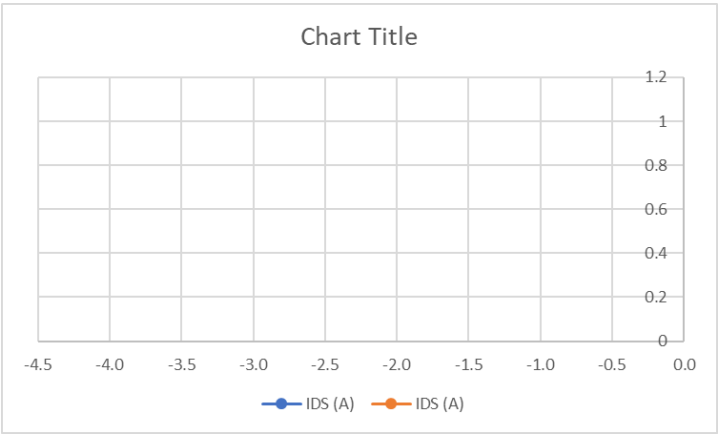
Effect of Gate Bias on Pinch-off

10. Create the circuit shown below (**A** only)



11. Place a multimeter on the Gate-Source Junction (*Refer to Diagram B for placement of Multimeter).* Adjust the V2 to obtain Gate-to-source bias (VGS) of 0V and Adjust V1 supply to 10V DC.
    a. Complete the Table shown below (*No need for schematic screenshot*)
       Values may vary between 0mA to 20mA
    b. Plot the 2 IDS in same chart

	V1 = 10 V	V1 = 5 V
V2	IDS (A)	IDS (A)
-4.0		
-3.5		
-3.0		
-2.5		
-2.0		
-1.0		
-0.5		



12. Based on your results, did the gate bias voltage needed to turn off the JFET Increase, remain about the same, or decrease as the drain voltage changed?

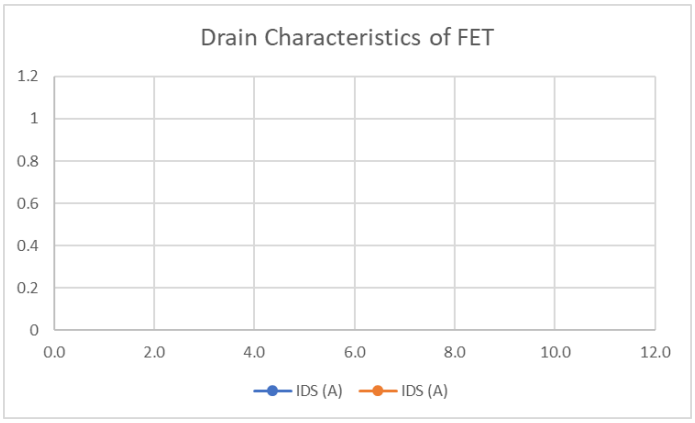
_____
_____

13. Based on your table data, does an increase in the gate bias voltage output result in an increase or a decrease in the pinch-off (saturation) current of JFET?

_____
_____

14. Adjust the V2 voltage for -0.5V. using the V1 Values in the table below
    a. Complete the IDS Column. Repeat your test using a -2V value for V1.
    b. Plot the 2 curves on same graph label each plot for the specific VGG (-0.5 and -2)

	V2 = -0.5 V	V2 = -2 V
V1	IDS (A)	IDS (A)
0.0		
0.5		
1.0		
1.5		
2.0		
2.5		
3.0		
3.5		
4.0		
4.5		
5.0		
6.0		
7.0		
8.0		
10.0		



15. Based on your data and plots, what effect did a higher value of bias voltage have on the pinch-off saturation point of the JFET under test?

_____
_____

Discussions:

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_____
_____
_____

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