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02-03-2022

ECE101-1L – FUNDAMENTALS OF ELECTRONIC CIRCUITS (LAB)

Activity #7: JFET Fundamentals and Application

A. Multisim

DC Characteristics of JFET

1. Identify the PIN Name of the JFET

A – DRAIN

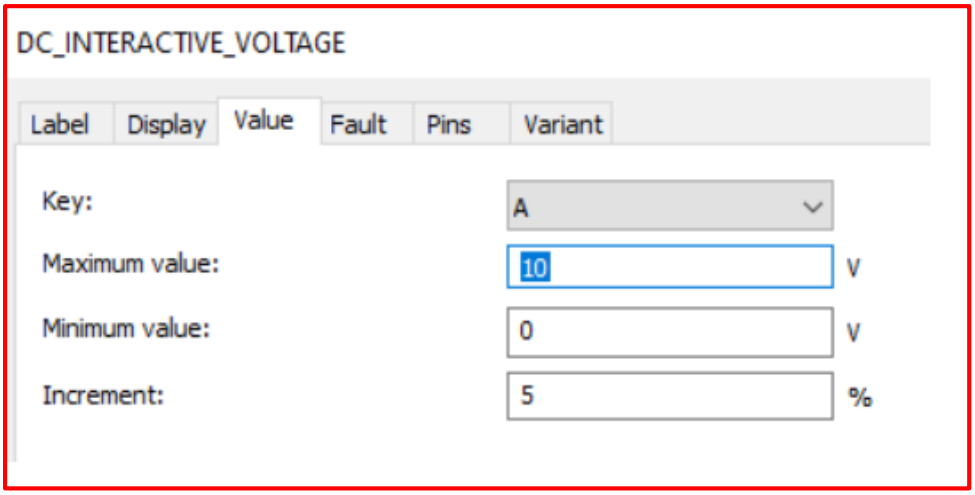
B – GATE

C - SOURCE

2. Identify the Type of JFET shown below

A. **N-Channel JFET**
B. **P-Channel JFET**

3. Create the circuit below using Multisim, and change the DC INTERACTIVE VOLTAGE Settings shown below



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4. Adjust the V1 Voltage base on the table below and measure the Current flowing through R2 (make sure Ammeter is not connected in parallel).

a. Complete the table below (Make sure the units are correct)

b. Graph the values obtain (use MSEXCEL or any spreadsheet software)

VDD	IDS (A)
0.0	0
0.5	0.001268
1.0	0.002445
1.5	0.003522
2.0	0.004487
2.5	0.005328
3.0	0.006026
3.5	0.00657
4.0	0.006927
4.5	0.007069
5.0	0.007099
6.0	0.007159
7.0	0.007218
8.0	0.007278

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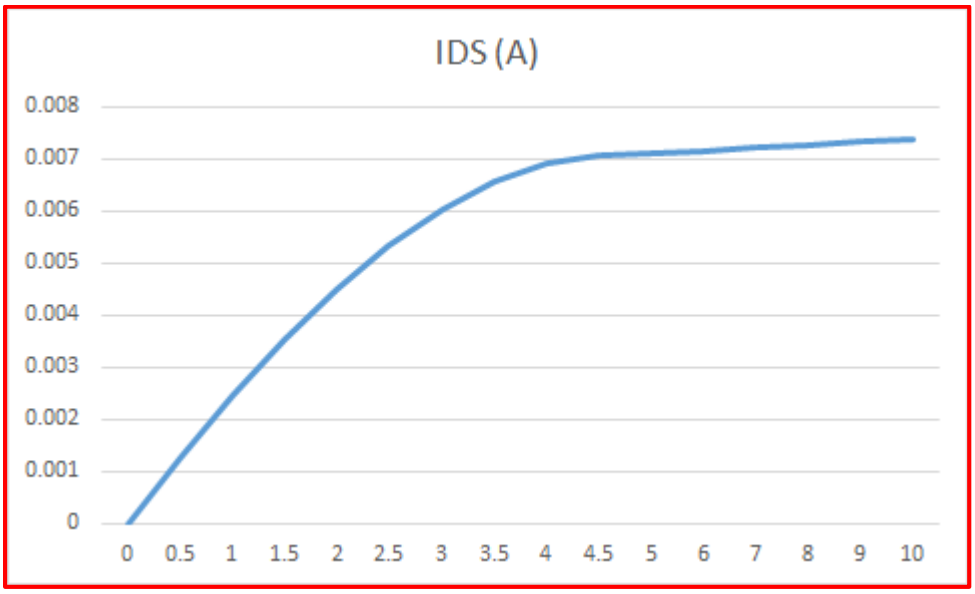
9.0	0.007337
10.0	0.007397



5. Base on the table does the value of drain current increase or decrease with drain voltage?

When the drain value of voltage increases the drain current also increases.

6. What gate bias is provided by your test circuit and why?

The gate introduces negative voltage on entry that's why it's a negative bias

7. Base on your graph 2.b identify the transition point from ohmic region to the constant current region. Place a rectangle with Border to pinpoint See sample below

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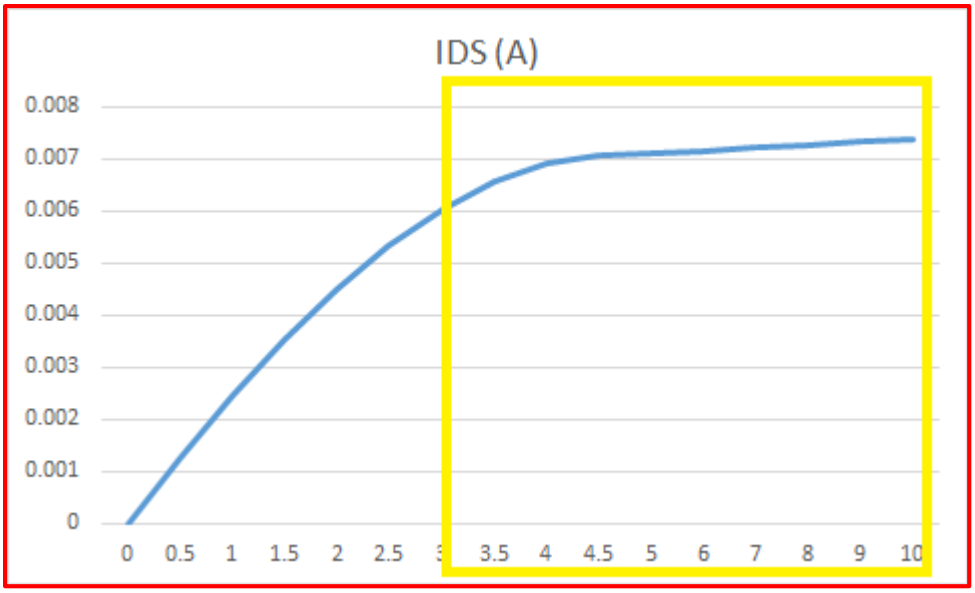

To know more about ohmic region and Constant Current visit link:

https://www.tutorialspoint.com/basic_electronics/basic_electronics_jfet.htm

8. Base on your answer in Q5 what is the value of pinch-off voltage?

Vp = 4.0 Vdc

9. In the Ohmic region of you curve, does the drain current increase or decrease with drain voltage?

When the drain value of voltage increases the drain current also increases.

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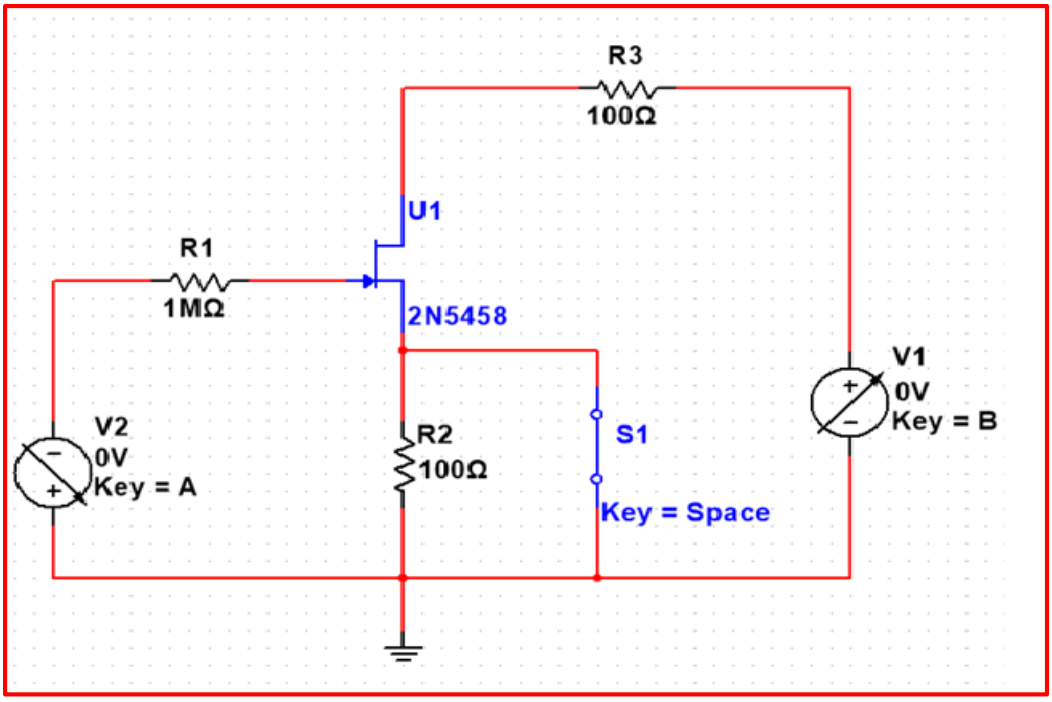
Effect of Gate Bias on Pinch-off

10. Create the circuit shown below (A only)



11. Place a multimeter on the Gate-Source Junction (Refer to Diagram B for placement of Multimeter). Adjust the V2 to obtain Gate-to-source bias (VGS) of 0V and Adjust V1 supply to 10V DC

a. Complete the Table shown below (No need for schematic screenshot) Values may vary between 0mA to 20mA

b. Plot the 2 IDS in same chart

	V1 = 10V	V1 = 5V
V2	IDS (A)	IDS (A)
-4.0	0.000004	0.000004
-3.5	0.0000035	0.0000035
-3.0	0.000003	0.000003
-2.5	0.0000025	0.0000025
-2.0	0.000002	0.000002

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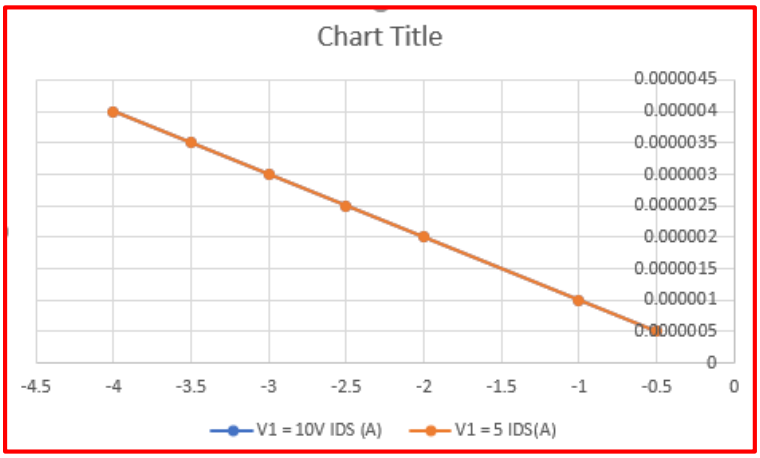
-1.0	0.000001	0.000001
-0.5	5.00008E-7	5.00003E-7



12. Based on your results, did the gate bias voltage needed to turn off the JFET Increase, remain about the same, or decrease as the drain voltage changed?

- Just as the drain voltage changed, the gate bias voltage remains the same.

13. Based on your table data, does an increase in the gate bias voltage output result in an increase or a decrease in the pinch-off (saturation) current of JFET?

- As shown in the table above, the decreasing current is caused by the increasing gate bias voltage.

14. Adjust the V2 voltage for -0.5V. using the V1 Values in the table below

a. Complete the IDS Column. Repeat your test using a -2V value for V1.

b. Plot the 2 curves on same graph label each plot for the specific VGG (-0.5 and -2)

	V2 = -0.5V	V2 = -2V
V1	IDS (A)	IDS (A)
0.0	0.0000005	0.000002
0.5	0.0000005	0.000002

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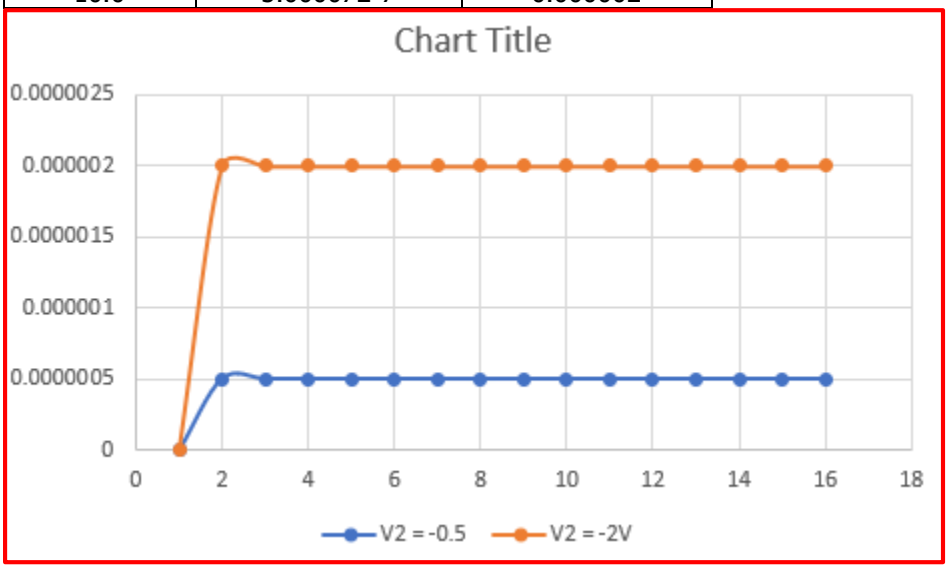
1.0	0.0000005	0.000002
1.5	5.00001E-7	0.000002
2.0	5.00001E-7	0.000002
2.5	5.00001E-7	0.000002
3.0	4.99843E-7	0.000002
3.5	5.00002E-7	0.000002
4.0	5.00002E-7	0.000002
4.5	5.00003E-7	0.000002
5.0	5.00003E-7	0.000002
6.0	5.00004E-7	0.000002
7.0	5.00005E-7	0.000002
8.0	5.00006E-7	0.000002
10.0	5.00007E-7	0.000002



15. Based on your data and plots, what effect did a higher value of bias voltage have on the pinch-off saturation point of the JFET under test?

- As shown above, 0.5V has a lower current in contrast to –2V in which it has a higher current.

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Discussions:

From the data collected above the current from source to drain can be controlled by the application voltage on the gate terminal, which is reverse biased. This is a reason that it is known as field effect transistor. When the VDs is positive the depletion region width increases and says otherwise when negative.