Mapúa Institute of Technology at Laguna
Malayan Colleges Laguna

ECE101-1L – FUNDAMENTALS OF ELECTRONIC CIRCUITS (LAB)

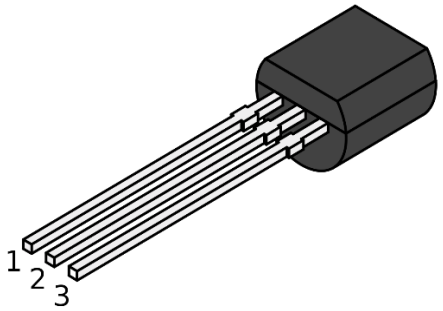
Preliminary Course Assessment

General Instructions:

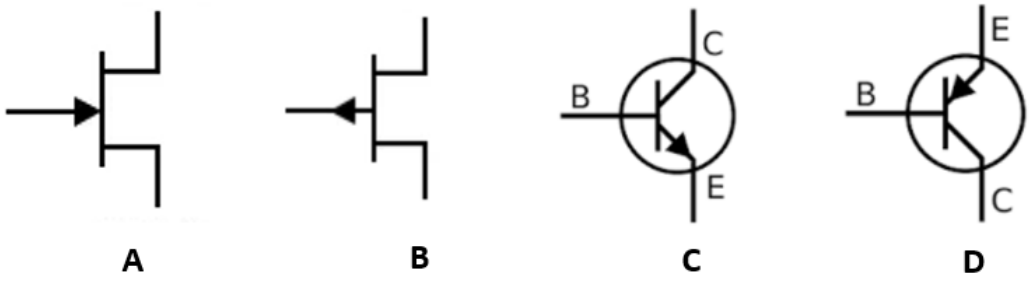
- Read the questions/instructions carefully (there might be trick questions / change in orientations in the figure or drawing)
- Communicate within your group only
- Answer the questions/problems honestly

Procedures:

1. Search for Datasheet for 2N5459 on the Internet and Identify the PIN Name of the JFET
   1. _____
   2. _____
   3. _____



2. Identify the **Specific Type of Transistor** shown below (10 pts)



3. Open the Multisim Included Multisim Attachment and locate the transistor for this question
   a. Is the transistor Q1 in good condition?
      _____
   b. Show your test method(s) *(ex. Using table and test of terminals)*
      _____
   c. Explain your answer in 3.a
      _____

4. On the Same File Attachment Locate the Schematic Diagram for this question
   a. Is the transistor Q4 in good condition?

      _____

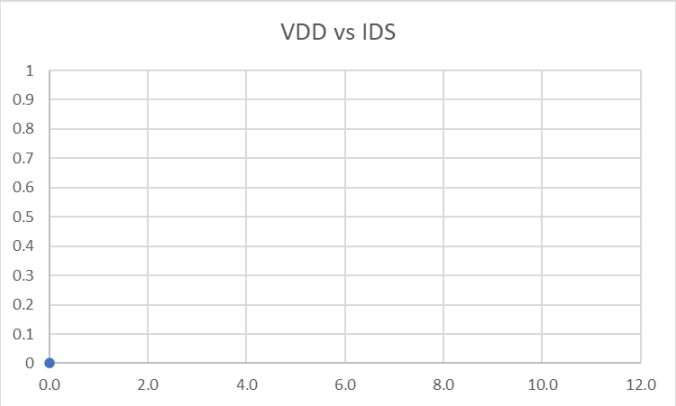
   b. Show your test method(s) *(ex. Using table and test of terminals)*

      _____

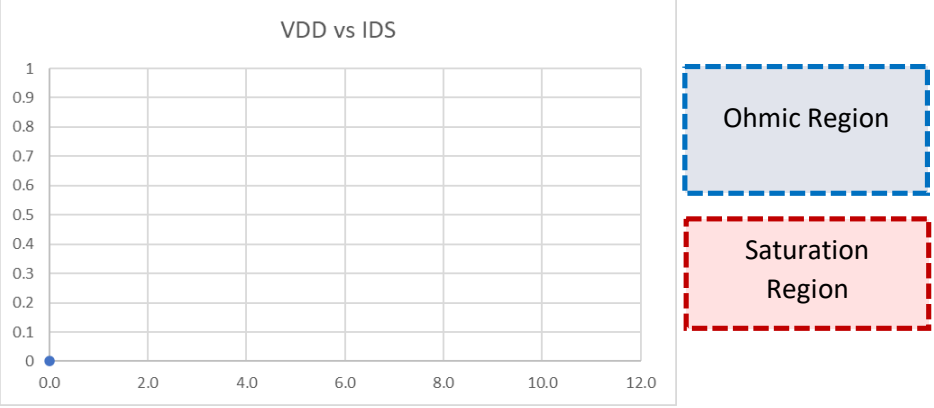
   c. Explain your answer in 4.a

      _____

5. On the Same File Attachment Locate the Schematic Diagram for this question
   a. Simulate and show the graph of V1 vs IDS (Use 0.5 Increments for V1)



   b. Identify the Ohmic Region and the Saturation Region
      i. Use Blue Border Rectangle for Ohmic Region
      ii. Use Red Border Rectangle for Saturation Region



   c. What is the Pinch-off Voltage?
      Vp = _____V

6. On the Same File Attachment Locate the Schematic Diagram for this question
    a. Complete the table below

	VGS= -0.5 V	VGS = -1 V	VGS = -1.5 V	VGS = -2 V
VDD	IDS (A)	IDS (A)	IDS (A)	IDS (A)
0.0				
0.5				
1.0				
1.5				
2.0				
2.5				
3.0				
3.5				
4.0				
4.5				
5.0				
6.0				
7.0				
8.0				
10.0				

    a. Plot the graph of VDD vs IDS
        a. Label each graph base on the VGS value