Jeremy Vuong

HW#5
CSc 137

Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, AND gate = 0.2 ns and EXOR = 0.3 ns determine the upper bound for its clock frequency. (10 pts)

Critical path : $d_0 \rightarrow z_2$

CLA Adder delay = $2(0.3) + 0.2 = 0.8$ ns
(0.3: XOR gate; 0.2: AND gate)

Mux delay = $3(0.2) = 0.6$ ns
(0.2: AND gate)

$T_{st} = 0.1$ ns

$T_{cs} = 0.2$ ns

$T_{cq} = 0.1\text{ns} + 0.1\text{ns} + 2(0.1\text{ns}) = 0.4$
(d_2, d_1, d_0)

T_{min} = CLA delay + mux delay + T_{st} + T_{cs} + T_{cq}

$= 0.8 + 0.6 + 0.1 + 0.2 + 0.4 =$

$= 2.1$ ns

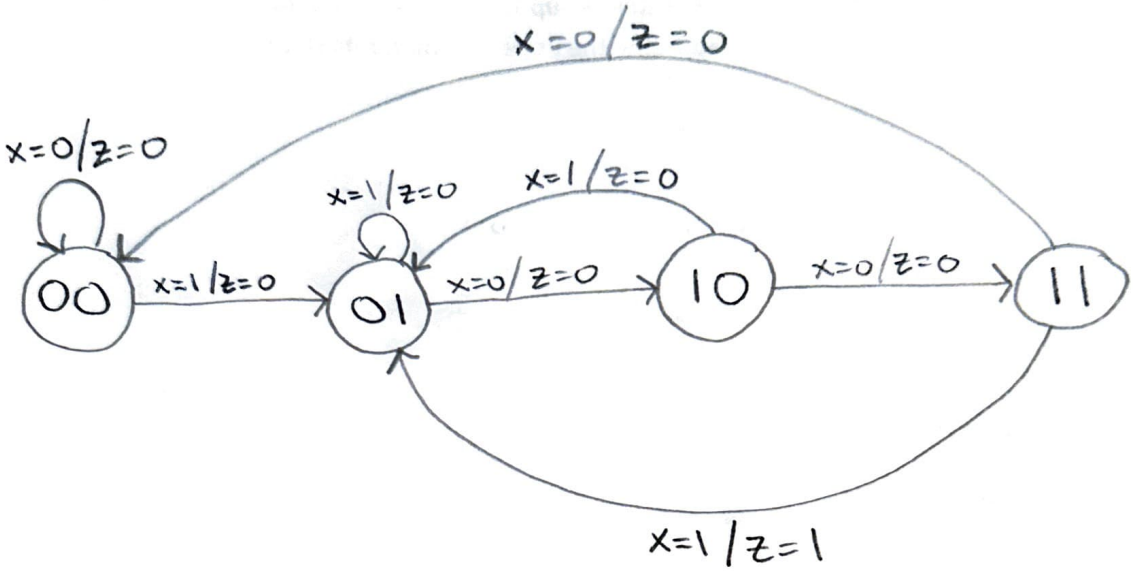
$f_{max} = 1/T = \frac{1}{2.1\text{ns}} = 0.4762\text{ns} \times \frac{1\text{sec}}{10^{-9}\text{ns}} = 476{,}200{,}000$ cycles

$476{,}200{,}000$ cycles $\times \frac{1\text{MHz}}{1 \times 10^{6}\text{ cycles}} = \boxed{476.2\text{ MHz}}$

Problem III: Textbook problem 5.11 (only FSD) (5 pts)

Textbook problem 5.11 (only FSD)

- Design a Mealy sequence recognizer that detects the overlapping sequence "1001". Use binary encoded state labels.



A=00

B=01

C=10

D=11