Name: _____ ID# _____

Date Submitted: _____ Time Submitted _____

CSE 4357/5357 Advanced Digital Logic Design Spring Semester 2021

**Assignment #3 – Carry-Lookahead Adder/Subtractor**

Due Date – February 20, 2021 (11:59 PM)

Submit on Canvas Assignments

**CSE 4357/5357** **ASSIGNMENT #3** **SPRING 2021**

# CARRY-LOOKAHEAD ADDER/SUBTRACTOR

# (100 POINTS)

## PURPOSE/OUTCOMES

To design in Verilog and simulate an 4-bit carry-lookahead adder/subtractor. You will also investigate how Quartus Prime 18.1 compiles your design for realization on a DE1-SoC development board. Once you complete this assignment, you will have demonstrated an ability to design and model combinational logic circuits in Verilog and gained an understanding of how Verilog compilers translate Verilog code to a realization on a Field Programmable Gate Array.

## BACKGROUND

Ripple-carry adders (RCA) as shown in Figure 1 are simple but slow due to the necessity for carries to propagate the full length of the chain in the worst case scenario. A carry-lookahead adder (CLA) overcomes the propagation problem by generating all carries at once with two-level logic but at the expensive of a much more complex design. Figure 2 shows the basic element of a CLA. The *p* and *g* outputs drive carry-generate logic that simultaneously produces the carries for all stages of the CLA as shown in Figure 3. Group carry-lookahead extends the concept to another level as shown in Figure 4.

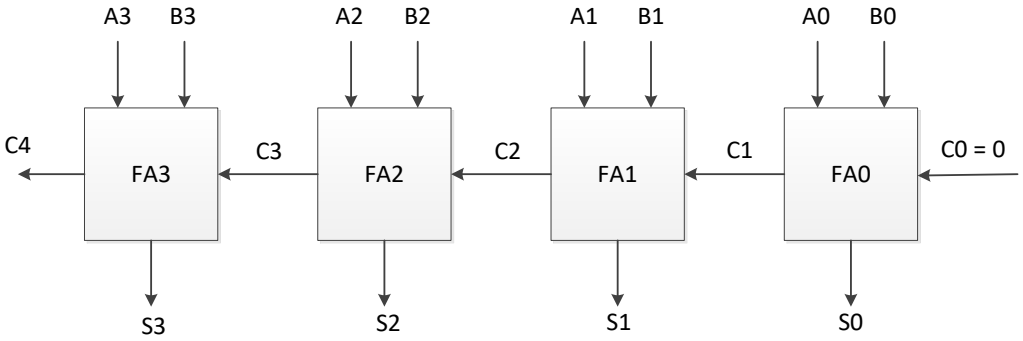
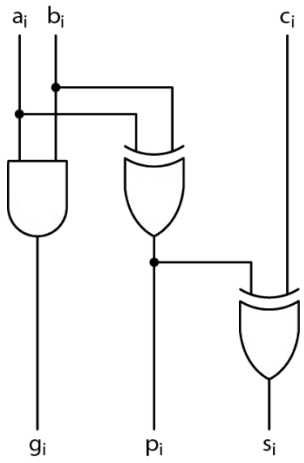



**Figure 1. Four-Bit Ripple-Carry Adder (A + B)**




where

$s = (a \oplus b) \oplus c_{in}$

$p = a \oplus b$ and $g = ab$

**Figure 2. Carry-Lookahead Adder (CLA) *p* and *g* Generator**

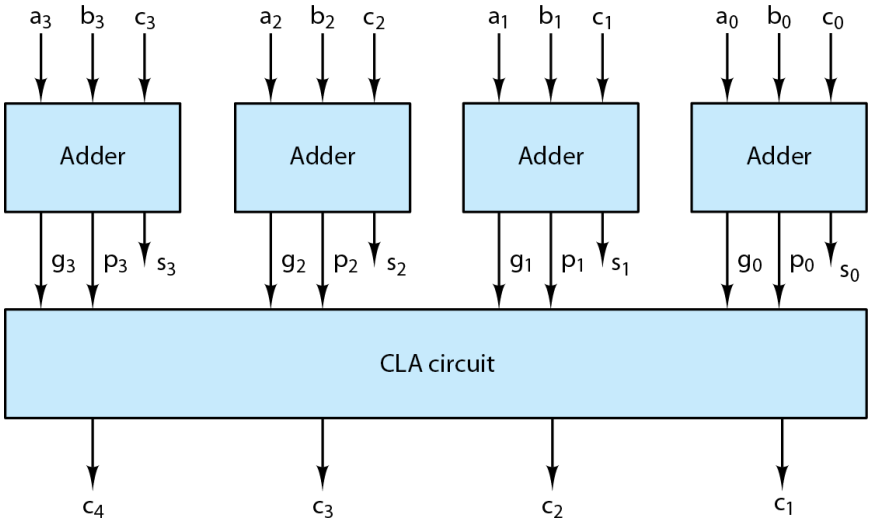
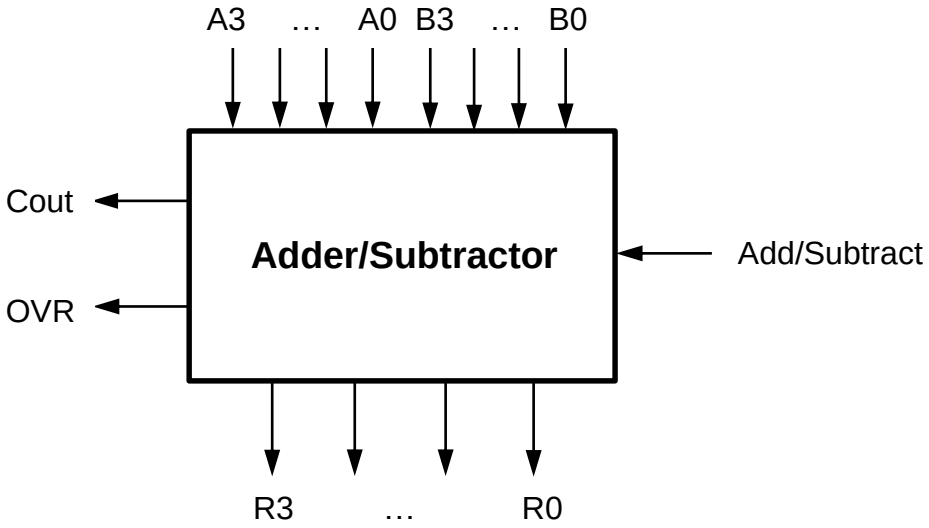



**Figure 3. Four-Bit Carry Lookahead Adder**

## DESIGN REQUIREMENTS

Your assignment is to design and simulate an eight-bit group carry-lookahead adder/subtractor with carry out and overflow outputs as shown in Figure 5. Assume A, B, and R are eight-bit signed binary numbers and Cout and OVR are carry out and overflow functions. Assume a two's complement number system is used for signed number representation.




If Add/Subtract = 0, then R = A + B; else R = A – B.

**Figure 5. Eight-Bit Carry-Lookahead Adder/Subtractor**

## DESIGN PROCESS (60 points)

1. Design your Adder/Subtractor using hierarchical design. Draw a hierarchy diagram.
2. Write Verilog modules of your lowest level components.
3. Instantiate your components bottom up to realize your adder/subtractor.

**DESIGN VERIFICATION (30 points)**

1. Simulate your design to verify its correctness. Use the following values of A and B in your simulation.

   (a) 0101 +/- 1010 *
   (b) 0111 +/- 0001 *
   (c) 0111 +/- 1111
   (d) 0110 +/- 1101
   (e) 1010 +/- 0011 *
   (f) 1001 +/- 1110
   (g) 1010 +/- 1110
   (h) 1101 +/- 1100 *

2. Record the simulation results in a table for your report.

**RTL ANALYSIS (10 POINTS)**

1. Generate RTL diagrams using the Quartus Prime Netlist Viewer for each module in your design.
2. How many ALMs, registers, and total pins are used?

**LAB REPORT REQUIREMENTS**

1. Cover sheet
2. Design requirements
3. CLA organization diagram
4. CLA hierarchy diagram
5. Verilog code for each module
6. Simulation waveform
7. Test results table
8. Photos of marked test results
9. RTL diagrams
10. Compilation Report (Flow Summary)