Name: _____ ID# _____

Date Submitted: _____ Time Submitted _____

CSE 4357/5357 Advanced Digital Logic Design Spring Semester 2021

Assignment #2 – Knight Rider Flasher

Due Date – February 6, 2021 (11:59 PM)

Submit on Canvas Assignments

CSE 4357/5357 **ASSIGNMENT #2** **SPRING 2021**

KNIGHT RIDER FLASHER

(100 POINTS)

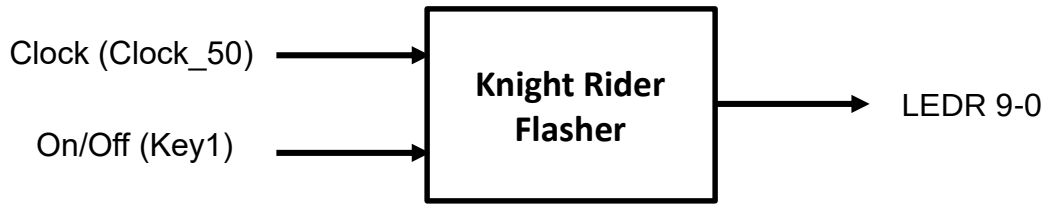
PURPOSE/OUTCOMES

To design in Verilog, implement on the DE1-SoC, and demonstrate a sequential machine that flashes the red LEDs on the DE1-SoC in a continuous back and forth pattern reminiscent of the action lights on the Knight Rider's Firebird Trans Am, KITT. Once you complete this assignment, you will have demonstrated an ability to design and model sequential logic circuits in Verilog that meet specified requirements and to implement the design using a Field Programmable Gate Array (FPGA) employing the following features.

- ✓ Clock_50 50-MHz clock
- ✓ On/Off toggle
- ✓ Clock divider
- ✓ Up/Down counter
- ✓ Module instantiation
- ✓ Pin assignment

BACKGROUND

The input/output diagram of the Flasher is shown below.



The DE1-SoC board provides a 50-MHz clock (CLOCK_50) that can be used as the timebase for the Flasher. You will need to design a clock divider to provide an appropriate frequency for the machine. The LEDs should flash in a continuous back and forth pattern, reversing direction about once per second, twice per second, and once every two seconds. An up/down counter can be used to realize the LED output pattern. Employ the on/off toggle discussed in class for your On/Off switch. It is recommended that you realize the clock divider and on/off toggle as two separate modules and instantiate them in your top-level module.

DESIGN REQUIREMENTS

Design, implement, and demonstrate the sequential machine described above.

- Top module – 25 points
- On/off toggle module – 25-points
- Clock divider module – 25 points
- Demonstrations – 25 points

REPORT REQUIREMENTS

1. Cover sheet
2. Design requirements
3. Verilog code
4. Pin Assignments
5. Demonstration videos