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1 // GPIO Library
2 // Jason Losh
3
4 //-----
5 // Hardware Target
6 //-----
7
8 // Target Platform: EK-TM4C123GXL with LCD/Keyboard Interface
9 // Target uC:      TM4C123GH6PM
10 // System Clock:   40 MHz
11
12 // Hardware configuration:
13 // GPIO APB ports A-F
14
15 //-----
16 // Device includes, defines, and assembler directives
17 //-----
18
19 #include <stdint.h>
20 #include <stdbool.h>
21 #include "tm4c123gh6pm.h"
22 #include "gpio.h"
23
24 // Bit offset of the registers relative to bit 0 of DATA_R at 3FCh
25 #define OFS_DATA_TO_DIR      1*4*8
26 #define OFS_DATA_TO_IS      2*4*8
27 #define OFS_DATA_TO_IBE     3*4*8
28 #define OFS_DATA_TO_IEV     4*4*8
29 #define OFS_DATA_TO_IM      5*4*8
30 #define OFS_DATA_TO_AFSEL   9*4*8
31 #define OFS_DATA_TO_ODR    68*4*8
32 #define OFS_DATA_TO_PUR    69*4*8
33 #define OFS_DATA_TO_PDR    70*4*8
34 #define OFS_DATA_TO_DEN    72*4*8
35 #define OFS_DATA_TO_CR     74*4*8
36 #define OFS_DATA_TO_AMSEL  75*4*8
37
38 //-----
39 // Global variables
40 //-----
41
42 //-----
43 // Subroutines
44 //-----
45
46 void enablePort(PORT port)
47 {
48     switch(port)
49     {
50         case PORTA:
51             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R0;
52             SYSCTL_GPIOHCTL_R  &= ~1;
53             break;
54         case PORTB:
55             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R1;
56             SYSCTL_GPIOHCTL_R  &= ~2;
57             break;
58         case PORTC:
59             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R2;
60             SYSCTL_GPIOHCTL_R  &= ~4;
61             break;
62         case PORTD:
63             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R3;
64             SYSCTL_GPIOHCTL_R  &= ~8;
65             break;
66         case PORTE:
67             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R4;
68             SYSCTL_GPIOHCTL_R  &= ~16;
69             break;

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70         case PORTF:
71             SYSCTL_RCGCGPIO_R |= SYSCTL_RCGCGPIO_R5;
72             SYSCTL_GPIOHCTL_R &= ~32;
73         }
74     _delay_cycles(3);
75 }
76
77 void disablePort(PORT port)
78 {
79     switch(port)
80     {
81         case PORTA:
82             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R0;
83             break;
84         case PORTB:
85             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R1;
86             break;
87         case PORTC:
88             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R2;
89             break;
90         case PORTD:
91             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R3;
92             break;
93         case PORTE:
94             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R4;
95             break;
96         case PORTF:
97             SYSCTL_RCGCGPIO_R &= ~SYSCTL_RCGCGPIO_R5;
98     }
99     _delay_cycles(3);
100 }
101
102 void selectPinPushPullOutput(PORT port, uint8_t pin)
103 {
104     uint32_t* p;
105     p = (uint32_t*)port + pin + OFS_DATA_TO_ODR;
106     *p = 0;
107     p = (uint32_t*)port + pin + OFS_DATA_TO_DIR;
108     *p = 1;
109     p = (uint32_t*)port + pin + OFS_DATA_TO_DEN;
110     *p = 1;
111 }
112
113 void selectPinOpenDrainOutput(PORT port, uint8_t pin)
114 {
115     uint32_t* p;
116     p = (uint32_t*)port + pin + OFS_DATA_TO_ODR;
117     *p = 1;
118     p = (uint32_t*)port + pin + OFS_DATA_TO_DIR;
119     *p = 1;
120     p = (uint32_t*)port + pin + OFS_DATA_TO_DEN;
121     *p = 1;
122 }
123
124 void selectPinDigitalInput(PORT port, uint8_t pin)
125 {
126     uint32_t* p;
127     p = (uint32_t*)port + pin + OFS_DATA_TO_DIR;
128     *p = 0;
129     p = (uint32_t*)port + pin + OFS_DATA_TO_DEN;
130     *p = 1;
131     p = (uint32_t*)port + pin + OFS_DATA_TO_AMSEL;
132     *p = 0;
133 }
134
135 void selectPinAnalogInput(PORT port, uint8_t pin)
136 {
137     uint32_t* p;
138     p = (uint32_t*)port + pin + OFS_DATA_TO_DEN;

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139     *p = 0;
140     p = (uint32_t*)port + pin + OFS_DATA_TO_AMSEL;
141     *p = 1;
142     p = (uint32_t*)port + pin + OFS_DATA_TO_AFSEL;
143     *p = 1;
144 }
145
146 void setPinCommitControl(PORT port, uint8_t pin)
147 {
148     switch(port)
149     {
150         case PORTA:
151             GPIO_PORTA_LOCK_R = GPIO_LOCK_KEY;
152             break;
153         case PORTB:
154             GPIO_PORTB_LOCK_R = GPIO_LOCK_KEY;
155             break;
156         case PORTC:
157             GPIO_PORTC_LOCK_R = GPIO_LOCK_KEY;
158             break;
159         case PORTD:
160             GPIO_PORTD_LOCK_R = GPIO_LOCK_KEY;
161             break;
162         case PORTE:
163             GPIO_PORTE_LOCK_R = GPIO_LOCK_KEY;
164             break;
165         case PORTF:
166             GPIO_PORTF_LOCK_R = GPIO_LOCK_KEY;
167     }
168     uint32_t* p;
169     p = (uint32_t*)port + pin + OFS_DATA_TO_CR;
170     *p = 1;
171 }
172
173 void enablePinPullup(PORT port, uint8_t pin)
174 {
175     uint32_t* p;
176     p = (uint32_t*)port + pin + OFS_DATA_TO_PUR;
177     *p = 1;
178 }
179
180 void disablePinPullup(PORT port, uint8_t pin)
181 {
182     uint32_t* p;
183     p = (uint32_t*)port + pin + OFS_DATA_TO_PUR;
184     *p = 0;
185 }
186
187 void enablePinPulldown(PORT port, uint8_t pin)
188 {
189     uint32_t* p;
190     p = (uint32_t*)port + pin + OFS_DATA_TO_PDR;
191     *p = 1;
192 }
193
194 void disablePinPulldown(PORT port, uint8_t pin)
195 {
196     uint32_t* p;
197     p = (uint32_t*)port + pin + OFS_DATA_TO_PDR;
198     *p = 0;
199 }
200
201 void setPinAuxFunction(PORT port, uint8_t pin, uint32_t fn)
202 {
203     // call with header file shifted values or 4-bit number
204     if (fn <= 15)
205         fn = fn << (pin*4);
206     else
207         fn = fn & (0x0000000F << (pin*4));

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208     switch(port)
209     {
210         case PORTA:
211             GPIO_PORTA_PCTL_R = (GPIO_PORTA_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
212             break;
213         case PORTB:
214             GPIO_PORTB_PCTL_R = (GPIO_PORTB_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
215             break;
216         case PORTC:
217             GPIO_PORTC_PCTL_R = (GPIO_PORTC_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
218             break;
219         case PORTD:
220             GPIO_PORTD_PCTL_R = (GPIO_PORTD_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
221             break;
222         case PORTE:
223             GPIO_PORTE_PCTL_R = (GPIO_PORTE_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
224             break;
225         case PORTF:
226             GPIO_PORTF_PCTL_R = (GPIO_PORTF_PCTL_R & ~(0x0000000F << (pin*4))) | fn;
227     }
228     // set AFSEL bit only if using aux function, otherwise clear bit
229     uint32_t* p;
230     p = (uint32_t*)port + pin + OFS_DATA_TO_AFSEL;
231     *p = (fn > 0);
232 }
233
234 void selectPinInterruptRisingEdge(PORT port, uint8_t pin)
235 {
236     uint32_t* p;
237     p = (uint32_t*)port + pin + OFS_DATA_TO_IS;
238     *p = 0;
239     p = (uint32_t*)port + pin + OFS_DATA_TO_IBE;
240     *p = 0;
241     p = (uint32_t*)port + pin + OFS_DATA_TO_IEV;
242     *p = 1;
243 }
244
245 void selectPinInterruptFallingEdge(PORT port, uint8_t pin)
246 {
247     uint32_t* p;
248     p = (uint32_t*)port + pin + OFS_DATA_TO_IS;
249     *p = 0;
250     p = (uint32_t*)port + pin + OFS_DATA_TO_IBE;
251     *p = 0;
252     p = (uint32_t*)port + pin + OFS_DATA_TO_IEV;
253     *p = 0;
254 }
255
256 void selectPinInterruptBothEdges(PORT port, uint8_t pin)
257 {
258     uint32_t* p;
259     p = (uint32_t*)port + pin + OFS_DATA_TO_IS;
260     *p = 0;
261     p = (uint32_t*)port + pin + OFS_DATA_TO_IBE;
262     *p = 1;
263 }
264
265 void selectPinInterruptHighLevel(PORT port, uint8_t pin)
266 {
267     uint32_t* p;
268     p = (uint32_t*)port + pin + OFS_DATA_TO_IS;
269     *p = 1;
270     p = (uint32_t*)port + pin + OFS_DATA_TO_IEV;
271     *p = 1;
272 }
273
274 void selectPinInterruptLowLevel(PORT port, uint8_t pin)
275 {
276     uint32_t* p;

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277     p = (uint32_t*)port + pin + OFS_DATA_TO_IS;
278     *p = 1;
279     p = (uint32_t*)port + pin + OFS_DATA_TO_IEV;
280     *p = 0;
281 }
282
283 void enablePinInterrupt(PORT port, uint8_t pin)
284 {
285     uint32_t* p;
286     p = (uint32_t*)port + pin + OFS_DATA_TO_IM;
287     *p = 1;
288 }
289
290 void disablePinInterrupt(PORT port, uint8_t pin)
291 {
292     uint32_t* p;
293     p = (uint32_t*)port + pin + OFS_DATA_TO_IM;
294     *p = 0;
295 }
296
297 void setPinValue(PORT port, uint8_t pin, bool value)
298 {
299     uint32_t* p;
300     p = (uint32_t*)port + pin;
301     *p = value;
302 }
303
304 bool getPinValue(PORT port, uint8_t pin)
305 {
306     uint32_t* p;
307     p = (uint32_t*)port + pin;
308     return *p;
309 }
310
311 void setPortValue(PORT port, uint8_t value)
312 {
313     switch(port)
314     {
315         case PORTA:
316             GPIO_PORTA_DATA_R = value;
317             break;
318         case PORTB:
319             GPIO_PORTB_DATA_R = value;
320             break;
321         case PORTC:
322             GPIO_PORTC_DATA_R = value;
323             break;
324         case PORTD:
325             GPIO_PORTD_DATA_R = value;
326             break;
327         case PORTE:
328             GPIO_PORTE_DATA_R = value;
329             break;
330         case PORTF:
331             GPIO_PORTF_DATA_R = value;
332     }
333 }
334
335 uint8_t getPortValue(PORT port)
336 {
337     uint8_t value;
338     switch(port)
339     {
340         case PORTA:
341             value = GPIO_PORTA_DATA_R;
342             break;
343         case PORTB:
344             value = GPIO_PORTB_DATA_R;
345             break;

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```
346         case PORTC:
347             value = GPIO_PORTC_DATA_R;
348             break;
349         case PORTD:
350             value = GPIO_PORTD_DATA_R;
351             break;
352         case PORTE:
353             value = GPIO_PORTE_DATA_R;
354             break;
355         case PORTF:
356             value = GPIO_PORTF_DATA_R;
357     }
358     return value;
359 }
360
```