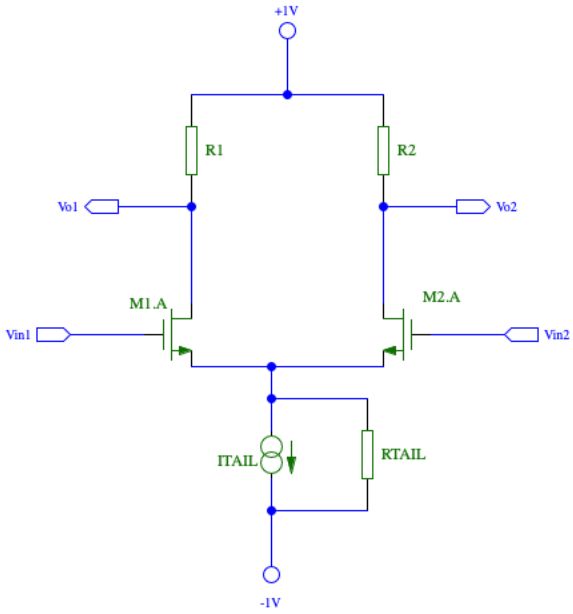
March 17, 2022

Homework 2

This assignment is about designing and analyzing a MOS differential amplifier. We will use the TSMC 0,18 μm technology as given in your moodle course page for the MOSFETs.

1) For the circuit diagram given below, we would like a differential gain of *7,5*. We would like that the overdrive voltages (V_{ov}) are *0,2 V* for the transistors. Using $g_m = 2I_D/V_{ov}$, and $V_{D1} = V_{D2} = V_{DD} - I_D R_D$, calculate the necessary V_D for these specs.
2) Using the μ_n, t_{ox}, and V_t values given in the transistor model, calculate k_n' and the necessary *W* and *L* values to provide the desired V_{ov}. Also, calculate the necessary R_D values. Choose a tail current of *120 μA* and a tail resistance of *1 MΩ*. Please use minimum *L* values. Ignore the tail resistance for DC calculations. Note that μ_n is approximated by U0 and V_t by VTO in the model. TOX represents t_{ox}.
3) Replace the resistors R_1 and R_2 by PMOS transistors, thus creating an active load. Choose $V_{ov} = 0,2$ *V* as well for these transistors. Thus, you can determine their bias voltage. Keeping the *L* values minimum for these devices, adjust their *W* values on the simulator so that the DC levels are approximately the same as the previous questions. You may start with a *W/L* ratio *2-3* times that of the NMOS transistors (Why?). What is the simulated differential gain? Assuming the "Early voltages (V_A)" to be about the same for all transistors, what are they equal to?
4) Keeping the *W/L* ratios the same, increase *L* by three times for all transistors. If the DC levels have shifted, you may do small adjustments to bring them back. Estimate and simulate the new gain?
5) Finally, using the V_A values you have approximately determined, find the necessary *W* and *L* values and the bias voltage for the tail current source for a *1 MΩ* tail resistance, keeping the overdrive voltage at *0,2 V*. The *W/L* ratio should be about twice the NMOS transistors (Why?). If the DC levels have shifted, correct them by making small changes.
6) To your circuit, apply the sum of a *0,5 V* amplitude *50 Hz* frequency interfering common mode signal and a *1 mV* amplitude *1 kHz* frequency differential input signal. Plot the inputs and the single ended and differential outputs from the simulator.



Hints:

0,18 μm technology means that your transistor lengths (L) are at least 0,18 μm. Your transistor widths (*W*) are also a minimum of 0,18 μm and typically (but not necessarily) larger than the *L* values.

You may perform your simulations on LTSPICE. For MOS model information, you may look up http://ltwiki.org/LTspiceHelp/LTspiceHelp/M_MOSFET.htm

You may connect the bulk terminals to the source terminals in your simulations.