EE-336

EXPERIMENT 7

Single-BJT Amplifiers at Low and High Frequencies

Name: Aras

Surname: Güngöre

Student ID: 2018401117

Section: Online

OBJECTIVE:
Exploring the behavior of capacitor-coupled BJT amplifiers at low-frequencies, and examining the high-frequency behavior of the BJT itself in a simple circuit.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
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PROCEDURE

1. The Basic Common-Emitter (CE) Circuit

E1.1 The DC Situation:

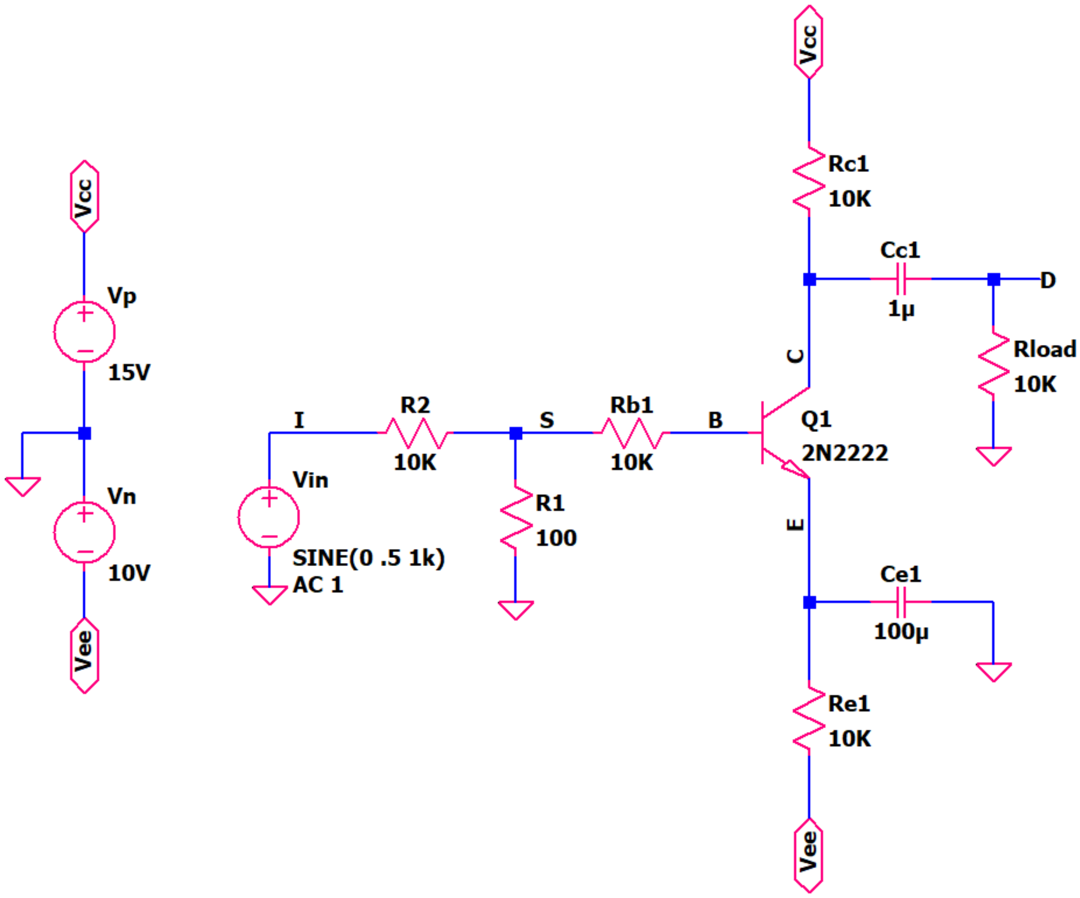


Figure 1. A Basic CE BJT Amplifier.

V_S	V_B	V_E	V_C	I_E	I_C
-434.6 µV	-44.33 mV	-696.3 mV	5.740 V	930.4 µA	926.0 µA
I_B	**β**	**α**	**r_e**	**r_π**	**g_m**
4.390 µA	211.0	0.9953	27.95 Ω	5.923 kΩ	35.61 mS

Table 1. DC values for CE BJT amplifier circuit.

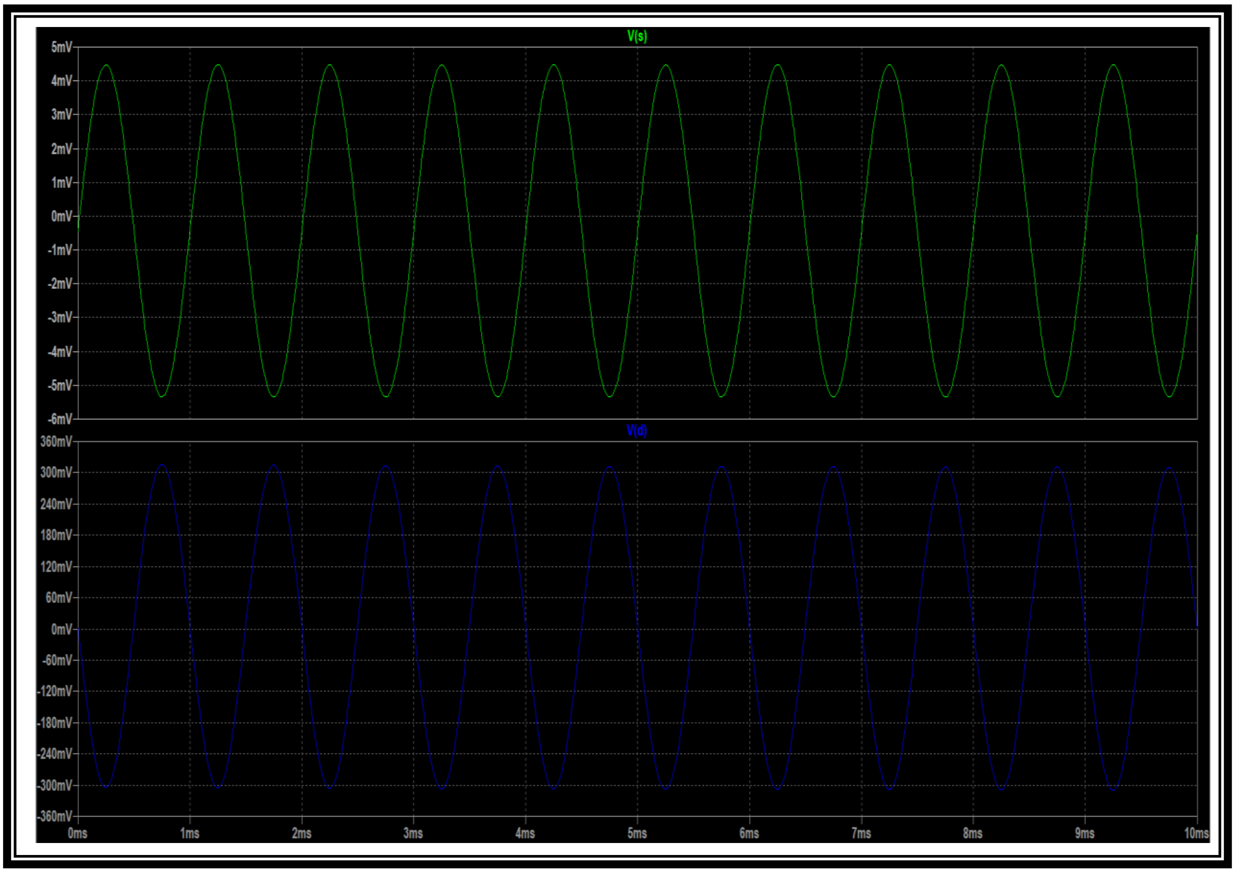
Assemble the circuit shown in Figure 1 in LTSpice using 2N2222 BJT model, available in LTSpice libraries. With input (node I) grounded, measure the DC voltages at nodes S, B, E and C. Use these values to calculate bias currents, β, α, r_e, r_π and g_m. We will assume V_A to be very large, as it normally is, and ignore r_o as a consequence.

E1.2 Mid-Band Response:

For the circuit in Figure 1, apply a sine-wave signal of 1 Vpp at 1 kHz to node I. Run a transient simulation and measure peak-to-peak voltages at nodes S, B, E, C, D. Put the waveforms of nodes S, D to the box below.

v_s	v_b	v_e	v_c	v_d
9.829 mV	3.703 mV	248.5 µV	621.6 mV	624.6 mV

Table 2. Peak-to-peak values for CE BJT amplifier circuit.



Waveforms of nodes S and D.

2. Low Frequency Response

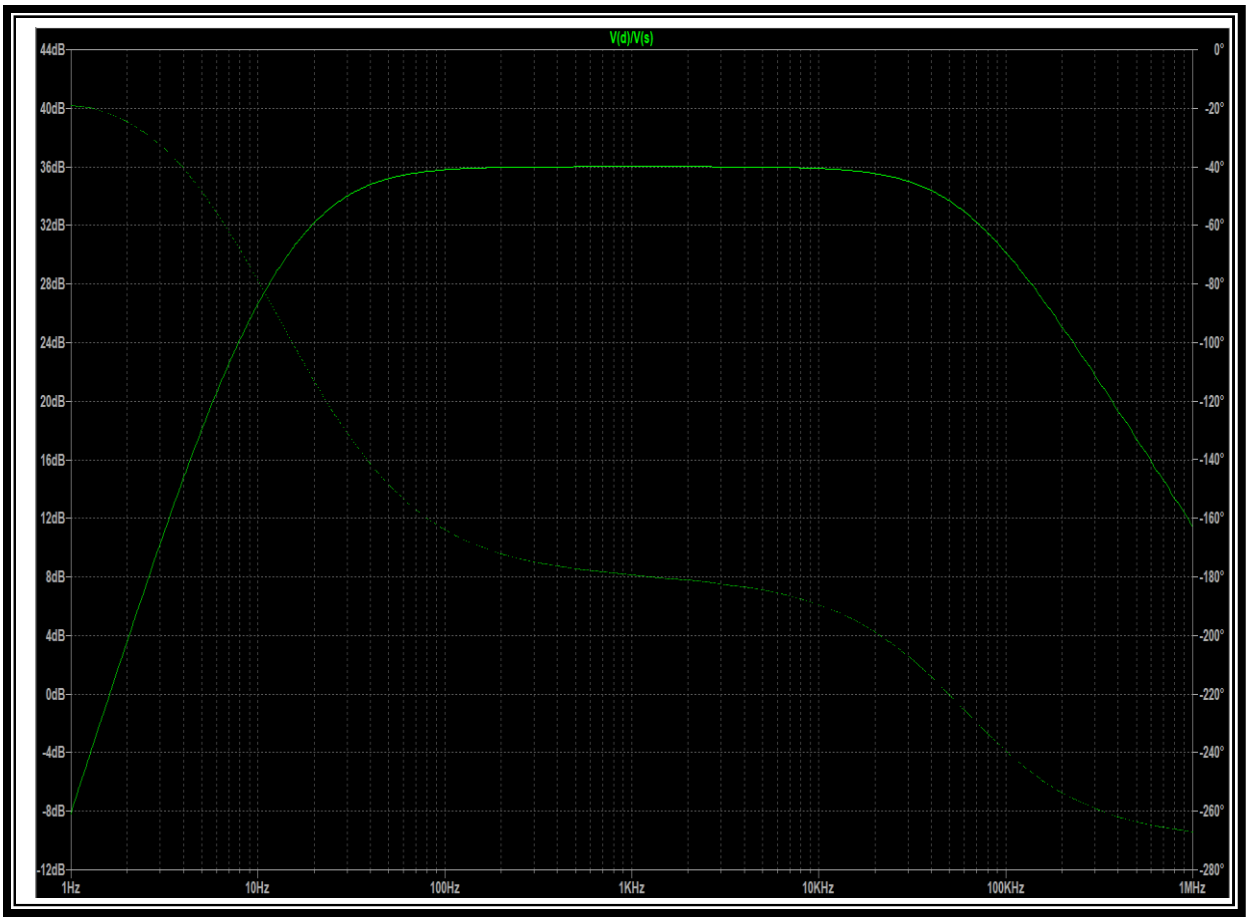
E2.1 Basic Overall Response:

Use the same circuit as E.1.2 (Figure 1), with a sine-wave signal of 1 Vpp at 1 kHz at node I. Probing nodes S and D, lower the frequency to the values in Table 3 and note the corresponding peak-to-peak voltages. After completing the transient simulations, run an .AC simulation to find the lower 3 dB frequency, f_L, at which the voltage gain at 1 kHz falls by 3dB. Put AC plot of the gain to the box below.

	υ_s	υ_d	υ_d / υ_s
1 kHz	9.809 mV	625.9 mV	-63.81
500 Hz	9.809 mV	632.0 mV	-64.43
200 Hz	9.810 mV	641.3 mV	-65.37
100 Hz	9.817 mV	633.9 mV	-64.56
50 Hz	9.830 mV	576.4 mV	-58.64
20 Hz	9.846 mV	404.7 mV	-41.10
10 Hz	9.875 mV	213.4 mV	-21.61
5 Hz	9.893 mV	79.75 mV	-8.061

f_L	23.56 Hz

Table 3. Peak-to-peak voltages for corresponding frequencies.



AC plot of the gain.

3. High Frequency Operation of the Common-Emitter (CE) Amplifier

E3.1 Basic AC Measurements:

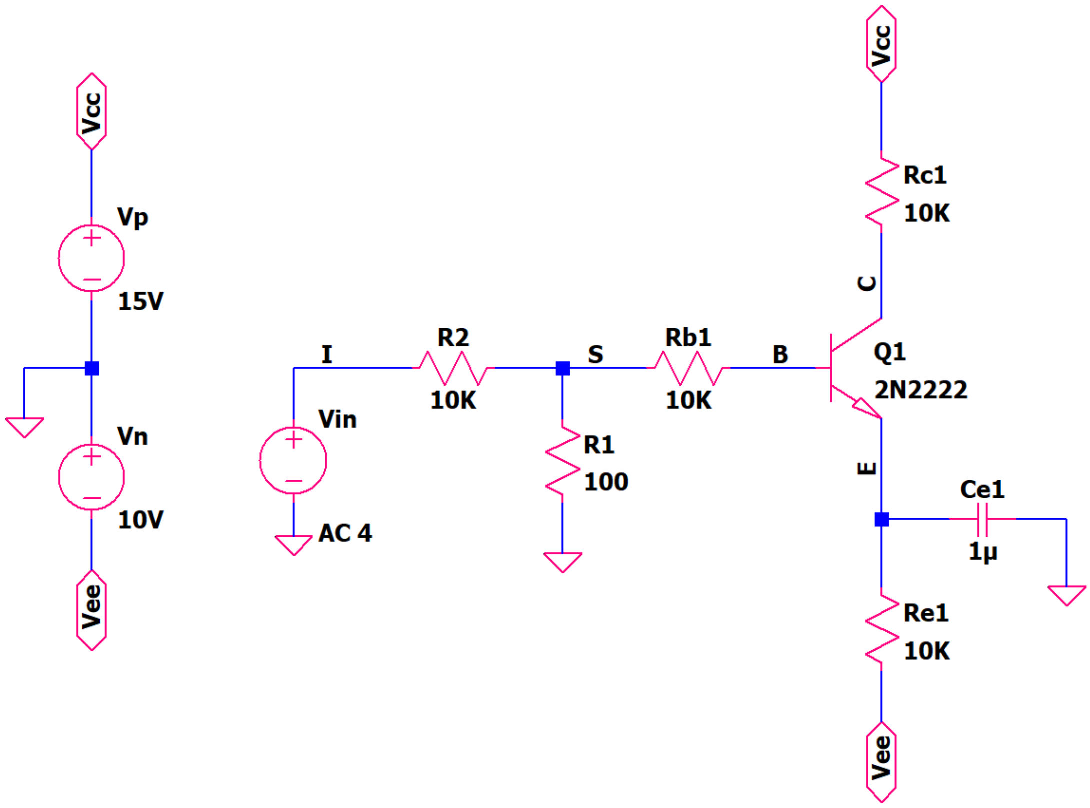


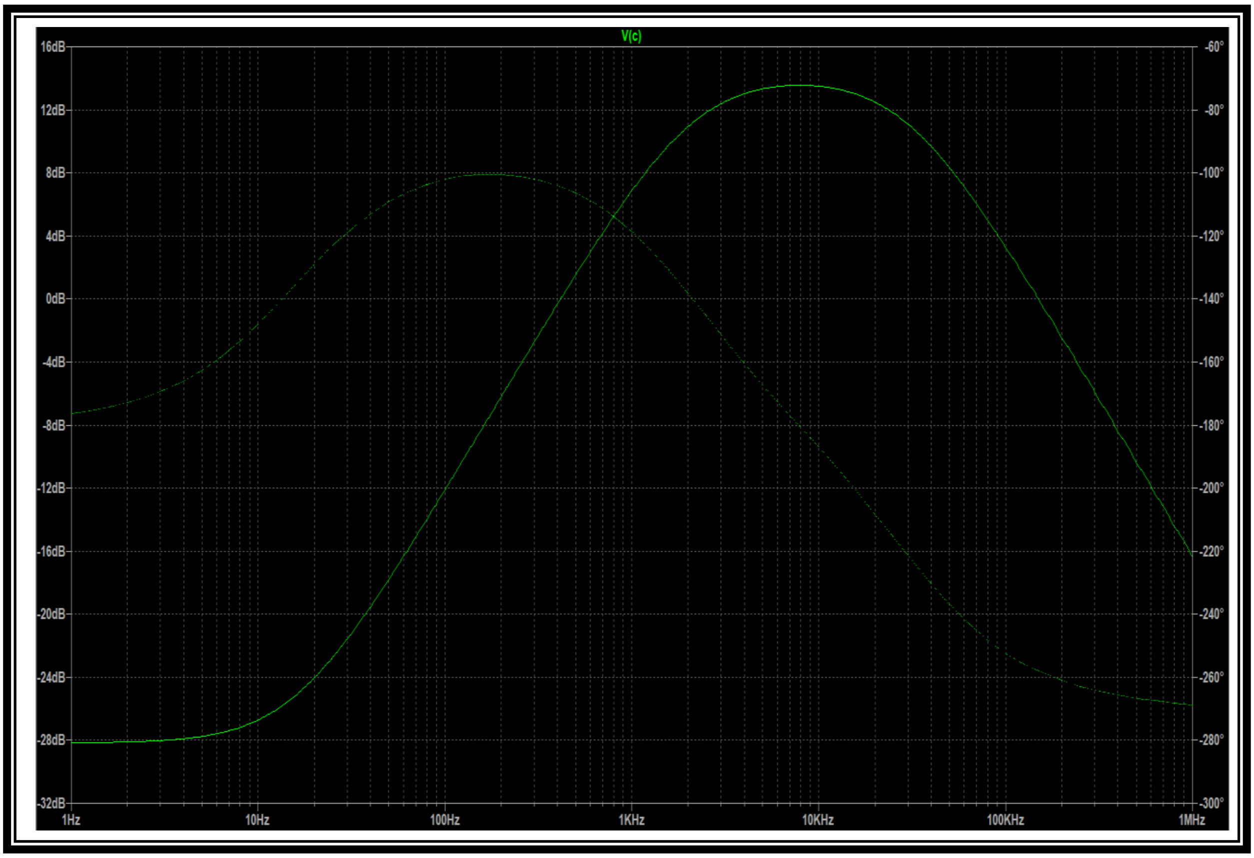
Figure 2. Modifications for high-frequency operation.

Assemble the circuit in Figure 2 in LTSpice using 2N2222 BJT model, with a 4 Vpp sine wave input at 10 kHz and run .AC simulation for the following questions.

a) Measure the peak-to-peak voltages at nodes S, B and C. Put AC plot of node C to the box below.
b) Now, noting the signal at node C in particular, raise the frequency, until the voltage at C falls by 3 dB, to 0.707 of its mid-band value. Note the frequency as f_1.
c) Raise the frequency to $10f_1$, and measure the peak-to-peak voltages at nodes S, B and C.
d) Now, connect another 10 kΩ resistor in parallel with R_C, and proceed to find the modified 3 dB frequency, f_2.

R_C	Input	f	υ_s	υ_b	υ_c
10 kΩ	10 kHz	10 kHz	39.23 mV	17.55 mV	4.829 V
	f_1	34.20 kHz	39.15 mV	10.81 mV	3.285 V
	$10f_1$	342.0 kHz	39.10 mV	1.791 mV	577.3 mV
5 kΩ	10 kHz	10 kHz	39.25 mV	18.44 mV	2.607 V
	f_2	69.46 kHz	39.16 mV	10.73 mV	1.773 V
	$10f_2$	694.6 kHz	39.10 mV	1.841 mV	315.7 mV

Table 4. Peak-to-peak values and gains for two cases.



AC plot for the first case, R_c = 10kΩ.

REFERENCES

- Smith, K. C. and Sedra, A. S., *Laboratory Explorations for Microelectronic Circuits*, Oxford University Press, 1998.

ANALYSIS AND DISCUSSION

At E1.1, we measure the node voltages and bias currents with DC analysis, then we use these values to calculate the transistor parameters using the following formulas: $\alpha = I_C / I_E$, $\beta = I_C / I_B$, $g_m = I_C / V_T$, $r_e = \alpha / g_m$, $r_\pi = \beta / g_m$, where $V_T = 26$ mV. At E1.2, we measure the peak-to-peak voltages of S, B, E, C, D at the mid-band frequency response which is 1 kHz. From the plots, we observe there is a 180° phase difference between V_S and V_D due to the Cc1 capacitor.

At E2.1, starting from the mid-band, we gradually lower the frequency and note the corresponding V_S, V_D, and gain values to find the zero frequency. At the zero frequency, the gain is $1/\sqrt{2} = 0.707$ times of the maximum gain, which I have measured using the following LTspice directives: ".meas ac A_max MAX MAG(V(D) / V(S)); .meas ac A_3db PARAM A_max / sqrt(2); .meas ac f_3db FIND freq WHEN MAG(V(D) / V(S)) = A_3db". From the AC plot, this measurement can be validated since the +3 dB frequency, that is the zero (lower cut-off) frequency is around 20 Hz, and the -3 dB frequency, that is the pole (higher cut-off) frequency is around 60 kHz. The gains listed on the table are negative due to the 180° phase difference between V_S and V_D, as determined in the AC plot at E1.2. From the average of the first three values on the table, we estimate the mid-band decibel gain to be $20 \cdot \log(63.5) \approx 36.06$ dB, which checks from the plot. Given that r_o isn't infinite and the transistors are not ideal, nonidealities in the AC plot can be observed.

At E3.1 in part a, we measure the node voltages of S, B, and C at mid-band on 10 kHz. From the AC plot, we observe that the mid-band is relatively narrow and 10 kHz corresponds to the peak of V_C. At E3.1 in part b, f_1 is the frequency that corresponds to the pole frequency, which can be defined as the higher of the two frequencies where V_C is $1/\sqrt{2} = 0.707$ times of its mid-band value that is measured in part a. At E3.1 in part c, we observe that when f_1 increases by a factor of 10, V_C accordingly becomes approximately 10 times smaller than its value previously measured in part b. At E3.1 in part d, when the collector resistance decreases from $R_{C1} = 10$ kΩ to $R_{C2} = 5$ kΩ, we observe that V_C decreases as well given that less voltage drop occurs. Moreover, when R_C is cut in half, the pole frequency has also been multiplied by 2. To express it mathematically, $R_{C1} = 2 \cdot R_{C2} \Rightarrow f_2 = 2 \cdot f_1$. Therefore, we deduce that there is an inversely proportional relationship between the collector resistance and the pole frequency.