EE-336

EXPERIMENT 6

The BJT Differential Pair and Applications

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Section: Online

OBJECTIVE:
Exploring the BJT differential pair, its properties, and potential applications.

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BOĞAZİÇİ UNIVERSITY-2022

1. The Basic Topology

E1.1 DC Parameters and Conditions:

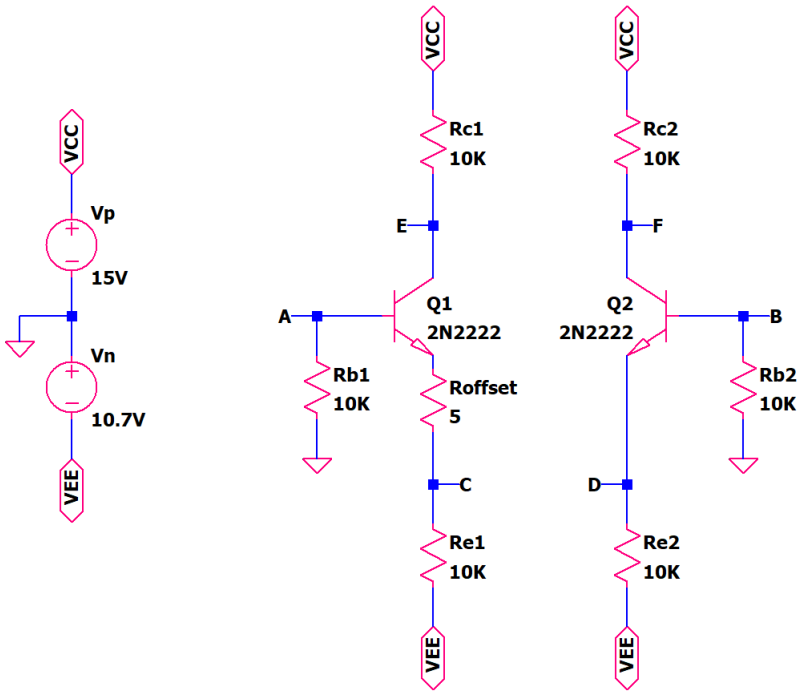


Figure 1. A Pair of Differential Half-Circuits

V_+	V_-	V_A	V_B	V_C	V_D	V_E	V_F	V_{BE1}	V_{BE2}
15 V	-10.7 V	-47.47 mV	-47.49 mV	-706.5 mV	-701.5 mV	5.054 V	5.049 V	659.0 mV	654.0 mV
I_{B1}	I_{C1}	I_{E1}	I_{B2}	I_{C2}	I_{E2}	α_1	α_2	β_1	β_2
4.747 µA	994.6 µA	999.4 µA	4.749 µA	995.1 µA	999.8 µA	0.9953	0.9953	209.5	209.5

Table 1. DC values for differential half-circuit pair. (Part a)

Part	V_A	V_B	V_C (V_D)	V_E	V_F	V_P
b)	-45.92 mV	-49.05 mV	-703.9 mV	5.35 V	4.753 V	N/A
c)	-47.47 mV	-52.46 mV	-706.5 mV	5.054 V	5.054 V	-552.6 mV

Table 2. DC values for two cases.

a) Assemble the two circuits shown in Figure 1, using the 2N2222 BJT model in LTSpice. The 5-Ohm resistor is added to provide an offset, so do not forget to add it to your schematics. Put your simulation and calculation results to Table 1.
b) Join nodes C and D and probe the voltages on nodes A through F. Note your simulation results to the first row of Table 2.

c) With nodes C and D joined, A open, connect a potentiometer to B via a 1MΩ resistor as in Figure 2, measure the voltage between nodes E and F. Instead of using a potentiometer, sweep the DC voltage of node P in your simulations. Adjust V_P until the difference is exactly zero. Probe the voltages on all nodes and note your simulation results to the second row of Table 2.

Hint: Observe how you compensated the DC offset by adjusting the potentiometer.

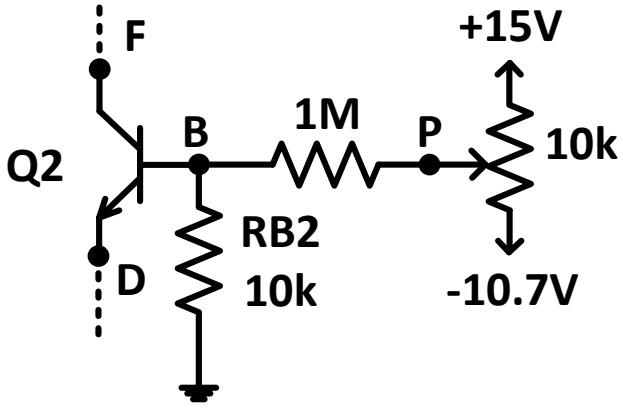


Figure 2. Connection of Series Resistor and Potentiometer to Node B

E1.2 Basic Amplification:

For the basic circuit in Figure 1, connect node A via a 10kΩ - 100Ω voltage divider to a signal source with a sine wave of 1 V_{pp} at 1 kHz. Remove R_{B1} and R_{offset}, ground node B. The resulting circuit will be as in Figure 3.

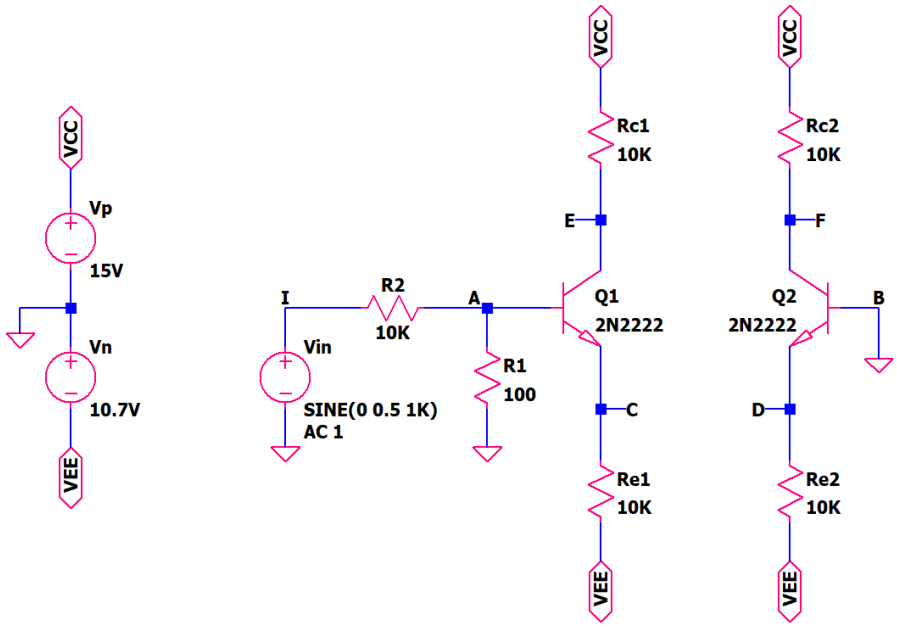


Figure 3. Differential Half-Circuits Driven by a Single-Ended Signal

a) Using transient simulations probe peak-to-peak voltages at nodes A, C, E. What is the voltage gain from A to C? From A to E? Note your results to the Table 3.
b) Now, connect nodes C and D with a 1kΩ resistor, R_e. Probe the peak-to-peak voltages at nodes A through F. What is the voltage gain from A to C, to D, to E, and to F? Note your results to the first row of the Table 4.
c) Now, repeat the process above but with R_e = 0, that is with nodes C and D joined. Measure the peak-to-peak voltages at nodes A, E, F and CD. Find the voltage gains A to E, to CD, and to F. Note your results to the second row of the Table 4 and put the waveforms at nodes A, CD, E and F into the box below.

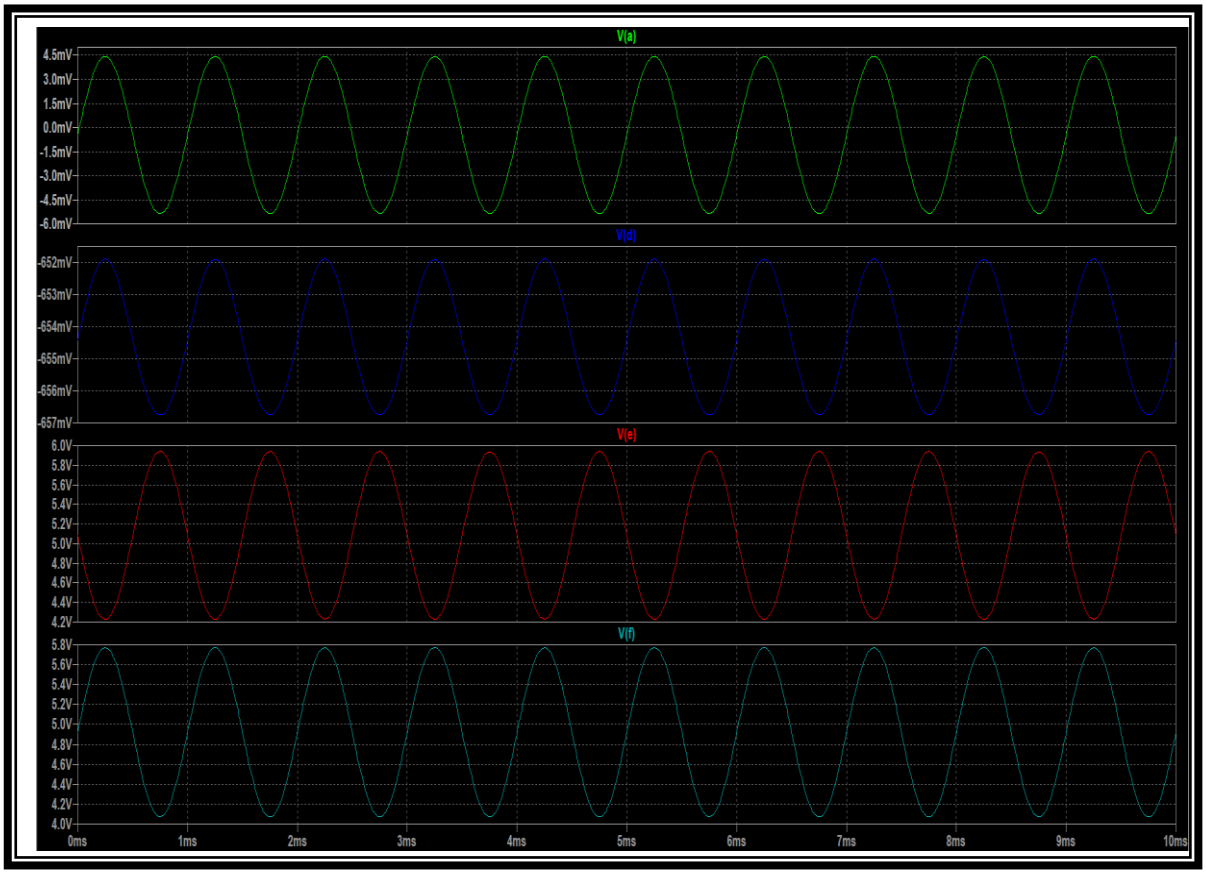
Hint: Observe the relations between voltage gains and configurations you used. How did R_e change voltage gain, why?

v_A	v_C	v_E	v_C/v_A	v_E/v_A
9.891 mV	9.860 mV	9.804 mV	0.9969	-0.9912

Table 3. Peak-to-peak values and gains for differential half-circuit pairs.

Case	v_A	v_C	v_D	v_E	v_F	v_C/v_A	v_D/v_A	v_E/v_A	v_F/v_A
R_e=1k	9.886 mV	9.590 mV	265.2 µV	102.3 mV	92.50 mV	0.9701	0.02682	-10.35	9.357
R_e=0	9.803 mV	4.851 mV	4.851 mV	1.710 V	1.700 V	0.4948	0.4948	-174.4	173.4

Table 4. Peak-to-peak values and gains for two cases.



Waveforms of A, CD, E and F for part c)

E1.3 Input Resistance:

Modify your circuit (slightly) to the form shown in Figure 4, where 10kΩ base resistors has been added (at node A and B). Use a 1 V_{pp} sine wave at 1kHz for input.

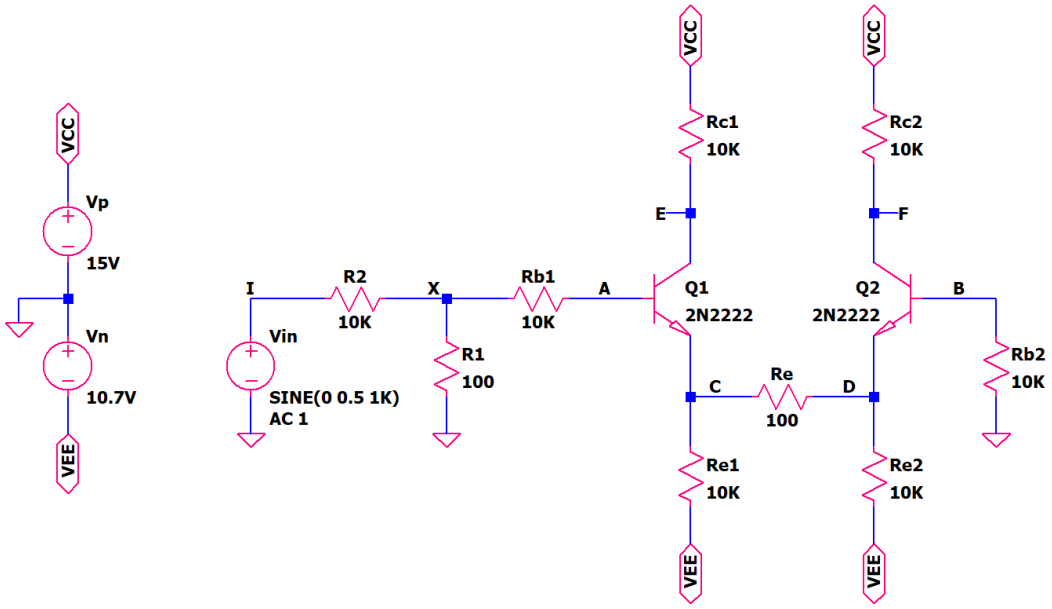


Figure 4. A Differential Amplifier Driven by a Single-Ended Signal

a) With R_e = 0, use transient simulations and probe the peak-to-peak voltages at nodes X, A, B, E, F.

b) Repeat with R_e = 100Ω.

Calculate the input resistance of the amplifier for both cases. Put your simulation and calculation results to the Table 5.

Hint: Comment on how you can estimate the input resistance of this amplifier using these measurements.

	v_x	v_a	v_b	v_e	v_f	R_{in}
R_e=0	9.860 mV	6.651 mV	3.158 mV	611.3 mV	601.6 mV	20.73 kΩ
R_e=100	9.872 mV	7.872 mV	1.947 mV	380.7 mV	371.0 mV	39.37 kΩ

Table 5. Measurement results for two cases.

E1.4 Loading the Amplifier:

Return to the amplifier of Figure 4, with nodes X and A joined (Short circuit the 10k resistor between nodes X and A), node B grounded and R_e = 100Ω. Use a sine wave input of 1 V_{pp} at 1kHz.

a) Load each of nodes E and F with a 10kΩ resistor coupled by a 10μF capacitor as in Figure 5. Probe the peak-to-peak voltages at nodes A, E, F.

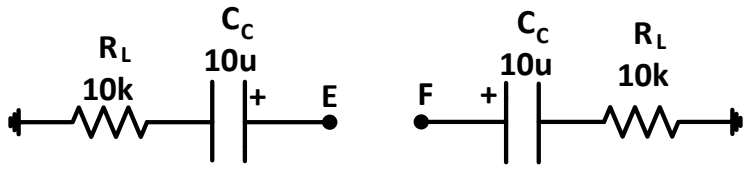


Figure 5. Connection of Load Resistors and Capacitors for Part a)

b) Now, remove the load capacitors and resistors added in Part a) and directly connect (using no capacitor) the two 10kΩ loads in series between nodes E and F. Let the connection between them be called node P as in Figure 6. Measure the peak-to-peak voltages at nodes A, E, F and P.

Figure 6. Connection of Load Resistors for Part b)

Estimate load resistances R_{Le} (Load resistance seeing at node E), R_{Lf} (Load resistance seeing at node F) and R_{Lef} (Load resistance between E and F) separately for both arrangements of loading. Put your simulation results and estimations to Table 6.

	v_a	v_e	v_f	v_p	R_{Le}	R_{Lf}	R_{Lef}
a)	9.860 mV	320.6 mV	315.7 mV	N/A	N/A	N/A	N/A
b)	9.860 mV	323.1 mV	313.3 mV	4.883 mV	N/A	N/A	N/A

Table 6. Measurement and calculation results for two loading arrangements.

Hint: Comment on how virtual ground affects the load impedances.

2. Common-Mode Rejection

E2.1 Single-Ended Load:

Arrange the circuit with a single-ended load as shown in Figure 7. Apply a sinewave signal of 2 V_{pp} at 1 kHz to the common input. Probe the peak-to-peak signals at nodes I, A, and F. Put your measurements to Table 7. Put the waveforms at nodes I, A and F into the box below.

Hint: Observe the difference between differential and common-mode gains. How are these two values related with common-mode rejection ratio?

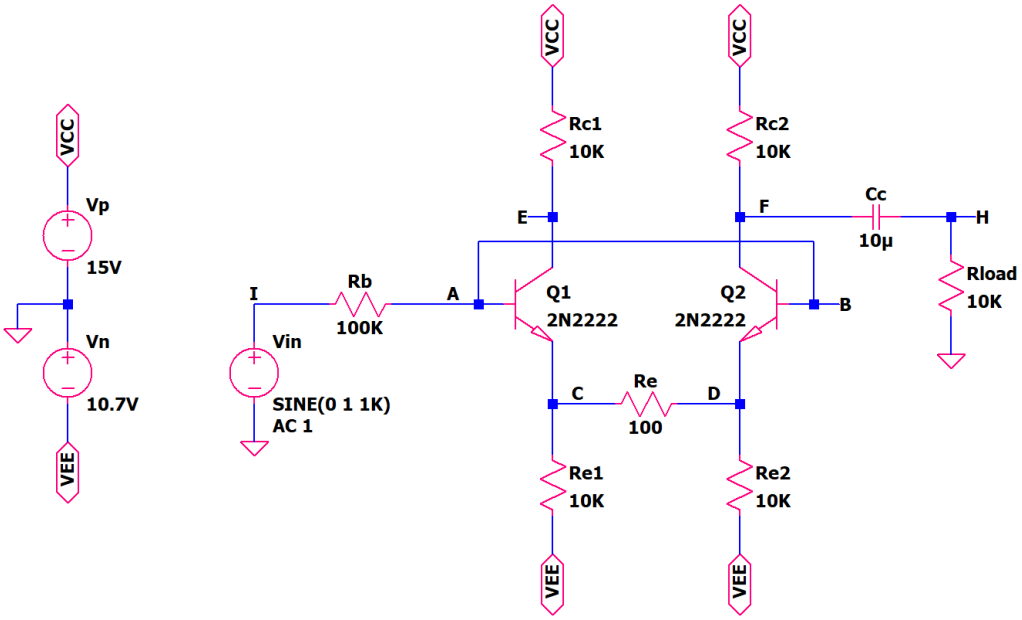
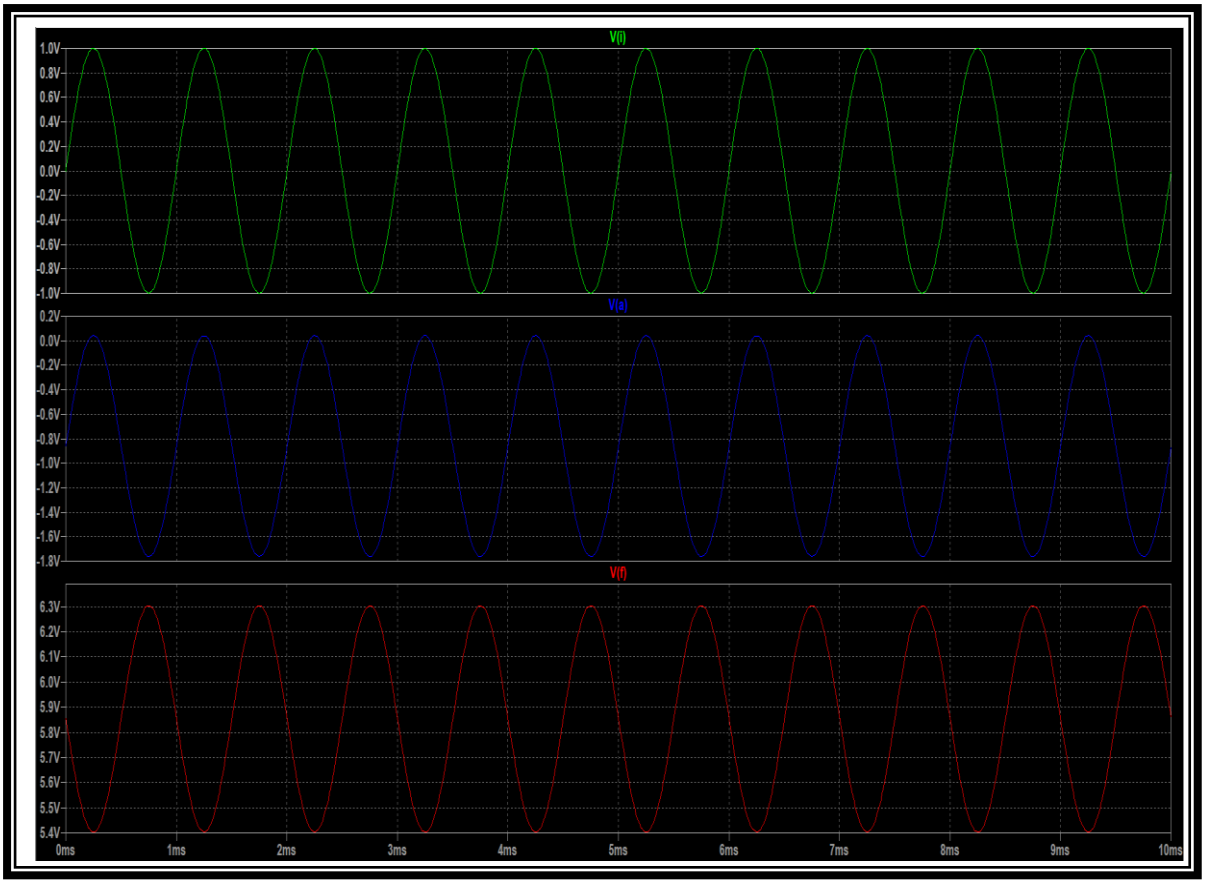


Figure 7. A Differential Amplifier Driven by a Common-Mode Signal

Vi	Va	Vf
2.000 V	1.804 V	901.1 mV

Table 7. Peak-to-peak values at three nodes.



Waveforms of I, A and F

REFERENCES

- Smith, K. C. and Sedra, A. S., *Laboratory Explorations for Microelectronic Circuits*, Oxford University Press, 1998.

ANALYSIS AND DISCUSSION

At E1.1 in part a, we observe that the corresponding base, emitter, and collector voltages and currents of Q1 and Q2 transistors on both sides are measured to be approximately the same; however, a minor difference occurs due to the offset resistance. The alpha and beta values of the transistors are also calculated to be the same, which is expected since the Q1 and Q2 transistors use the same LTspice model. At E1.1 in part b, when C and D nodes are joined, we observe that V_E increases by $\Delta V = 0.296$ V while V_F decreases by the same amount as more current flows through node F due to the offset resistance. At E1.1 in part c, this DC offset is compensated with the addition of an offset voltage via adjusting a potentiometer in which this voltage can be calculated according to voltage division. Hence, we get similar results as in E1.1 part a.

At E1.2 in part a, the node voltages of A and C are in phase whereas the node voltages of A and E are out of phase by 180°, so the V_C/V_A gain is positive while the V_E/V_A gain is negative. The absolute gains are equal to nearly 1, so no amplification occurs. At E1.2 in part b, when C and D nodes are joined with a resistor of $R_e = 1$ kΩ, the V_E/V_A gain increases about 10 times. Hence, the circuit acts as a differential amplifier. Also, the node voltages of C, D, and F are in phase with A whereas the node voltages of A and E are out of phase by 180°, which is why V_E/V_A gain is negative while the other gains are positive. At E1.2 in part c, when $R_e = 0$ the V_C/V_A gain decreases whereas the other V_D/V_A, V_E/V_A, V_F/V_A gains increase by an additional amount of about 15-20 times. From this, we can conclude that joining the C and D nodes can be used to increase the V_D/V_A, V_E/V_A, and V_E/V_F gains and the amplifier gain can be increased even more as the emitter resistance decreases.

At E1.3 in part a, the input resistance R_{in} can be found by connecting node A to the ground with a resistor. According to voltage division, the input resistance is calculated from the formula $R_{in} = V_A / I_A$ where $I_A = (V_X - V_A) / R_{b1}$. At E1.3 in part b, the R_e is increased from $R_e = 0$ to $R_e = 100$ Ω, so the node voltages at A, B, E, and F decrease along with the gain. Since V_A decreases, the R_{in} value increases about 2 times.

At E1.4, since the measurements at parts a and b are approximately equal, one can deduce that both processes are essentially the same. At E1.4 in part b, V_P is measured to be near 0, so we infer that the P node acts as a virtual ground.

At E2.1, the common-mode rejection ratio (CMRR) is found by the formula CMRR = A_{dm} / A_{cm}. From our measurements, the common-mode gain can be calculated as A_{cm} = V_F / V_A = -901.1 mV / 1.804 V ≈ -0.5, which is much lower than the differential-mode gain. Therefore, CMRR becomes significantly high. Thus, we observe the behavior of a differential amplifier since the common-mode voltage is rejected and the differential-mode voltage is amplified.