Ultra-Small, Low-Power, 16-Bit Analog-to-Digital Converter with Internal Reference

Check for Samples: ADS1115-Q1

FEATURES

- **WIDE SUPPLY RANGE: 2.0V to 5.5V**
- **LOW CURRENT CONSUMPTION:**
  Continuous Mode: Only 150µA
  Single-Shot Mode: Auto Shut-Down
- **PROGRAMMABLE DATA RATE:**
  8SPS to 860SPS
- **INTERNAL LOW-DRIFT VOLTAGE REFERENCE**
- **INTERNAL OSCILLATOR**
- **INTERNAL PGA**
- **I²C™ INTERFACE: Pin-Selectable Addresses**
- **FOUR SINGLE-ENDED OR TWO DIFFERENTIAL INPUTS**
- **PROGRAMMABLE COMPARATOR**

APPLICATIONS

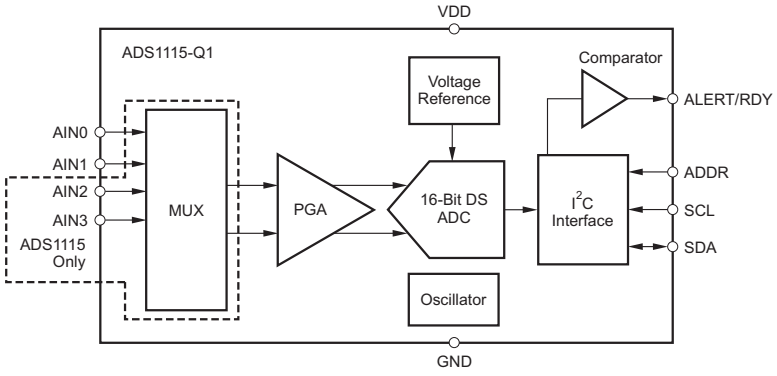
- **AUTOMOTIVE APPLICATIONS**
- **PORTABLE INSTRUMENTATION**
- **CONSUMER GOODS**
- **BATTERY MONITORING**
- **TEMPERATURE MEASUREMENT**
- **FACTORY AUTOMATION AND PROCESS CONTROLS**

DESCRIPTION

The ADS1115-Q1 is a precision analog-to-digital converter (ADCs) with 16 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1115-Q1 is designed with precision, power, and ease of implementation in mind. The ADS1115-Q1 feature an onboard reference and oscillator. Data are transferred via an I²C-compatible serial interface; four I²C slave addresses can be selected. The ADS1115-Q1 operates from a single power supply ranging from 2.0V to 5.5V.

The ADS1115-Q1 can perform conversions at rates up to 860 samples per second (SPS). An onboard PGA is available on the ADS1115 that offers input ranges from the supply to as low as ±256mV, allowing both large and small signals to be measured with high resolution. The ADS1115 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

The ADS1115-Q1 operate either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1115-Q1 is specified from –40°C to +125°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

ORDERABLE P/N	T_A	PACKAGE	TOP SIDE SYMBOL
ADS1115QDGSRQ1	-40°C to 125°C	VSSOP - DGS/ Reel of 2500	BCOQ

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
VDD to GND	–0.3 to +5.5	V
Analog input current	100, momentary	mA
Analog input current	10, continuous	mA
Analog input voltage to GND	–0.3 to VDD + 0.3	V
SDA, SCL, ADDR, ALERT/RDY voltage to GND	–0.5 to +5.5	V
Maximum junction temperature	+150	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS1115-Q1 DGS 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	187.44	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.28	
θ_{JB}	Junction-to-board thermal resistance	108.97	
ψ_{JT}	Junction-to-top characterization parameter	2.78	
ψ_{JB}	Junction-to-board characterization parameter	107.11	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C, $T_A = T_J$

PARAMETER	TEST CONDITIONS	ADS1115-Q1 MIN	ADS1115-Q1 TYP	ADS1115-Q1 MAX	UNIT
ANALOG INPUT					
Full-scale input voltage(1)	$V_{IN} = (AIN_P) – (AIN_N)$		±4.096/PGA		V
Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Differential input impedance			See Table 2		
Common-mode input impedance	FS = ±6.144V(1)		10		MΩ
	FS = ±4.096V(1), ±2.048V		6		MΩ
	FS = ±1.024V		3		MΩ
	FS = ±0.512V, ±0.256V		100		MΩ
SYSTEM PERFORMANCE					
Resolution	No missing codes	16			Bits
Data rate (DR)			8, 16, 32, 64, 128, 250, 475, 860		SPS
Data rate variation	All data rates	–10		10	%
Output noise		See Typical Characteristics			
Integral nonlinearity	DR = 8SPS, FS = ±2.048V, best fit(2)			1	LSB
Offset error	FS = ±2.048V, differential inputs		±1	±3	LSB
	FS = ±2.048V, single-ended inputs		±3		LSB
Offset drift	FS = ±2.048V		0.005		LSB/°C
Offset power-supply rejection	FS = ±2.048V		1		LSB/V
Gain error(3)	FS = ±2.048V at 25°C		0.01	0.15	%
Gain drift(3)	FS = ±0.256V		7		ppm/°C
	FS = ±2.048V		5	40	ppm/°C
	FS = ±6.144V(1)		5		ppm/°C
Gain power-supply rejection			80		ppm/V
PGA gain match(3)	Match between any two PGA gains		0.02	0.1	%
Gain match	Match between any two inputs		0.05	0.1	%
Offset match	Match between any two inputs		3		LSB
Common-mode rejection	At dc and FS = ±0.256V		105		dB
	At dc and FS = ±2.048V		100		dB
	At dc and FS = ±6.144V(1)		90		dB
	f_{CM} = 60Hz, DR = 8SPS		105		dB
	f_{CM} = 50Hz, DR = 8SPS		105		dB
DIGITAL INPUT/OUTPUT					
Logic level					
V_{IH}		0.7VDD		5.5	V
V_{IL}		GND – 0.5		0.3VDD	V
V_{OL}	I_{OL} = 3mA	GND	0.15	0.4	V
Input leakage					
I_H	V_{IH} = 5.5V			10	µA
I_L	V_{IL} = GND	10			µA

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.
(2) 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.

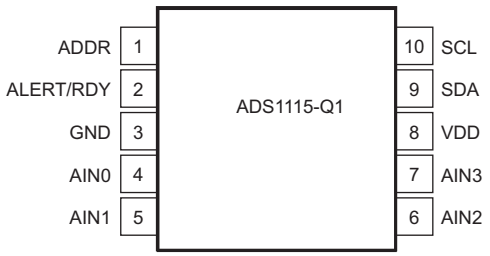
ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +125°C, VDD = 3.3V, and Full-Scale (FS) = ±2.048V, unless otherwise noted.
Typical values are at +25°C, $T_A = T_J$

PARAMETER	TEST CONDITIONS	ADS1115-Q1			UNIT
		MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage		2		5.5	V
Supply current	Power-down current at 25°C		0.5	2	µA
	Power-down current up to 125°C			5	µA
	Operating current at 25°C		150	200	µA
	Operating current up to 125°C			300	µA
Power dissipation	VDD = 5.0V		0.9		mW
	VDD = 3.3V		0.5		mW
	VDD = 2.0V		0.3		mW
TEMPERATURE					
Storage temperature		–60		+150	°C
Specified ambient temperature		–40		+125	°C

PIN CONFIGURATIONS

DGS PACKAGE
MSOP-10
(TOP VIEW)



PIN DESCRIPTIONS

PIN #	DEVICE	ANALOG/ DIGITAL INPUT/ OUTPUT	DESCRIPTION
1	ADDR	Digital Input	I^2C slave address select
2	ALERT/RDY	Digital Output	Digital comparator output or conversion ready
3	GND	Analog	Ground
4	AIN0	Analog Input	Differential channel 1: Positive input or single-ended channel 1 input
5	AIN1	Analog Input	Differential channel 1: Negative input or single-ended channel 2 input
6	AIN2	Analog Input	Differential channel 2: Positive input or single-ended channel 3 input
7	AIN3	Analog Input	Differential channel 2: Negative input or single-ended channel 4 input
8	VDD	Analog	Power supply: 2.0V to 5.5V
9	SDA	Digital I/O	Serial data: Transmits and receives data
10	SCL	Digital Input	Serial clock input: Clocks data on SDA

TIMING REQUIREMENTS

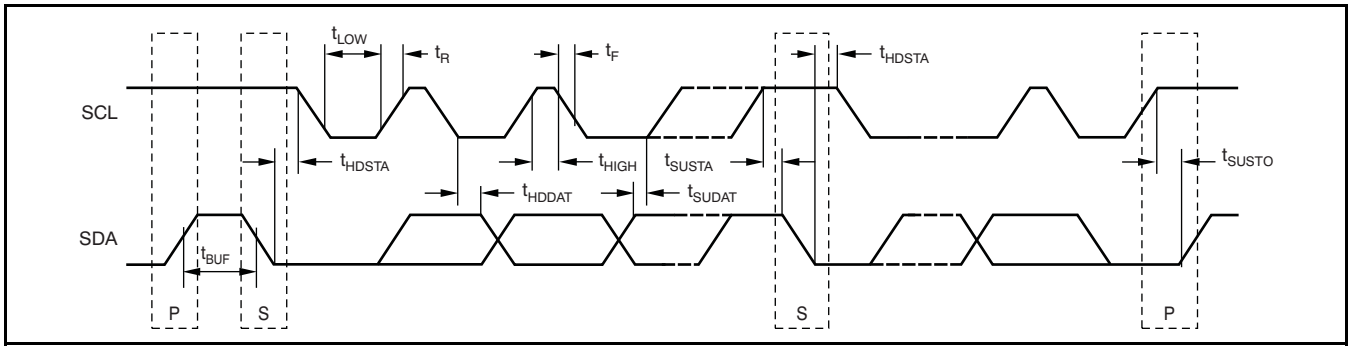


Figure 1. I²C Timing Diagram

Table 1. I²C Timing Definitions (Not included in production flow)

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL operating frequency	f_{SCL}	0.01	0.4	0.01	3.4	MHz
Bus free time between START and STOP condition	t_{BUF}	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	t_{HDSTA}	600		160		ns
Repeated START condition setup time	t_{SUSTA}	600		160		ns
Stop condition setup time	t_{SUSTO}	600		160		ns
Data hold time	t_{HDDAT}	0		0		ns
Data setup time	t_{SUDAT}	100		10		ns
SCL clock low period	t_{LOW}	1300		160		ns
SCL clock high period	t_{HIGH}	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns

TYPICAL CHARACTERISTICS

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

OPERATING CURRENT vs TEMPERATURE

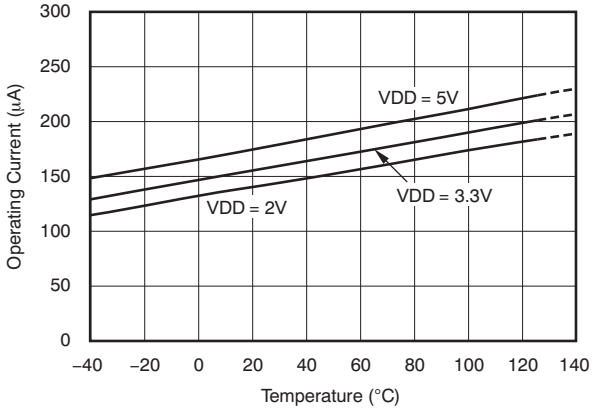


Figure 2.

SHUTDOWN CURRENT vs TEMPERATURE

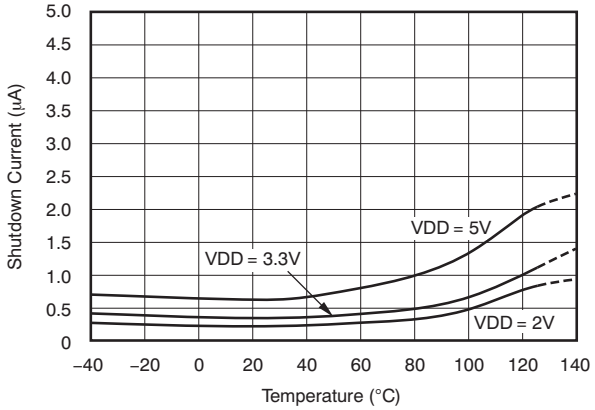


Figure 3.

SINGLE-ENDED OFFSET ERROR vs TEMPERATURE(1)

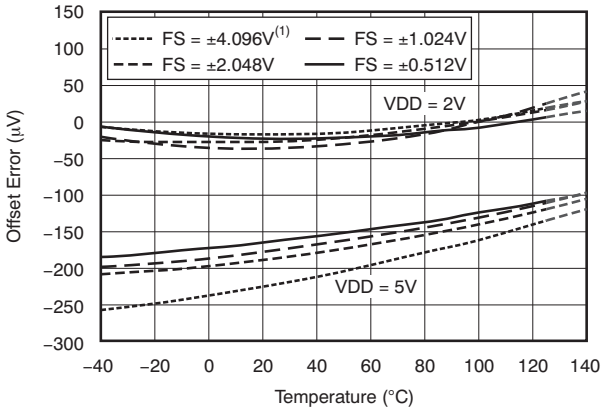


Figure 4.

DIFFERENTIAL OFFSET vs TEMPERATURE

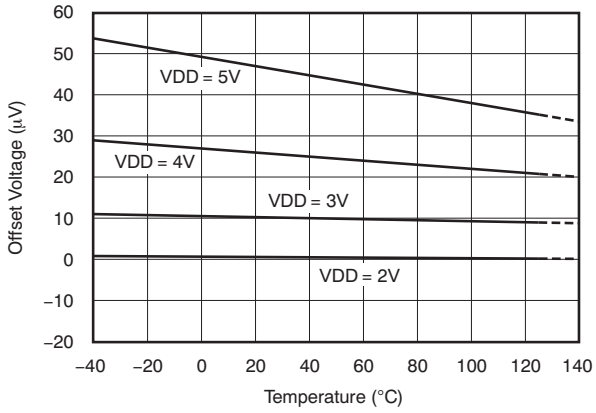


Figure 5.

GAIN ERROR vs TEMPERATURE

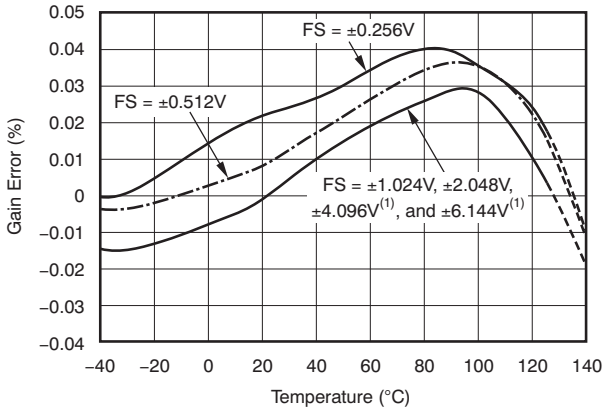


Figure 6.

GAIN ERROR vs SUPPLY

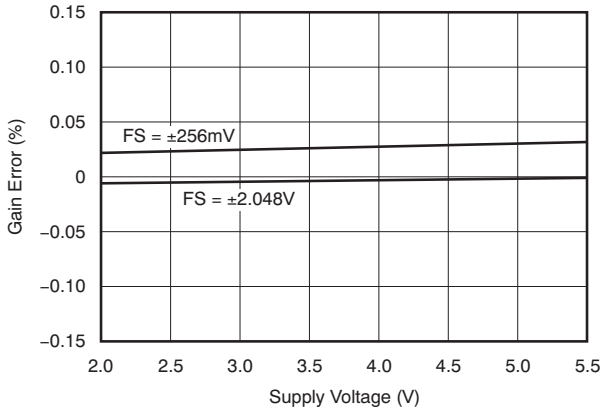


Figure 7.

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

INL vs SUPPLY VOLTAGE(2)

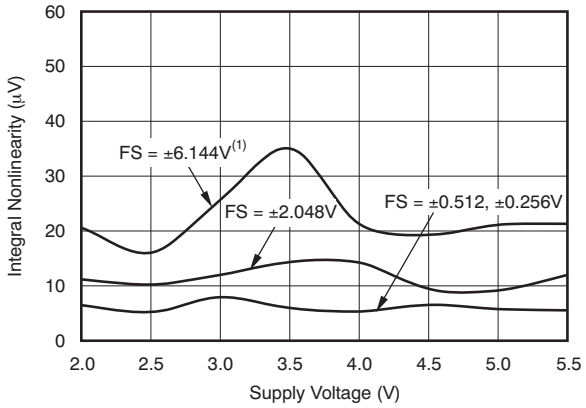


Figure 8.

INL vs INPUT SIGNAL

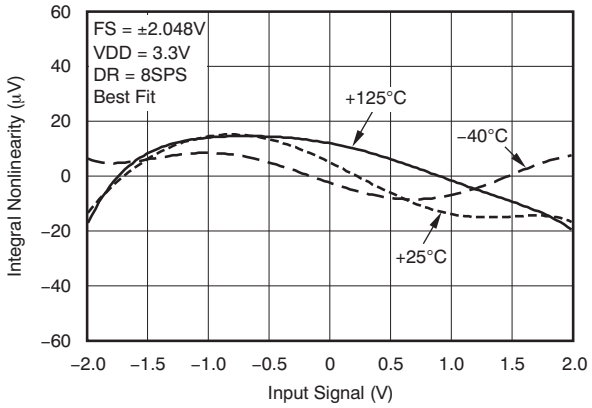


Figure 9.

INL vs INPUT SIGNAL

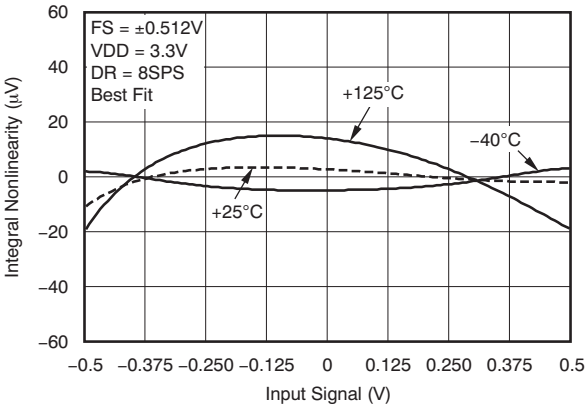


Figure 10.

INL vs INPUT SIGNAL

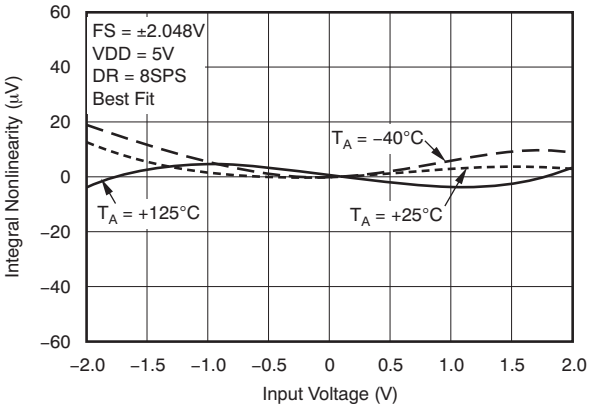


Figure 11.

INL vs INPUT SIGNAL

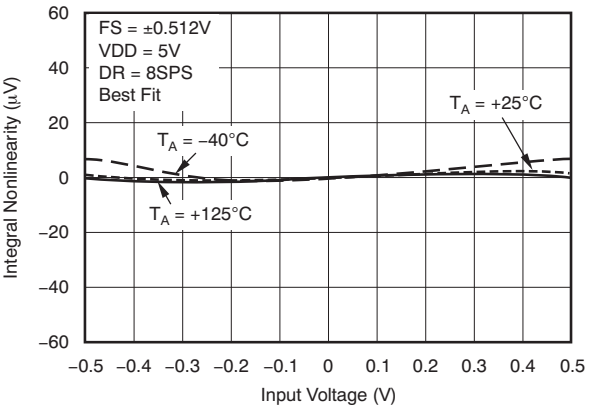


Figure 12.

INL vs TEMPERATURE

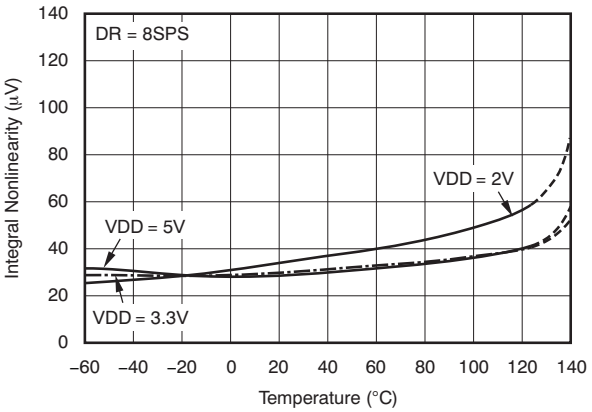


Figure 13.

(2) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

NOISE vs INPUT SIGNAL

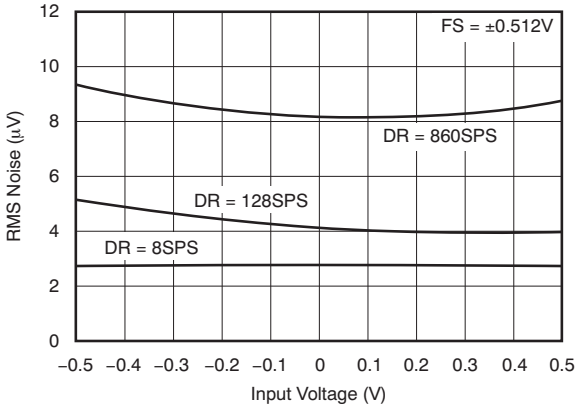


Figure 14.

NOISE vs SUPPLY VOLTAGE

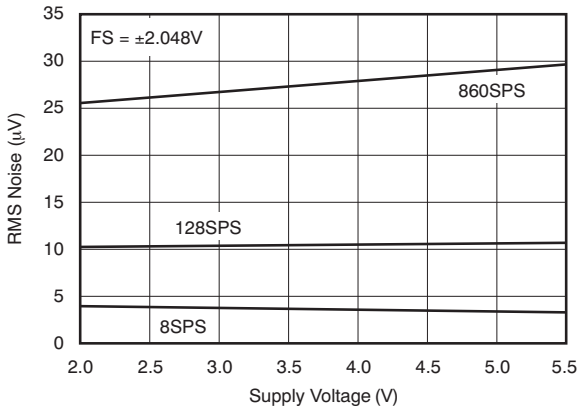


Figure 15.

NOISE vs TEMPERATURE

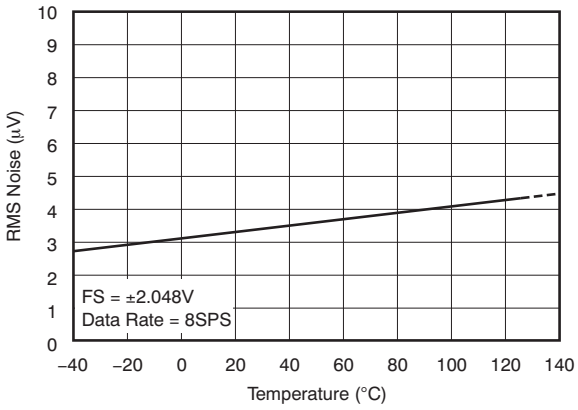


Figure 16.

GAIN ERROR HISTOGRAM

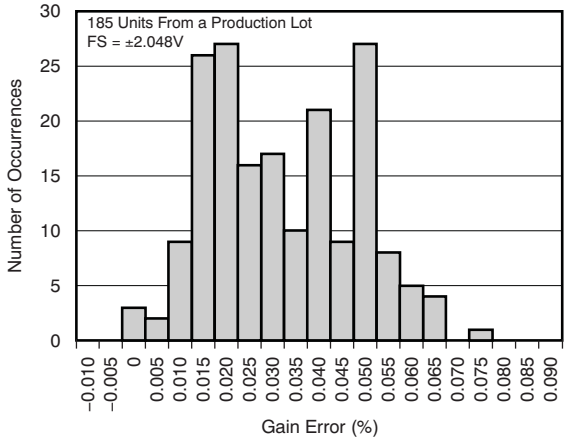


Figure 17.

OFFSET HISTOGRAM

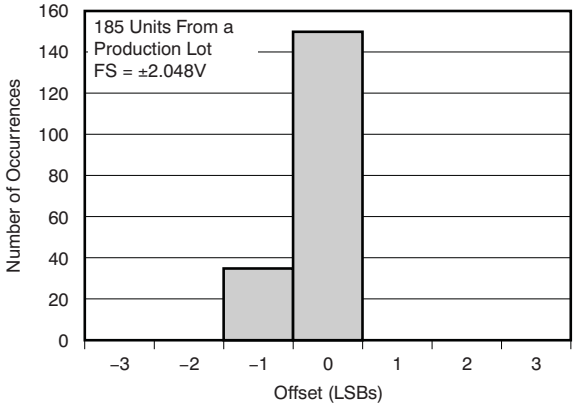


Figure 18.

TOTAL ERROR vs INPUT SIGNAL

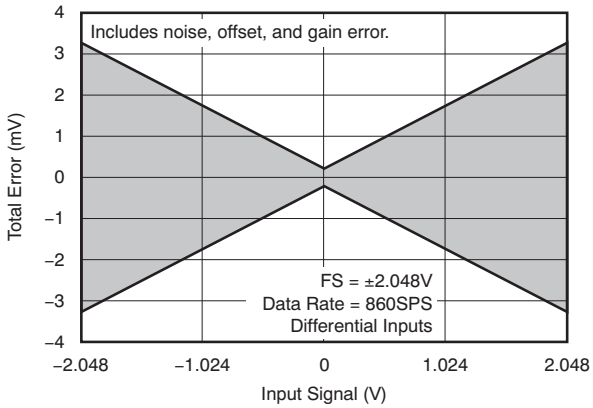


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3V, unless otherwise noted.

DATA RATE vs TEMPERATURE

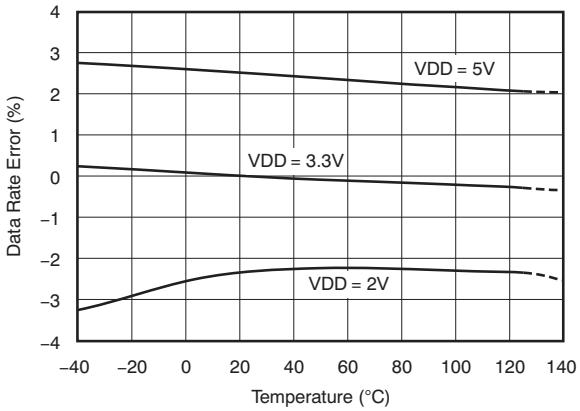


Figure 20.

FREQUENCY RESPONSE

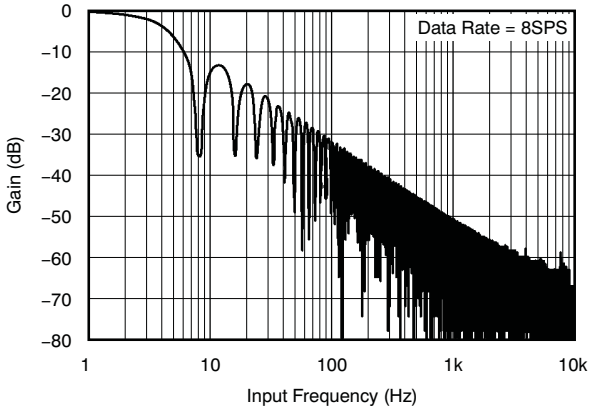


Figure 21.

OVERVIEW

The ADS1115-Q1 is a small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS1115-Q1 is an easy to configure and design into a wide variety of applications, and allow precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1115-Q1 intuitive and problem-free.

The ADS1115-Q1 consists of a ΔΣ analog-to-digital (A/D) core with adjustable gain, an internal voltage reference, a clock oscillator, and an I^2C interface. An additional feature available on the ADS1115-Q1 is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance. Figure 22 shows the ADS1115-Q1 functional block diagram.

The ADS1115-Q1 A/D core measures a differential signal, V_{IN}, that is the difference of AIN_P and AIN_N. A MUX is available on the ADS1115. This architecture results in a strong attenuation in any common-mode signals. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1115-Q1 have two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion.

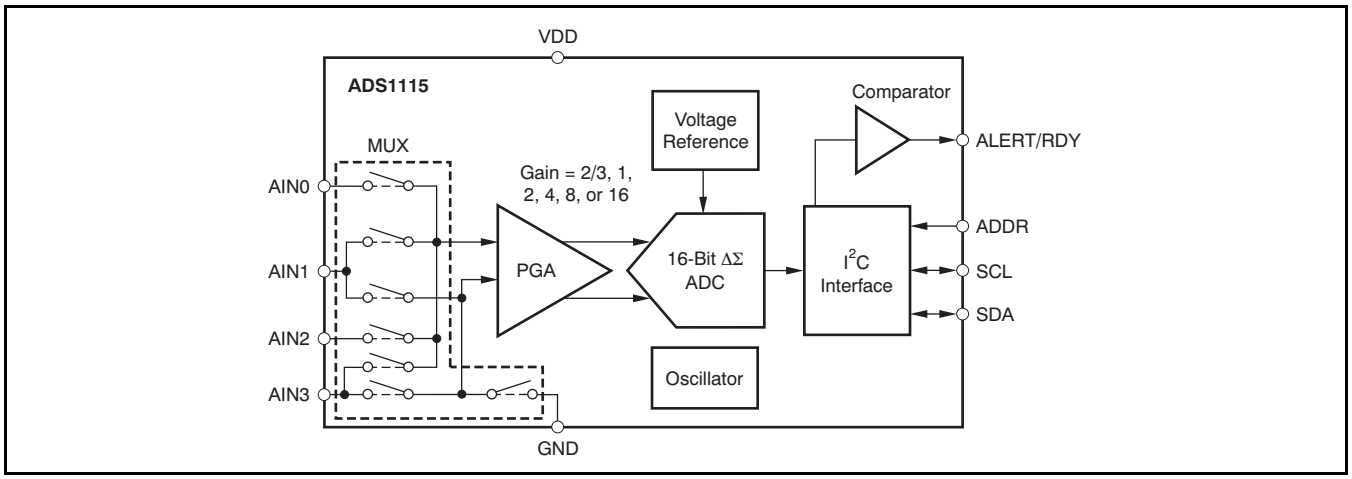


Figure 22. ADS1115-Q1 Functional Block Diagram

QUICKSTART GUIDE

This section provides a brief example of the ADS1115-Q1 communications. Refer to subsequent sections of this data sheet for more detailed explanations. Hardware for this design includes: one ADS1115-Q1 configured with an I^2C address of 1001000; a microcontroller with an I^2C interface (TI recommends the MSP430F2002); discrete components such as resistors, capacitors, and serial connectors; and a 2V to 5V power supply. Figure 23 shows the basic hardware configuration.

The ADS1115-Q1 communicates with the master (microcontroller) through an I^2C interface. The master provides a clock signal on the SCL pin and data are transferred via the SDA pin. The ADS1115-Q1 never drives the SCL pin. For information on programming and debugging the microcontroller being used, see the device-specific product data sheet.

The first byte sent by the master should be the ADS1115-Q1 address followed by a bit that instructs the ADS1115-Q1 to listen for a subsequent byte. The second byte is the register pointer. See Table 9 for a register map. The third and fourth bytes sent from the master are written to the register indicated in the second byte. Refer to Figure 30 and Figure 31 for read and write operation timing diagrams, respectively. All read and write transactions with the ADS1115-Q1 must be preceded by a start condition and followed by a stop condition.

For example, to write to the configuration register to set the ADS1115-Q1 to continuous conversion mode and then read the conversion result, send the following bytes in this order:

Write to Config register:

First byte: 0b10010000 (first 7-bit I^2C address followed by a low read/write bit)

Second byte: 0b00000001 (points to Config register)

Third byte: 0b10000100 (MSB of the Config register to be written)

Fourth byte: 0b10000011 (LSB of the Config register to be written)

Write to Pointer register:

First byte: 0b10010000 (first 7-bit I^2C address followed by a low read/write bit)

Second byte: 0b00000000 (points to Conversion register)

Read Conversion register:

First byte: 0b10010001 (first 7-bit I^2C address followed by a high read/write bit)

Second byte: the ADS1115-Q1 response with the MSB of the Conversion register

Third byte: the ADS1115-Q1 response with the LSB of the Conversion register

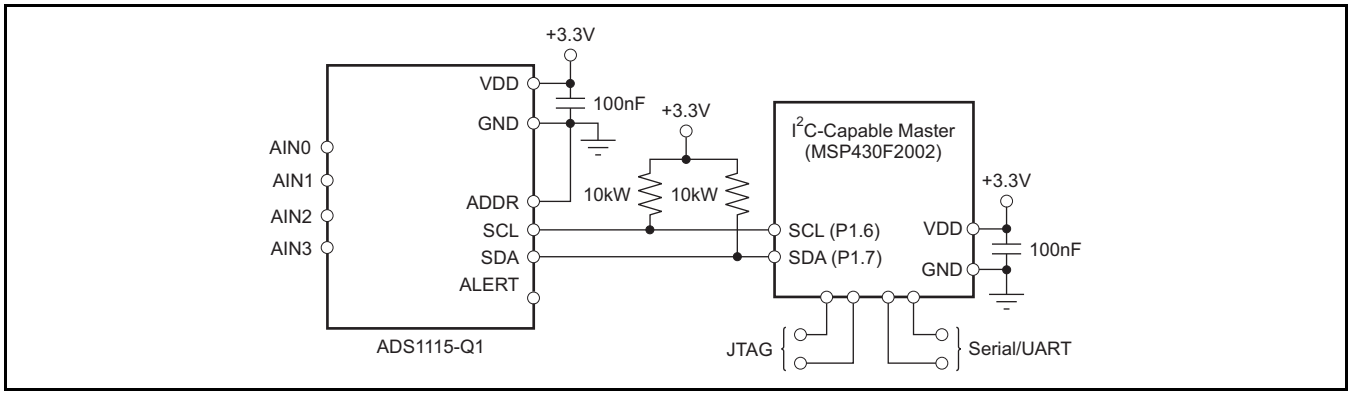


Figure 23. Basic Hardware Configuration

MULTIPLEXER

The ADS1115-Q1 contains an input multiplexer, as shown in Figure 24. Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 may be measured differentially to AIN3. The multiplexer is configured by three bits in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

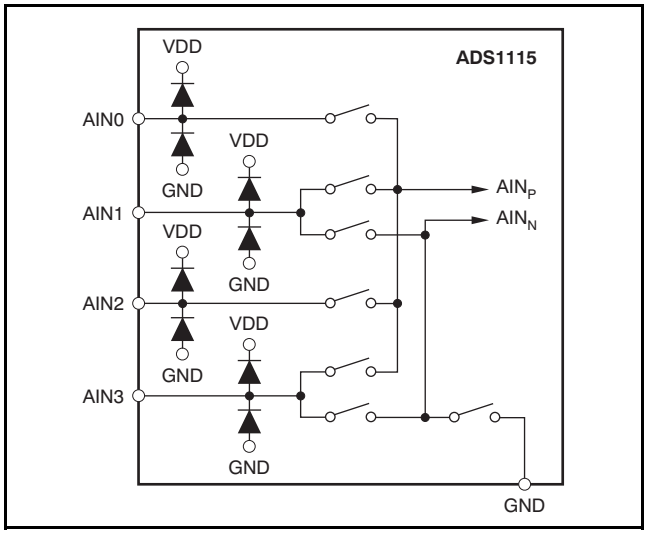


Figure 24. ADS1115 MUX

When measuring single-ended inputs it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals such as (AIN_P – AIN_N) < 0. ESD diodes to VDD and GND protect the inputs on this device. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the following range:

GND – 0.3V < AINx < VDD + 0.3V (1)

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Also, overdriving one unused input on the ADS1115-Q1 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, again it is recommended to clamp the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1115-Q1 use a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The capacitors used are small, and to external circuitry the average loading appears resistive. This structure is shown in Figure 26. The resistance is set by the capacitor values and the rate at which they are switched. Figure 25 shows the on/off setting of the switches illustrated in Figure 26. During the sampling phase, S_1 switches are closed. This event charges C_{A1} to AIN_P, C_{A2} to AIN_N, and C_B to (AIN_P – AIN_N). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7V and C_B discharges to 0V. This charging draws a very small transient current from the source driving the ADS1115-Q1 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}) where $R_{eff} = V_{IN}/I_{AVERAGE}$.

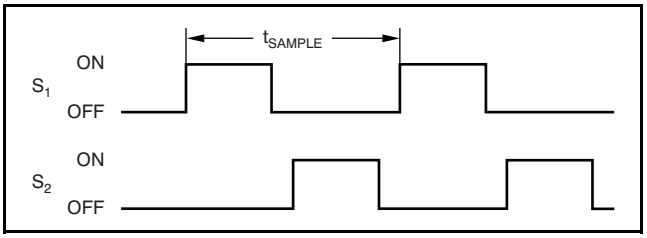


Figure 25. S_1 and S_2 Switch Timing for Figure 26

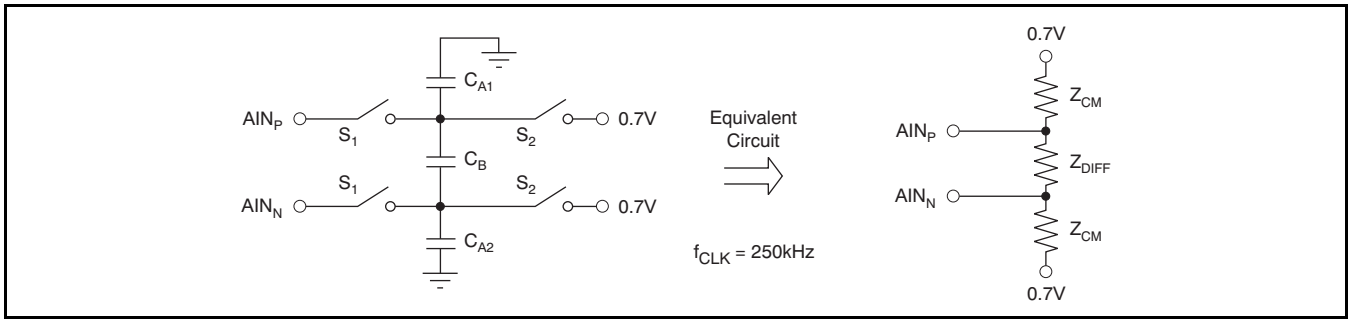


Figure 26. Simplified Analog Input Circuit

The common-mode input impedance is measured by applying a common-mode signal to shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6MΩ for the default PGA gain setting. In Figure 26, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the PGA gain setting. In Figure 26, the differential input impedance is Z_{DIFF}. Table 2 describes the typical differential input impedance.

Table 2. Differential Input Impedance

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
±6.144V(1)	22MΩ
±4.096V(1)	15MΩ
±2.048V	4.9MΩ
±1.024V	2.4MΩ
±0.512V	710kΩ
±0.256V	710kΩ

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1115-Q1 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 2 for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the ΔΣ core of the ADS1115-Q1. The PGA can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 3 shows the corresponding full-scale (FS) ranges. The PGA is configured by three bits in the Config register. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when VDD is larger than 4V. Note though that in this case (as well as for PGA = 1 and VDD < 4V), it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table.

Table 3. PGA Gain Full-Scale Range

PGA SETTING	FS (V)
2/3	±6.144V(1)
1	±4.096V(1)
2	±2.048V
4	±1.024V
8	±0.512V
16	±0.256V

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

DATA FORMAT

The ADS1115-Q1 provide 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 4 summarizes the ideal output codes for different input signals. Figure 27 shows code transitions versus input voltage.

Table 4. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ FS (2^{15} – 1)/2^{15}	7FFFh
+FS/2^{15}	0001h
0	0
–FS/2^{15}	FFFFh
≤ –FS	8000h

1. Excludes the effects of noise, INL, offset, and gain errors.

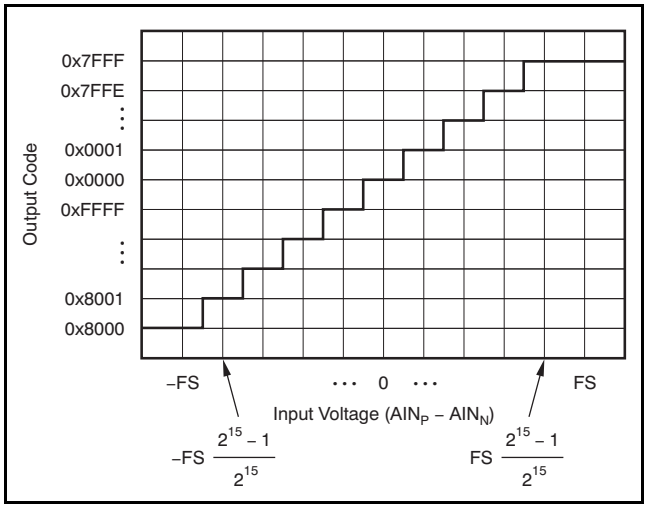


Figure 27. ADS1115-Q1 Code Transition Diagram

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1115-Q1 digital filter provides some attenuation of high-frequency noise, but the digital Sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the ADS1115-Q1.

OPERATING MODES

The ADS1115-Q1 operate in one of two modes: continuous conversion or single-shot. In continuous conversion mode, the ADS1115-Q1 continuously perform conversions. Once a conversion has been completed, the ADS1115-Q1 place the result in the Conversion register and immediately begins another conversion. In single-shot mode, the ADS1115-Q1 wait until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

RESET AND POWER-UP

When the ADS1115-Q1 powers up, a reset is performed. As part of the reset process, the ADS1115-Q1 set all of the bits in the Config register to the respective default settings.

The ADS1115-Q1 respond to the I^2C general call reset command. When the ADS1115-Q1 receive a general call reset, an internal reset is performed as if the device had been powered on.

DUTY CYCLING FOR LOW POWER

For many applications, the improved performance at low data rates may not be required. For these applications, the ADS1115-Q1 support duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1115-Q1 in power-down mode with a data rate set to 860SPS could be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 860SPS only requires about 1.2ms, the ADS1115-Q1 enter power-down mode for the remaining 123.8ms. In this configuration, the ADS1115-Q1 consume about 1/100th the power of the ADS1115-Q1 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The ADS1115-Q1 offer lower data rates that do not implement duty cycling and offer improved noise performance if it is needed.

COMPARATOR

The ADS1115-Q1 is equipped with a customizable comparator that can issue an alert on the ALERT/RDY pin. This feature can significantly reduce external circuitry for many applications. The comparator can be implemented as either a traditional comparator or a window comparator via the COMP_MODE bit in the Config register. When implemented as a traditional comparator, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the high threshold register. The comparator then deasserts when the input signal falls below the low threshold register value. In window comparator mode, the ALERT/RDY pin asserts if conversion data exceed the high threshold register or fall below the low threshold register.

In either window or traditional comparator mode, the comparator can be configured to latch once asserted by the COMP_LAT bit in the Config register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can be cleared by issuing an SMBus alert response or by reading the Conversion register. The COMP_POL bit in the Config register configures the ALERT/RDY pin as active high or active low. Operational diagrams for the comparator modes are shown in Figure 28 and Figure 29.

The comparator can be configured to activate the ALERT/RDY pin after a set number of successive readings exceed the threshold. The comparator can be configured to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin by changing the COMP_QUE bits in the Config register. The COMP_QUE bits can also disable the comparator function.

CONVERSION READY PIN

The ALERT/RDY pin can also be configured as a conversion ready pin. This mode of operation can be realized if the MSB of the high threshold register is set to '1' and the MSB of the low threshold register is set to '0'. The COMP_POL bit continues to function and the COMP_QUE bits can disable the pin; however, the COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion ready pin, ALERT/RDY continues to require a pull-up resistor. When in continuous conversion mode, the ADS1115-Q1 provide a brief (~8μs) pulse on the ALERT/RDY pin at the end of each conversion. When in single-shot shutdown mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to '0'.

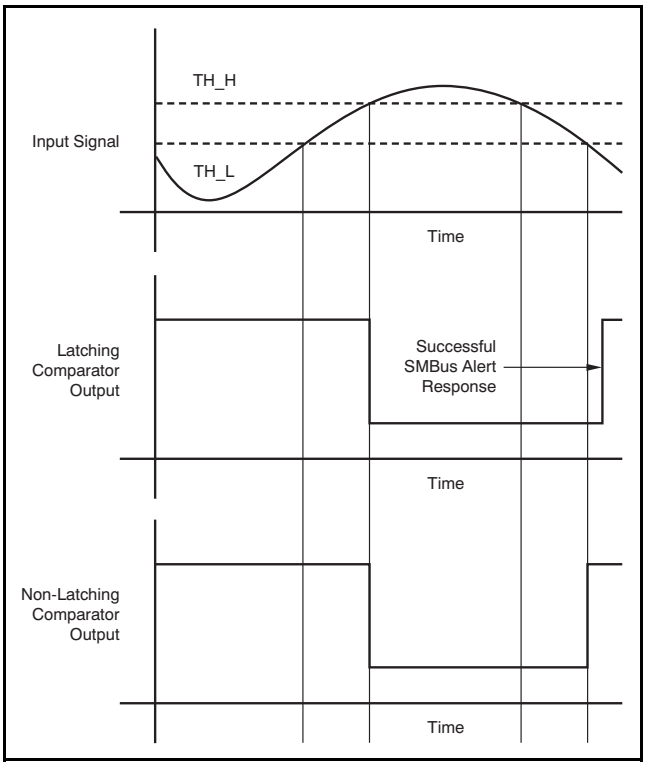


Figure 28. Alert Pin Timing Diagram When Configured as a Traditional Comparator

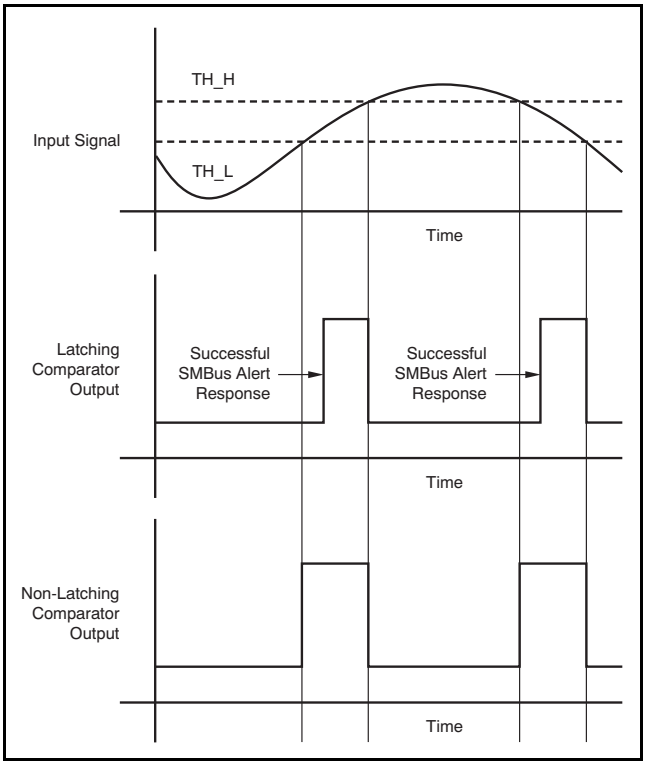


Figure 29. Alert Pin Timing Diagram When Configured as a Window Comparator

SMBus ALERT RESPONSE

When configured in latching mode (COMP_LAT = '1' in the Config register), the ALERT/RDY pin can be implemented with an SMBus alert. The pin asserts if the comparator detects a conversion that exceeds an upper or lower threshold. This interrupt is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I^2C address. If conversion data exceed the upper or lower thresholds after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin, as with the SDA pin, is an open-drain pin. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that it does not interfere with other devices on the same bus line.

When the master senses that the ALERT/RDY pin has latched, it issues an SMBus alert command (00011001) to the I^2C bus. Any ADS1115-Q1 data converters on the I^2C bus with the ALERT/RDY pins asserted respond to the command with the slave address. In the event that two or more ADS1115-Q1 data converters present on the bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert decides which device clears its assertion. The device with the lowest I^2C address always wins arbitration. If a device loses arbitration, it does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have had the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a '1' if signals exceed the high threshold and a '0' if signals exceed the low threshold.

I^2C INTERFACE

The ADS1115-Q1 communicate through an I^2C interface. I^2C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1115-Q1 can only act as slave devices.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). Once the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I^2C bus is held idle for more than 25ms, the bus times out.

The I^2C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1115-Q1 never drive SCL, because they cannot act as a master. On the ADS1115-Q1, SCL is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the *address byte*. Each device on an I^2C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an *acknowledge* bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls SDA low to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

See the *Timing Requirements* section for a timing diagram showing the ADS1115-Q1 I²C transaction.

I²C ADDRESS SELECTION

The ADS1115-Q1 have one address pin, ADDR, that sets the I²C address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 5. The state of the address pin ADDR is sampled continuously.

Table 5. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN	SLAVE ADDRESS
Ground	1001000
VDD	1001001
SDA	1001010
SCL	1001011

I²C GENERAL CALL

The ADS1115-Q1 respond to the I²C general call address (0000000) if the eighth bit is '0'. The devices acknowledge the general call address and respond to commands in the second byte. If the second byte is 00000110 (06h), the ADS1115-Q1 reset the internal registers and enter power-down mode.

I²C SPEED MODES

The I²C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called Hs mode) allows a clock frequency of up to 3.4MHz. The ADS1115-Q1 are fully compatible with all three modes.

No special action is required to use the ADS1115-Q1 in standard or fast mode, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of *00001xxx* following the START condition, where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes; the eighth bit does not indicate read/write status.) The ADS1115-Q1 do not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. Upon receiving a master code, the ADS1115-Q1 switch on Hs mode filters, and communicate at up to 3.4MHz. The ADS1115-Q1 switch out of Hs mode with the next STOP condition.

For more information on high-speed mode, consult the I²C specification.

SLAVE MODE OPERATIONS

The ADS1115-Q1 can act as either slave receivers or slave transmitters. As a slave device, the ADS1115-Q1 cannot drive the SCL line.

Receive Mode:

In slave receive mode the first byte transmitted from the master to the slave is the address with the R/$\overline{W}$ bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the register pointer byte. The ADS1115-Q1 then acknowledge receipt of the register pointer byte. The next two bytes are written to the address given by the register pointer. The ADS1115-Q1 acknowledge each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

Transmit Mode:

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/$\overline{W}$ bit. This byte places the slave into transmit mode and indicates that the ADS1115-Q1 are being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register pointer. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

WRITING/READING THE REGISTERS

To access a specific register from the ADS1115-Q1, the master must first write an appropriate value to the Pointer register. The Pointer register is written directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. After the Pointer register is written, the slave acknowledges and the master issues a STOP or a repeated START condition.

When reading from the ADS1115-Q1, the previous value written to the Pointer register determines the register that is read from. To change which register is read, a new value must be written to the Pointer register. To write a new value to the Pointer register, the master issues a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data need to be transmitted, and a STOP condition can be issued by the master. The master may now issue a START condition and send the slave address byte with the R/$\overline{W}$ bit high to begin the read. Table 10 details this sequence. If repeated reads from the same register are desired, there is no need to continually send Pointer register bytes, because the ADS1115-Q1 store the value of the Pointer register until it is modified by a write operation. However, every write operation requires the Pointer register to be written.

REGISTERS

The ADS1115-Q1 have four registers that are accessible via the I^2C port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1115-Q1 operating modes and query the status of the devices. Two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

POINTER REGISTER

The four registers are accessed by writing to the Pointer register byte; see Figure 30. Table 6 and Table 7 indicate the Pointer register byte map.

Table 6. Register Address

BIT 1	BIT 0	REGISTER
0	0	Conversion register
0	1	Config register
1	0	Lo_thresh register
1	1	Hi_thresh register

CONVERSION REGISTER

The 16-bit register contains the result of the last conversion in binary twos complement format. Following reset or power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is completed.

The register format is shown in Table 8.

CONFIG REGISTER

The 16-bit register can be used to control the ADS1115-Q1 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in Table 9.

Table 7. Pointer Register Byte (Write-Only)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	Register address	

Table 8. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 9. Config Register (Read/Write)

BIT	15	14	13	12	11	10	9	8
NAME	OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
BIT	7	6	5	4	3	2	1	0
NAME	DR2	DR1	DR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0

Default = 8583h.

Bit [15] **OS: Operational status/single-shot conversion start**

This bit determines the operational status of the device.
This bit can only be written when in power-down mode.

For a write status:
0 : No effect
1 : Begin a single conversion (when in power-down mode)
For a read status:
0 : Device is currently performing a conversion
1 : Device is not currently performing a conversion

Bits [14:12] **MUX[2:0]: Input multiplexer configuration**

These bits configure the input multiplexer.

000 : AIN_P = AIN0 and AIN_N = AIN1 (default)	100 : AIN_P = AIN0 and AIN_N = GND
001 : AIN_P = AIN0 and AIN_N = AIN3	101 : AIN_P = AIN1 and AIN_N = GND
010 : AIN_P = AIN1 and AIN_N = AIN3	110 : AIN_P = AIN2 and AIN_N = GND
011 : AIN_P = AIN2 and AIN_N = AIN3	111 : AIN_P = AIN3 and AIN_N = GND

Bits [11:9] **PGA[2:0]: Programmable gain amplifier configuration**

These bits configure the programmable gain amplifier.

000 : FS = ±6.144V(1)	100 : FS = ±0.512V
001 : FS = ±4.096V(1)	101 : FS = ±0.256V
010 : FS = ±2.048V (default)	110 : FS = ±0.256V
011 : FS = ±1.024V	111 : FS = ±0.256V

Bit [8] **MODE: Device operating mode**

This bit controls the current operational mode of the ADS1115-Q1.
0 : Continuous conversion mode
1 : Power-down single-shot mode (default)

Bits [7:5] **DR[2:0]: Data rate**

These bits control the data rate setting.

000 : 8SPS	100 : 128SPS (default)
001 : 16SPS	101 : 250SPS
010 : 32SPS	110 : 475SPS
011 : 64SPS	111 : 860SPS

Bit [4] **COMP_MODE: Comparator mode**

This bit controls the comparator mode of operation. It changes whether the comparator is implemented as a traditional comparator (COMP_MODE = '0') or as a window comparator (COMP_MODE = '1').
0 : Traditional comparator with hysteresis (default)
1 : Window comparator

Bit [3] **COMP_POL: Comparator polarity**

This bit controls the polarity of the ALERT/RDY pin. When COMP_POL = '0' the comparator output is active low. When COMP_POL='1' the ALERT/RDY pin is active high.
0 : Active low (default)
1 : Active high

Bit [2] **COMP_LAT: Latching comparator**

This bit controls whether the ALERT/RDY pin latches once asserted or clears once conversions are within the margin of the upper and lower threshold values. When COMP_LAT = '0', the ALERT/RDY pin does not latch when asserted. When COMP_LAT = '1', the asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master, the device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line.
0 : Non-latching comparator (default)
1 : Latching comparator

Bits [1:0] **COMP_QUE: Comparator queue and disable**

These bits perform two functions. When set to '11', they disable the comparator function and put the ALERT/RDY pin into a high state. When set to any other value, they control the number of successive conversions exceeding the upper or lower thresholds required before asserting the ALERT/RDY pin.
00 : Assert after one conversion
01 : Assert after two conversions
10 : Assert after four conversions
11 : Disable comparator (default)

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Lo_thresh AND Hi_thresh REGISTERS

The upper and lower threshold values used by the comparator are stored in two 16-bit registers. These registers store values in the same format that the output register displays values; that is, they are stored in twos complement format. Because it is implemented as a digital comparator, special attention should be taken to readjust values whenever PGA settings are changed.

A secondary conversion ready function of the comparator output pin can be realized by setting the Hi_thresh register MSB to '1' and the Lo_thresh register MSB to '0'. However, in all other cases, the Hi_thresh register must be larger than the Lo_thresh register. The threshold register formats are shown in Table 10. When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode and pulses when in continuous conversion mode.

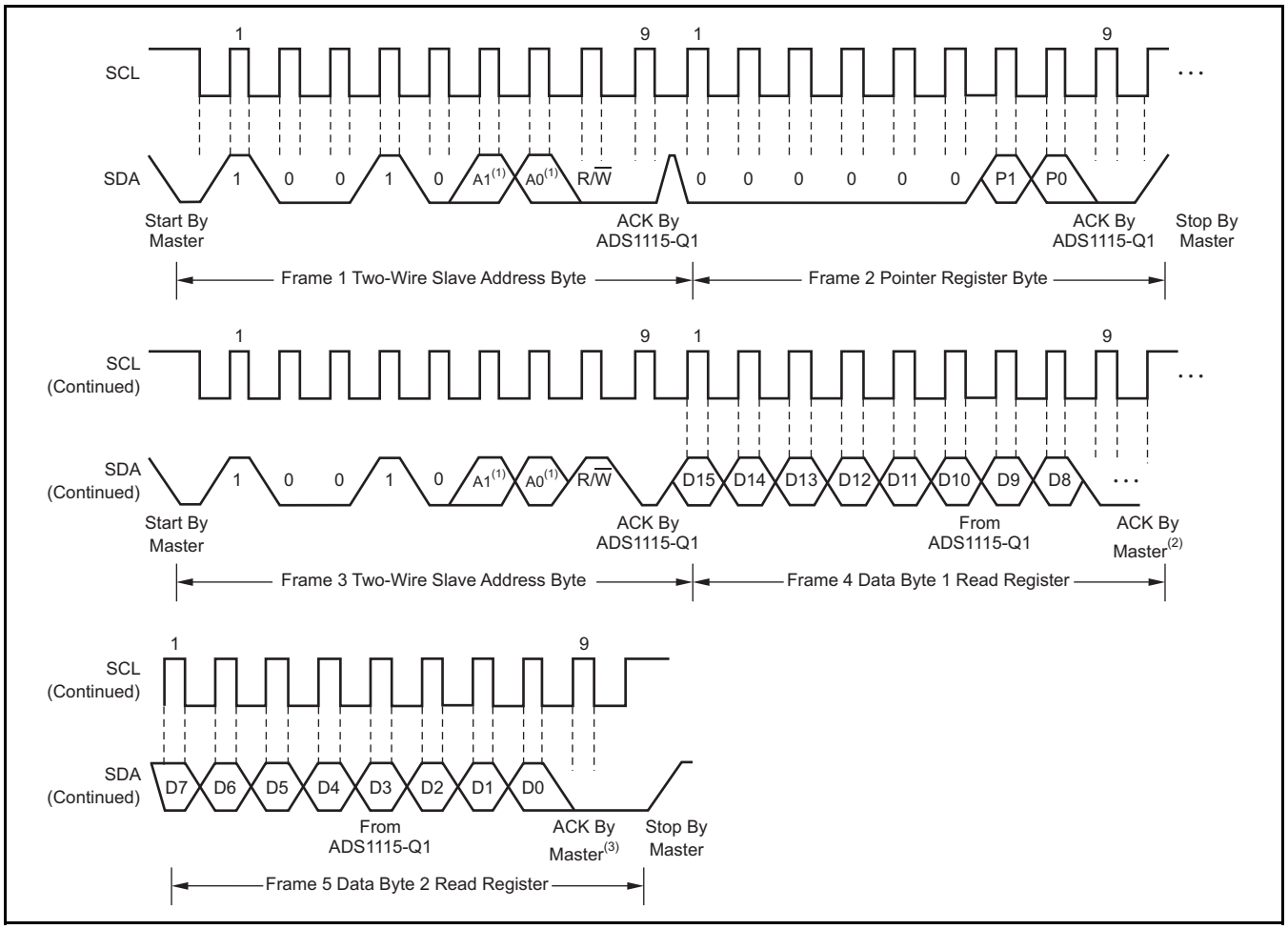
Table 10. Lo_thresh and Hi_thresh Registers

REGISTER	Lo_thresh (Read/Write)							
BIT	15	14	13	12	11	10	9	8
NAME	Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
BIT	7	6	5	4	3	2	1	0
NAME	Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0

REGISTER	Hi_thresh (Read/Write)							
BIT	15	14	13	12	11	10	9	8
NAME	Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
BIT	7	6	5	4	3	2	1	0
NAME	Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0

Lo_thresh default = 8000h.

Hi_thresh default = 7FFFh.

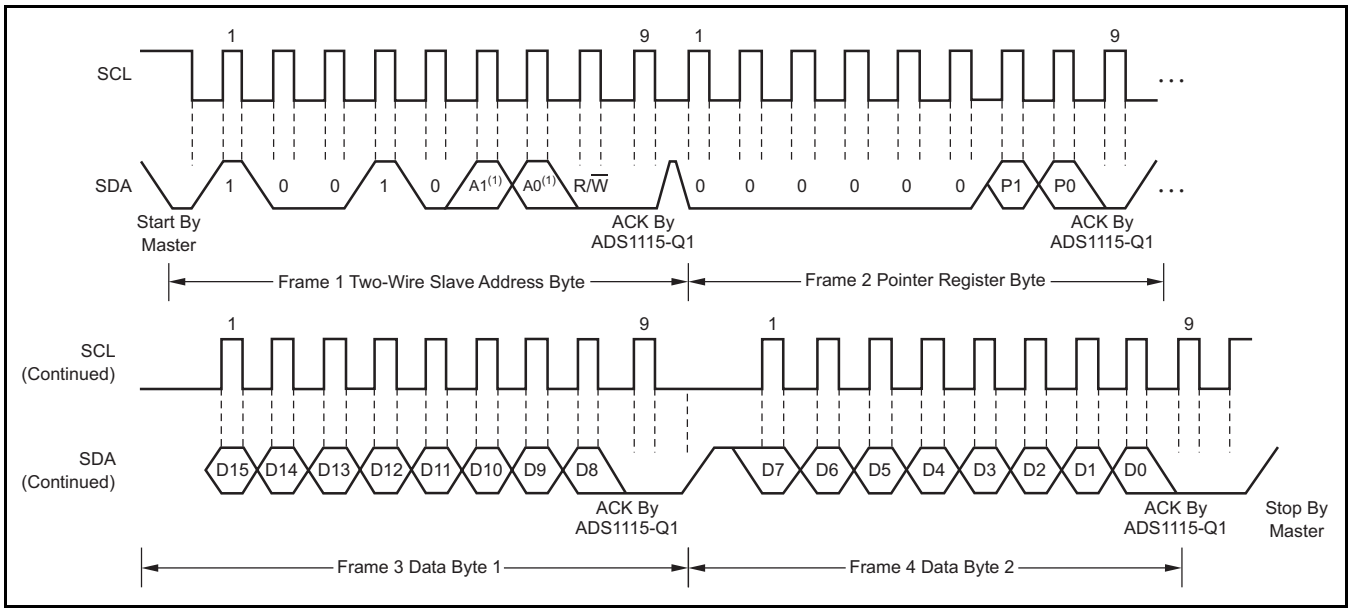


(1) The values of A0 and A1 are determined by the ADDR pin.

(2) Master can leave SDA high to terminate a single-byte read operation.

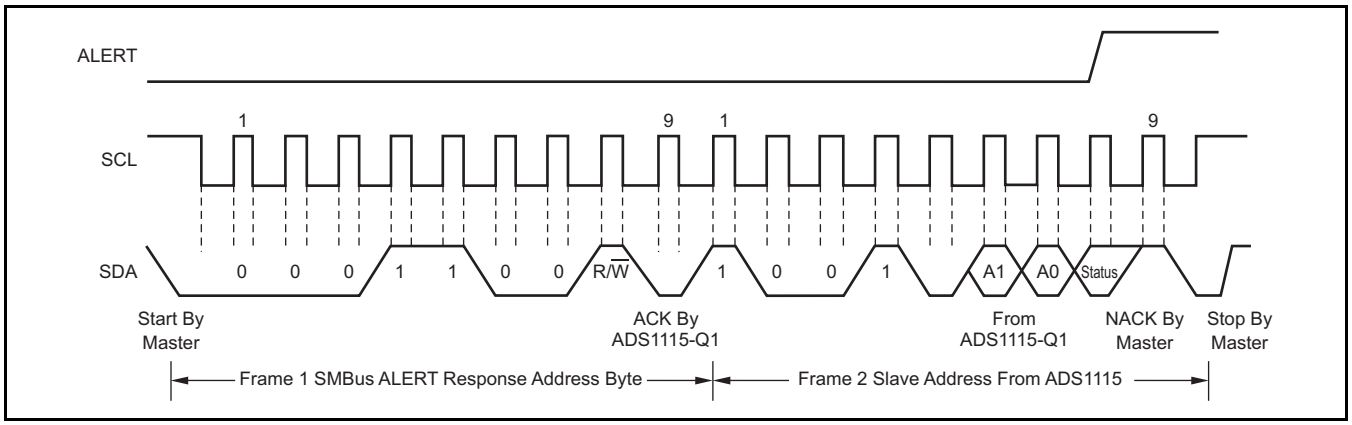
(3) Master can leave SDA high to terminate a two-byte read operation.

Figure 30. Two-Wire Timing Diagram for Read Word Format



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 31. Two-Wire Timing Diagram for Write Word Format



(1) The values of A0 and A1 are determined by the ADDR pin.

Figure 32. Timing Diagram for SMBus ALERT Response

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1115-Q1 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1115-Q1 is simple. A basic connection diagram for the ADS1115-Q1 is shown in Figure 33.

The fully differential voltage input of the ADS1115-Q1 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS1115-Q1 can read bipolar differential signals, they cannot accept negative voltages on either input. It may be helpful to think of the ADS1115-Q1 positive voltage input as *noninverting*, and of the negative input as *inverting.*

When the ADS1115-Q1 are converting data, they draw current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1115-Q1 interface directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, can operate with the ADS1115-Q1. The ADS1115-Q1 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this function unless other clock-stretching devices are on the same I^2C bus.

Pull-up resistors are required on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

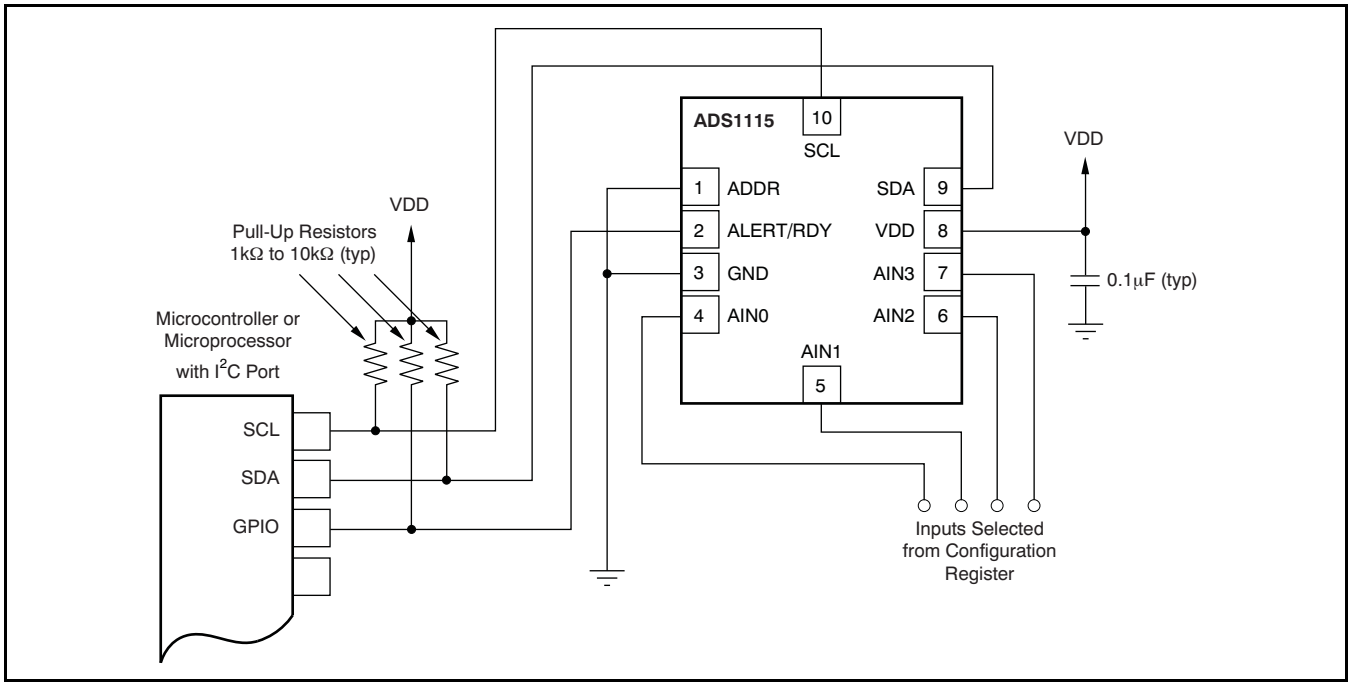


Figure 33. Typical Connections of the ADS1115-Q1

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1115-Q1s to a single bus is simple. Using the address pin, the ADS1115-Q1 can be set to one of four different I^2C addresses. An example showing three ADS1115-Q1 devices is given in Figure 35. Up to four ADS1115-Q1s (using different address pin configurations) can be connected to a single bus.

Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

The TMP421 and DAC8574 devices detect the respective I^2C bus addresses based on the states of pins. In the example, the TMP421 has the address 0101010, and the DAC8574 has the address 1001100. Consult the DAC8574 and TMP421 data sheets, available at www.ti.com, for further details.

USING GPIO PORTS FOR COMMUNICATION

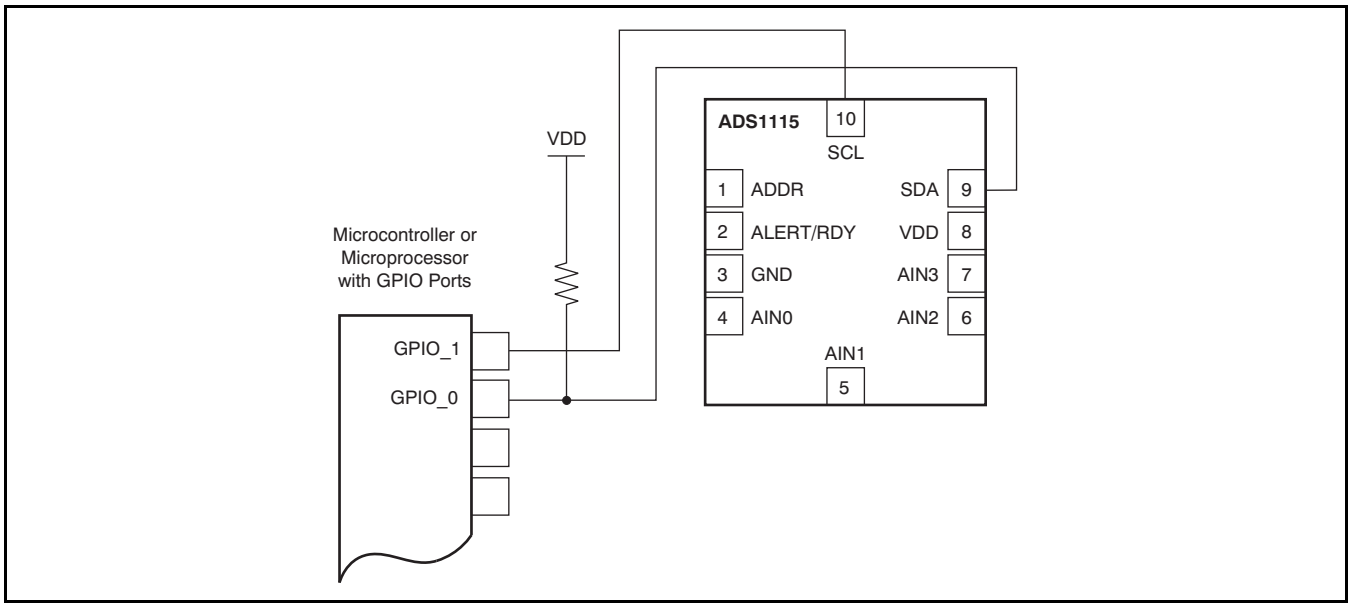
Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an I^2C controller is not available, the ADS1115-Q1 can be connected to GPIO pins and the I^2C bus protocol simulated, or *bit-banged*, in software. An example of this configuration for a single ADS1115-Q1 is shown in Figure 34.

Bit-banging I^2C with GPIO pins can be done by setting the GPIO line to '0' and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this configuration reads as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. This action is possible because the ADS1115-Q1 never drive the clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption as a result of the absence of a resistive pull-up.

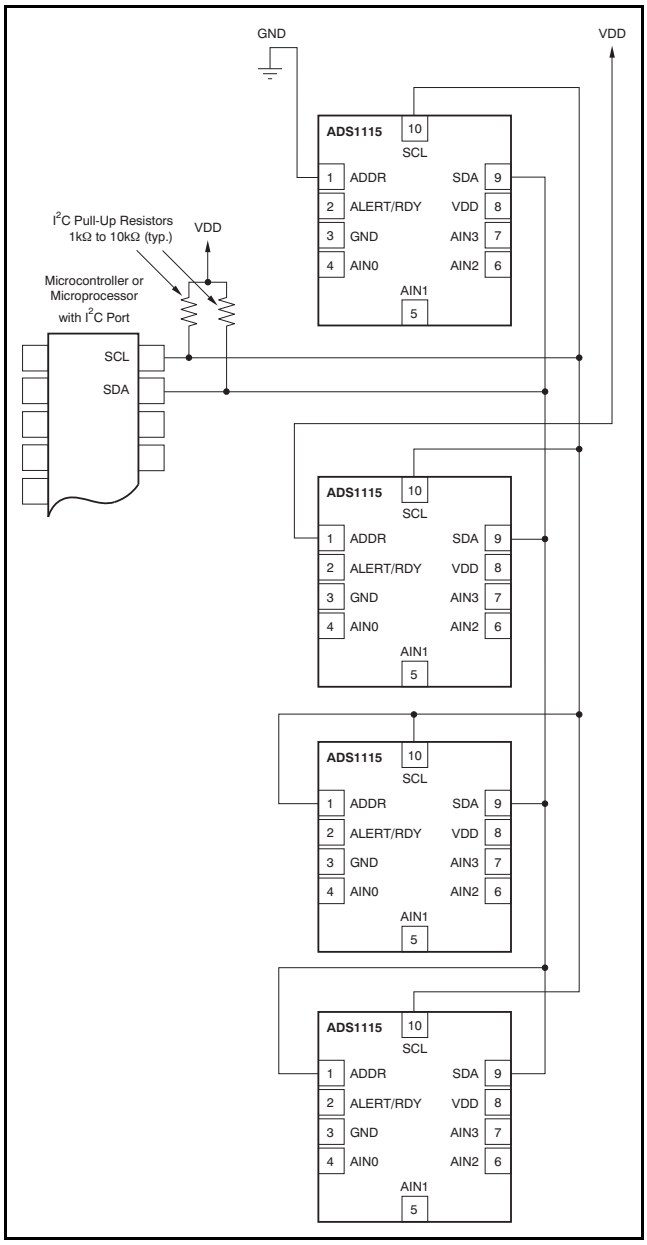
If there are any devices on the bus that may drive the clock lines low, this method should not be used; the SCL line should be high-Z or '0' and a pull-up resistor provided as usual.

Some microcontrollers have selectable strong pull-up circuits built in to the GPIO ports. In some cases, these circuits can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I^2C communication. If there is any doubt about the matter, test the circuit before committing it to production.



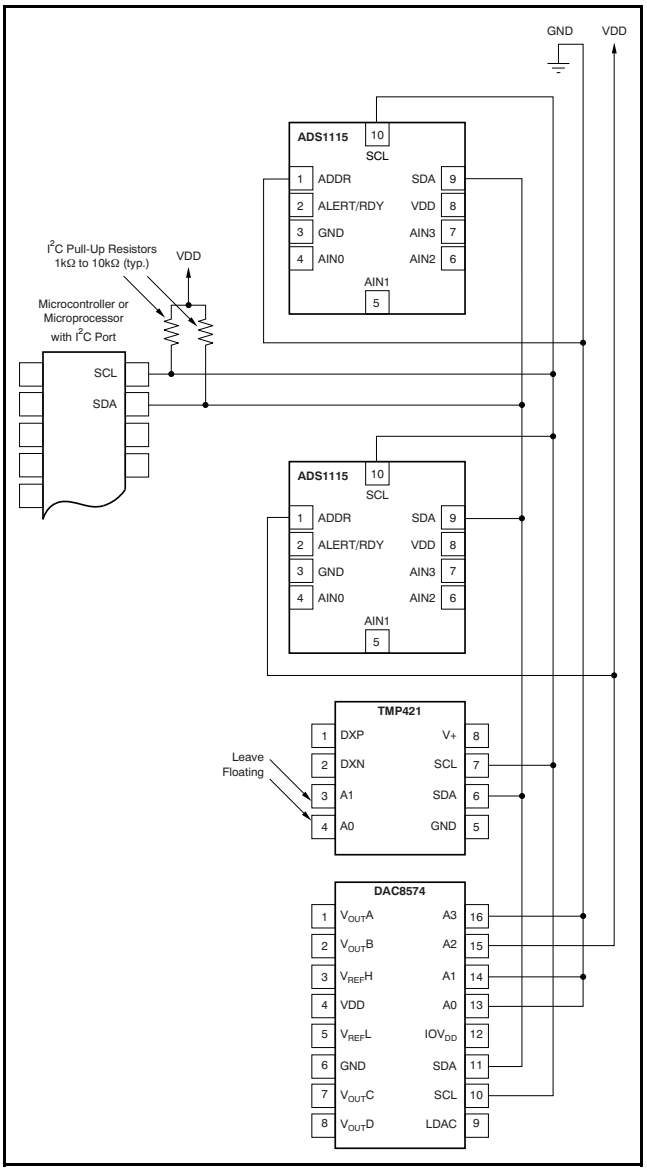
NOTE: ADS1115-Q1 power and input connections omitted for clarity.

Figure 34. Using GPIO with a Single ADS1115-Q1



NOTE: The ADS1115-Q1 power and input connections are omitted for clarity. The ADDR pin selects the I^2C address.

Figure 35. Connecting Multiple ADS1115-Q1s



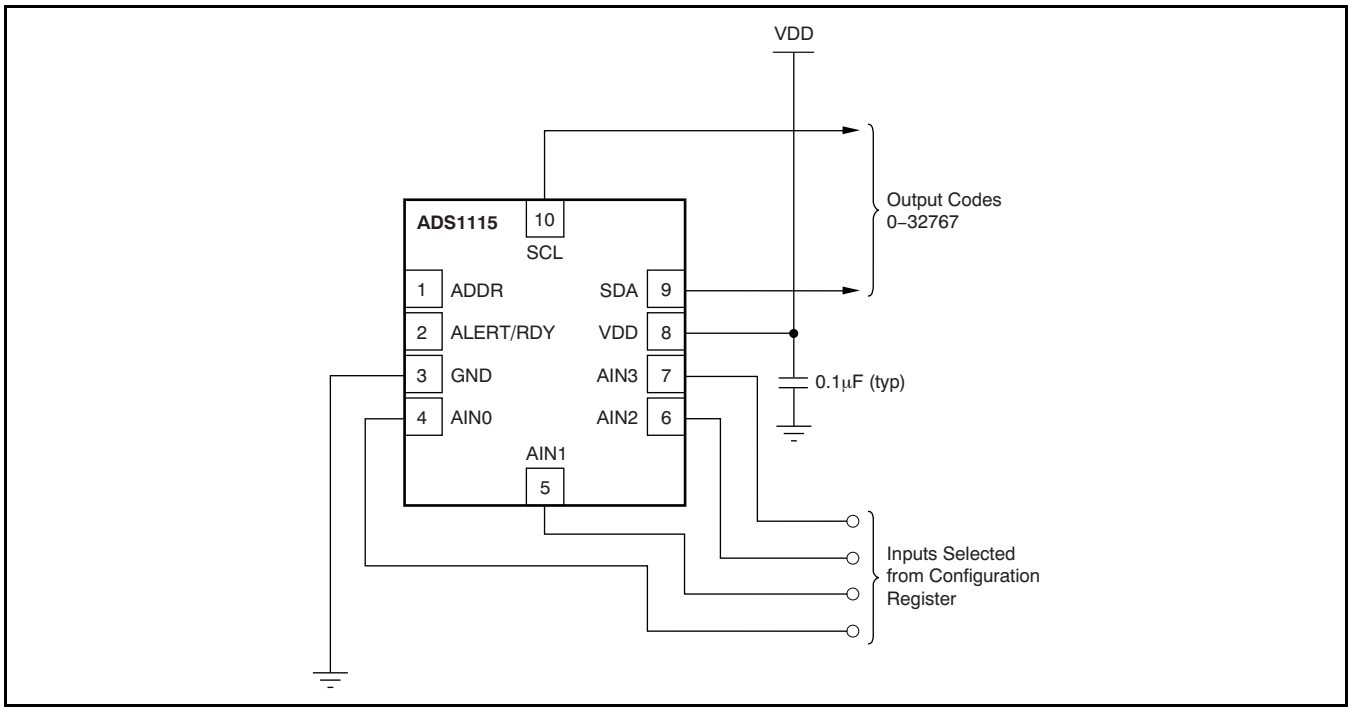
NOTE: ADS1115-Q1 power and input connections are omitted for clarity. ADDR, A3, A2, A1, and A0 select the I^2C addresses.

Figure 36. Connecting Multiple Device Types

SINGLE-ENDED INPUTS

Although the ADS1115-Q1 has two differential inputs, the device can easily measure four single-ended signals. Figure 37 shows a single-ended connection scheme. The ADS1115-Q1 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0V to supply. The ADS1115-Q1 loses no linearity anywhere within the input range. Negative voltages cannot be applied to this circuit because the ADS1115-Q1 can only accept positive voltages.

The ADS1115-Q1 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 37 covers only half the ADS1115-Q1 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.



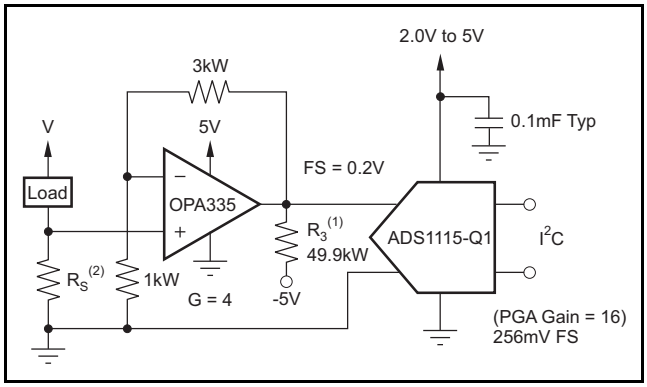
NOTE: Digital and address pin connections omitted for clarity.

Figure 37. Measuring Single-Ended Inputs

LOW-SIDE CURRENT MONITOR

Figure 38 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an OPA335 low-drift op amp, and the result is read by the ADS1115-Q1.

It is suggested that the ADS1115-Q1 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 16, the op amp should be set up to give a maximum output voltage no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1115-Q1 is 0.2V.



(1) Pull-down resistor to allow accurate swing to 0V.

(2) R_S is sized for a 50mV drop at full-scale current.

Figure 38. Low-Side Current Measurement

The ADS1115-Q1 are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1115-Q1 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1115-Q1 analog inputs can withstand momentary currents as large as 100mA.

If the ADS1115-Q1 are driven by an op amp with high-voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1115-Q1. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with an ADS1115-Q1, performance characteristics must be taken into account when designing the application.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS1115QDGSRQ1	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF ADS1115-Q1 :

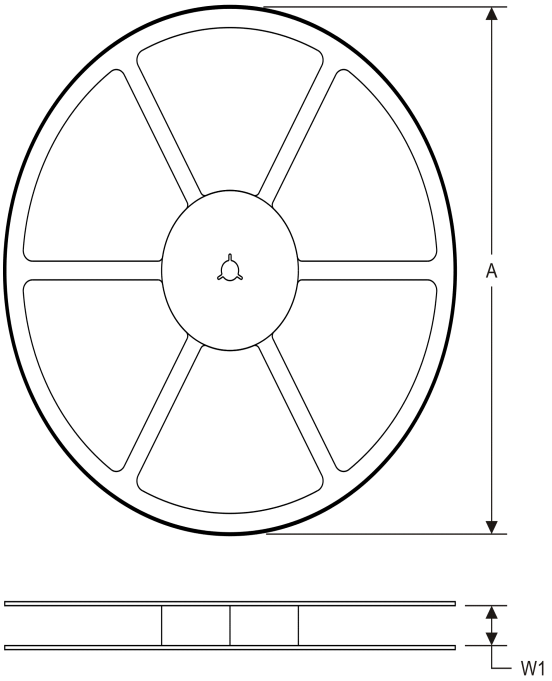
- Catalog: ADS1115

NOTE: Qualified Version Definitions:

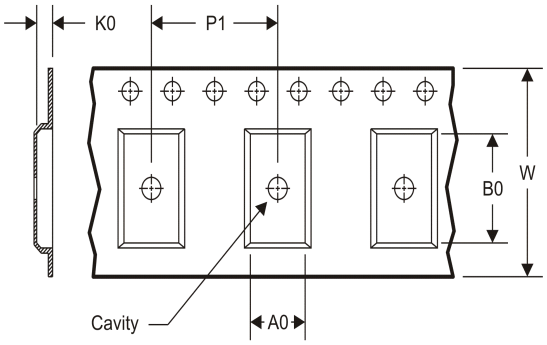
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



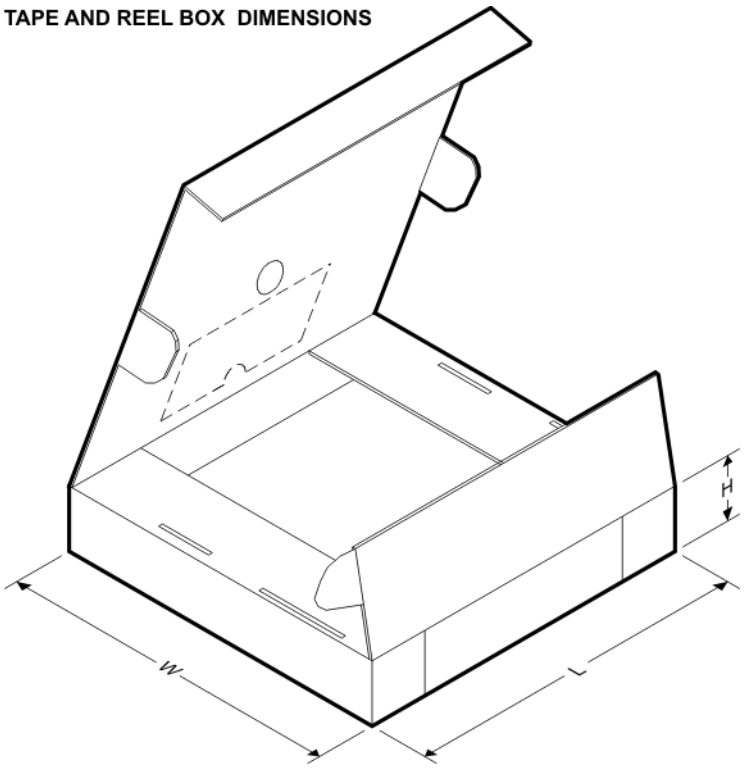
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1115QDGSRQ1	MSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

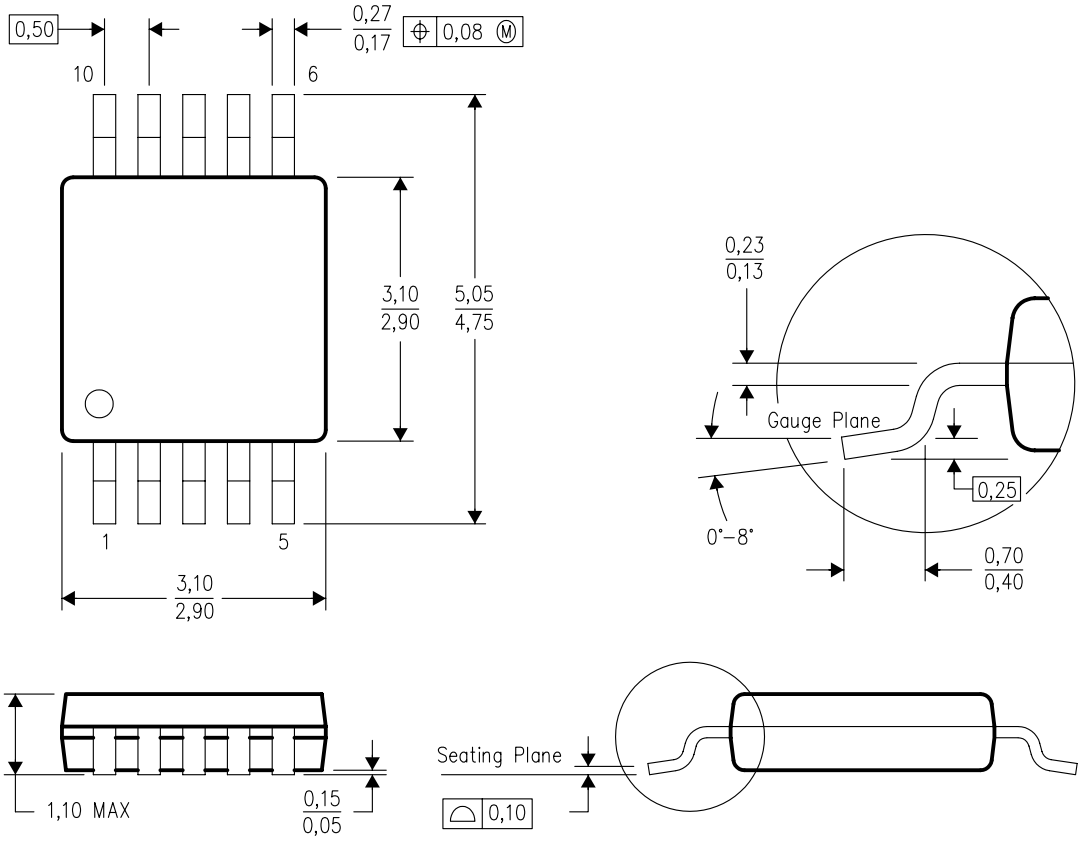
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1115QDGSRQ1	MSOP	DGS	10	2500	370.0	355.0	55.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
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