## **COP 3402 Systems Software**

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## **COP 3402 Systems Software**

Virtual Machines as instruction interpreters

## **Outline**

- 1. Virtual machines as software interpreters
- 2. P-code: instruction set architecture
- 3. The instruction format
- 4. Assembly language

## Virtual Machine: P-code

The Pseudo-code (P-code) is a virtual machine.

A virtual machine is a software implementation of an instruction set architecture.

P-code was implemented in the 70s to generate intermediate code for Pascal compilers.

Another example of a virtual machine is the JVM (Java Virtual Machine) whose intermediate language is commonly referred to as Java bytecode.

#### The P-machine Instruction format (PM/0)

The ISA of the PM/0 has 24 instructions and the instruction format has three components [OP, L, M]:

- **OP** is the operation code.
- indicates the lexicographical level.
- **M** depending of the opcode it indicates:
  - A number (instructions: LIT, INC).
  - A program address (instructions: JMP, JPC, CAL).
  - A data address (instructions: LOD, STO)
  - The identity of the operator OPR(i.e. OPR 0, 2 (ADD) or OPR 0, 4 (MUL)). 2 means ADD, 4 means MUL.

## Virtual Machine: P- code

The interpreter of the P-machine(PM/0) consists of a process address space(PAS), a memory area which consists of two segments:

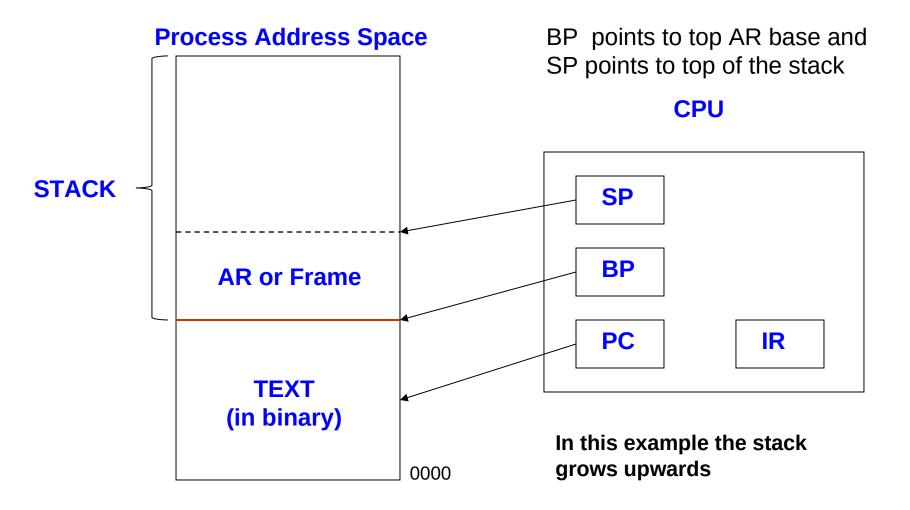
text	stack	PAS
A "text" segment	A segment called the "stack".	_

<sup>&</sup>quot;text" segment that contains the instructions.

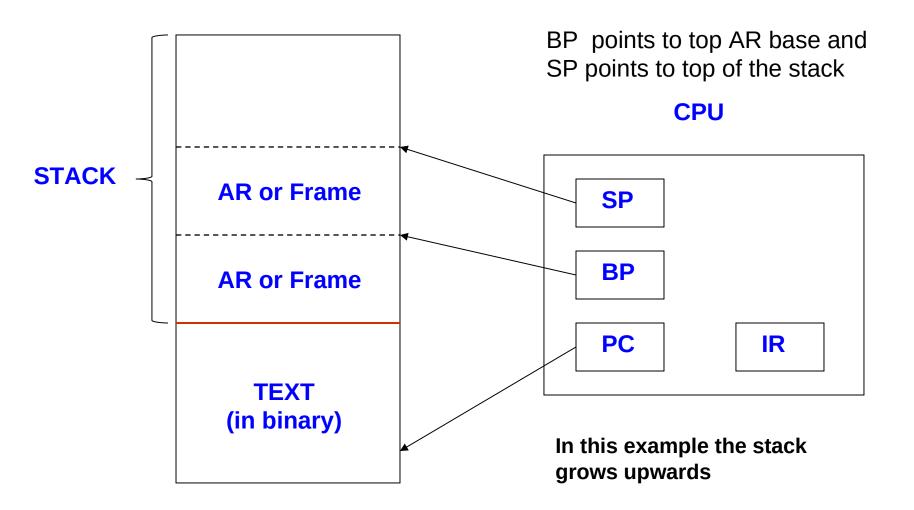
#### The CPU has four registers:

- -Base pointer **(bp)** which points to the base of the current **activation record (AR)** in the stack. (AR is also known as stack frame)
- -Stack pointer **(sp)** which points to the top of the stack
- Program counter or instruction pointer (pc), which points to the next instruction to be executed
- Instruction register (**ir**). Where instruction fetched from memory are placed into.

## Virtual Machine: P- code



## When a function is called a new AR is created for that function, and BP and SP are updated to point to the newly created AR.

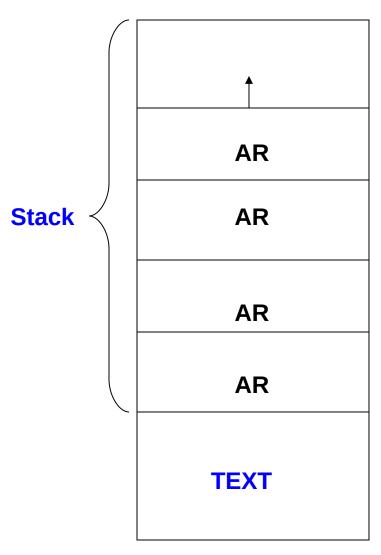


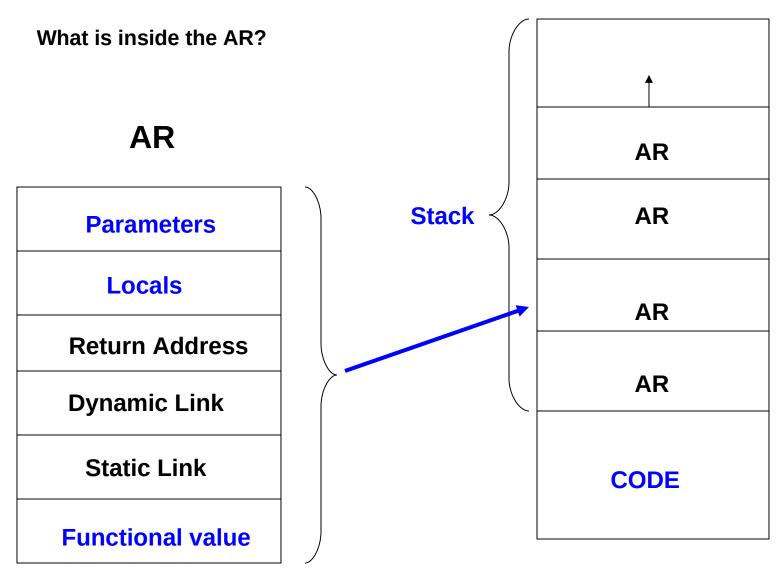
#### What is an activation record?

Activation record or stack frame is the name given to a data structure which is inserted in the stack, each time a procedure or function is called.

The data structure contains information to control sub-routine linkage when a program is in execution.

In the AR there is as well reserve space for local variables and parameters.





#### **Control Information:**

Return Address (RA): Points, in the text segment, to the next instruction to be executed in the calling function after termination of the current function or procedure.

**Dynamic Link (DL):** Points to the calling function stack frame base

Static Link (SL): Points to the stack frame of the procedure that statically encloses the current function or procedure. (More details will be presented shortly)

**DL** and **RA** restore the callers environment

#### AR

**Parameters** 

Locals

**Return Address** 

**Dynamic Link** 

**Static Link** 

**Functional value** 

**Functional value:** Location to store the function returned value.

**Parameters:** Space reserved to store the actual parameters of the function.

**Locals:** Space reserved to store local variables declared within the function or procedure.

Return Address: Points, in the code segment, to the next instruction (in the calling function) to be executed after termination of the current function or procedure.

**Dynamic Link:** Points to the base of the previous stack frame (AR = stack frame)

**Static Link:** Points to the stack frame of the procedure that statically encloses the current function or procedure

AR

**Parameters** 

Locals

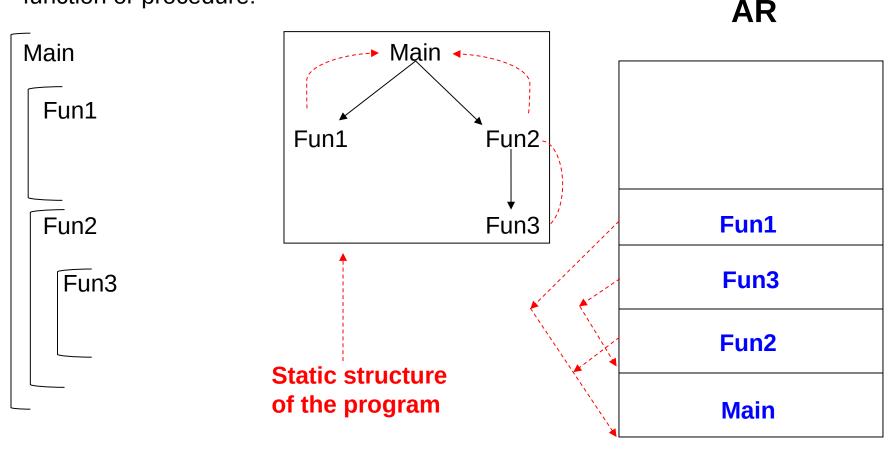
**Return Address** 

**Dynamic Link** 

**Static Link** 

**Functional value** 

**Static Link:** Points to the stack frame of the procedure that statically encloses the current function or procedure:



## Back to the P-machine!! Instruction cycle

The machine instruction cycle has two step known as fetch and execute.

#### Fetch step:

In the fetch step an instruction is fetch from the text segment (ir  $\leftarrow$  text[pc]) and the program counter is incremented by one (pc  $\leftarrow$  pc + ?).

```
FETCH

ir \leftarrow text[pc]

pc \leftarrow pc + ? ? = 1 or 2 or 3 or 4
```

#### **Execute step:**

In this step ir.op indicates the operation to be executed. In case ir.op = OPR then the field ir.m is used to identified the operator and execute the appropriate arithmetic or logical instruction

- 02 OPR (to be defined later, after the examples)
- $03 LOD L, M \rightarrow Push from location at offset M in stack frame L levels down.$
- 04 STO L, M → Store value on top of stack at offset M in stack frame L levels down.
- 05 CAL L, M  $\rightarrow$  Call procedure at M (generates new AR and pc = M).
- 06 INC 0, M  $\rightarrow$  Increment sp by M
- $07 JMP \quad 0, M \rightarrow pc = M$
- 08 JPC 0, M  $\rightarrow$  Jump to M if top of stack element is 0
- 09 SYS 0, 1 → Write the top stack element to the screen

  SYS 0, 2 → Read in input from the user and store it on top of the stack

  SYS 0, 3 → End of program (Set Halt flag to zero)

## P-machine ISA

We will show, with examples, how some instructions work

01 - LIT 0, M  $\rightarrow$  Push constant value (literal) M onto stack

03 – LOD L, M → Push from location at offset M in stack frame L levels down.

04 – STO L, M → Store top of stack at offset M in stack frame L levels down.

Pay attention to theses details: L = 0 in the examples for LOD and STO because a value will be loaded or stored in the current activation record (the active one).

We need to clarify this because eventually several ARs might be coexisting in the stack and the AR on top of the stack is current or active AR.

L!= 0 means that a value has to be LOD or STO in a different AR (when L!= 0, it is a **Natural** number)

AR or Frame (Current AR)

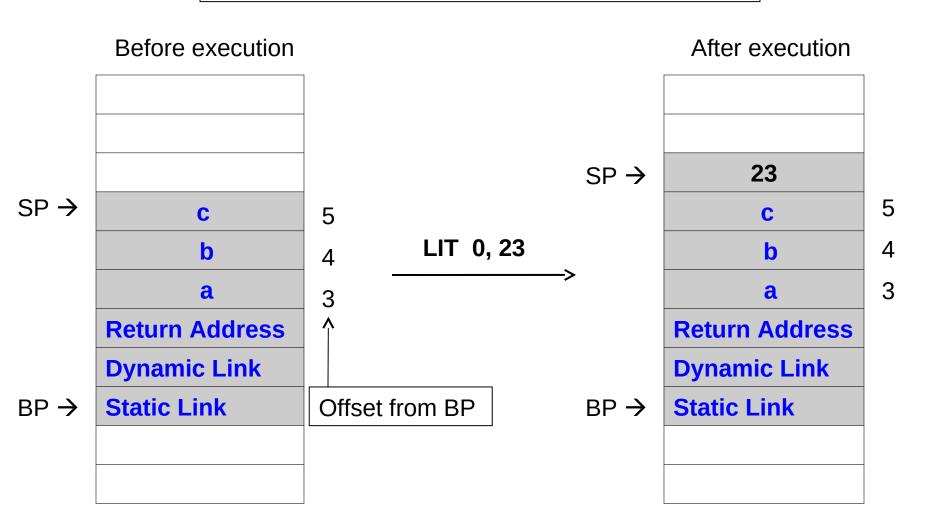
**AR or Frame** 

**AR or Frame** 

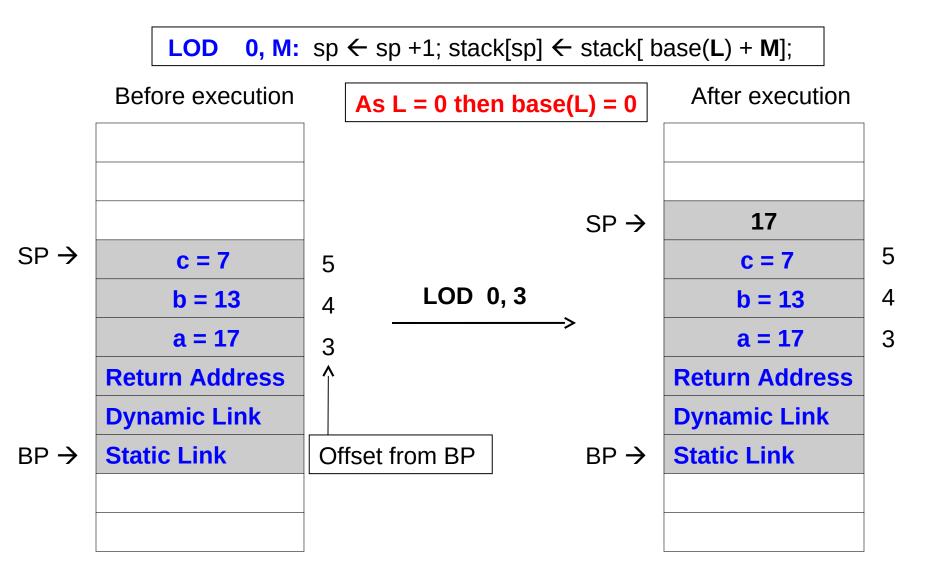
**AR or Frame** 

01-LIT 0, M  $\rightarrow$  Push constant value (literal) M onto stack

LIT 0, M steps: 
$$sp \leftarrow sp + 1$$
;  $stack[sp] \leftarrow M$ ;

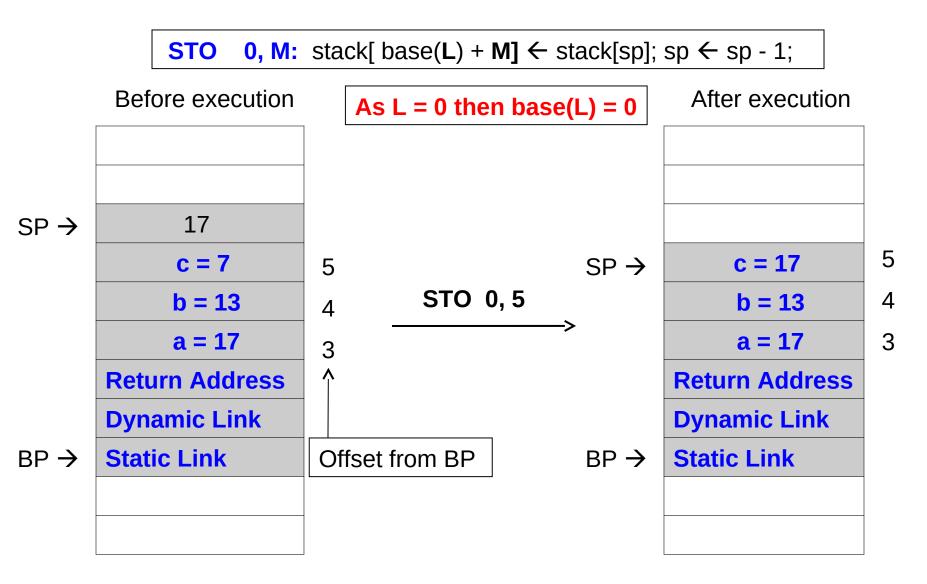


03-LOD 0, M  $\rightarrow$  Push from location at offset M in current AR



"base(L) is a function which locates the base of an ARs"

03- Store top of stack at offset **M** in current AR.



"base(L) is a function which locates the base of an ARs"

```
P-machine ISA
opcode
 02 - OPR:
             0.0 \rightarrow \text{Return operation} (i.e. return from subroutine)
 RTN
            0,1 \rightarrow NEG (-stack[sp])
 OPR
 OPR
            0,2 \rightarrow ADD (sp\leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] + stack[sp + 1])
 OPR
            0,3 \rightarrow SUB  (sp \leftarrow sp -1 and stack[sp] \leftarrow stack[sp] - stack[sp + 1])
 OPR
            0.4 \rightarrow MUL (sp \leftarrow sp - 1 \text{ and } stack[sp] \leftarrow stack[sp] * stack[sp + 1])
 OPR
            0.5 \rightarrow DIV  (sp\leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] div stack[sp + 1])
            0,6 \rightarrow ODD (stack[sp] \leftarrow stack mod 2) or ord(odd(stack[sp]))
 OPR
             0.7 \rightarrow MOD (sp \leftarrow sp -1 and stack[sp] \leftarrow stack[sp] mod stack[sp + 1])
 OPR
 OPR
            0.8 \rightarrow EQL  (sp \leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] = =stack[sp + 1])
 OPR
             0.9 \rightarrow NEO (sp \leftarrow sp - 1 \text{ and } stack[sp] \leftarrow stack[sp] != stack[sp + 1])
             0,10 \rightarrow LSS (sp \leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] < stack[sp + 1])
 OPR
             0,11 \rightarrow LEQ (sp \leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] <= stack[sp + 1])
 OPR
            0,12 \rightarrow GTR (sp \leftarrow sp -1 and stack[sp] \leftarrow stack[sp] > stack[sp +1])
 OPR
             0,13 \rightarrow GEQ (sp \leftarrow sp - 1 and stack[sp] \leftarrow stack[sp] >= stack[sp + 1])
 OPR
```

```
opcode
```

## P-machine ISA

```
01 - LIT 0, M \rightarrow sp \leftarrow sp +1;
                          stack[sp] \leftarrow M;
02 - RTN \quad 0, 0 \rightarrow sp \leftarrow bp -1;
                           cpu.pc \leftarrow stack[sp + 3]; // cpu.pc = RA
                           cpu.bp \leftarrow stack[sp + 2]; // cpu.bp = DL
03 - LOD L, M \rightarrow sp \leftarrow sp +1;
                           stack[sp] \leftarrow stack[base(L) + M];
```

$$04 - STO L, M \rightarrow stack[base(L) + M] \leftarrow stack[sp];$$
  
  $sp \leftarrow sp -1;$ 

"base(L) is a function which locates the base of an ARs"

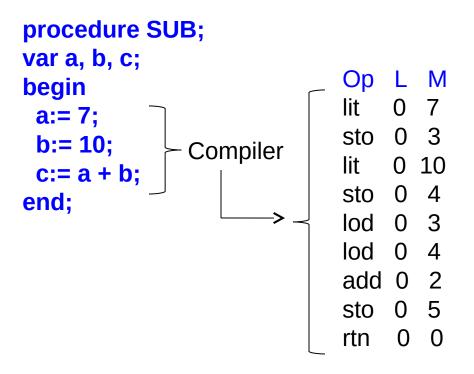
```
opcode
```

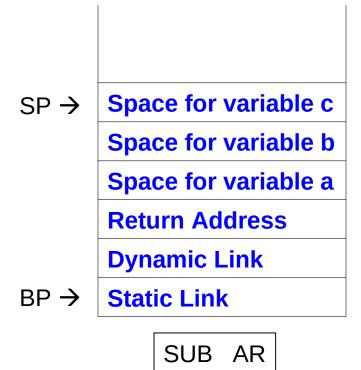
## P-machine ISA

/\* static link (SL)

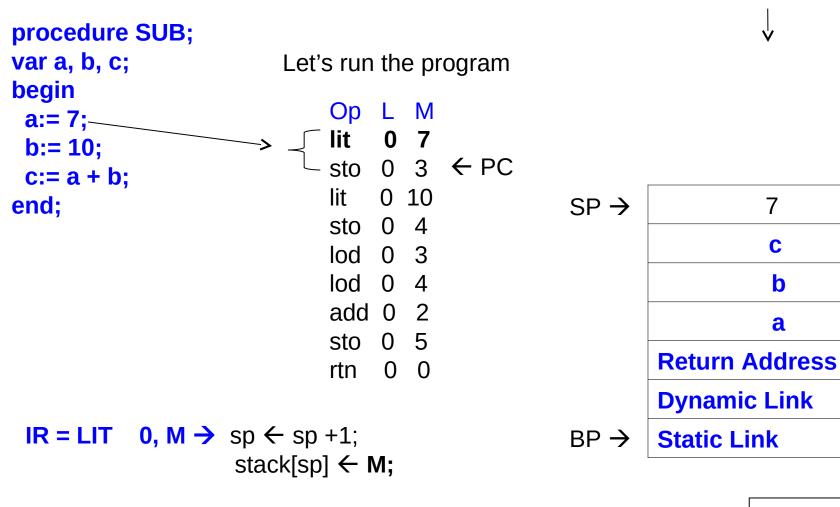
```
05 - CAL L, M \rightarrow stack[sp + 1] \leftarrow base(L);
                         stack[sp + 2] \leftarrow cpu.bp; /* dynamic link (DL)
                         stack[sp + 3] \leftarrow cpu.pc /* return address (RA)
                         bp \leftarrow sp + 1;
                         pc \leftarrow M;
06 - INC 0, M \rightarrow sp \leftarrow sp + M;
07 - JMP 0, M \rightarrow pc = M;
08 - \text{JPC } 0, M \rightarrow \text{ if stack[sp]} == 0 \text{ then } pc \leftarrow M;
                        sp \leftarrow sp - 1;
09 - WRT 0, 0 \rightarrow print (stack[sp]);
                         sp \leftarrow sp - 1;
```

Let us assume we have a function called SUB, and we are executing the instruction inside the function





#### Literal 7 loaded on top of stack.



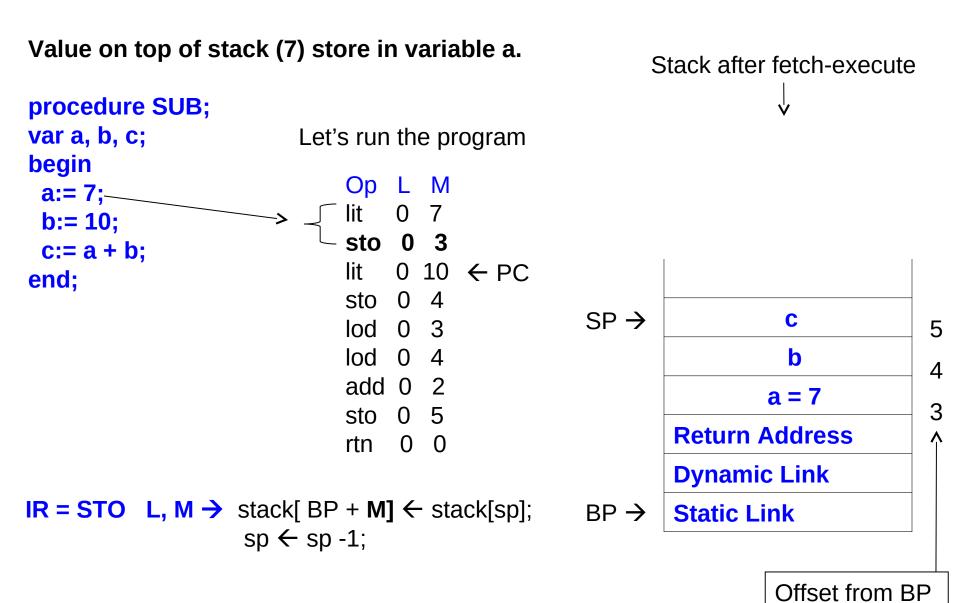
Offset from BP

5

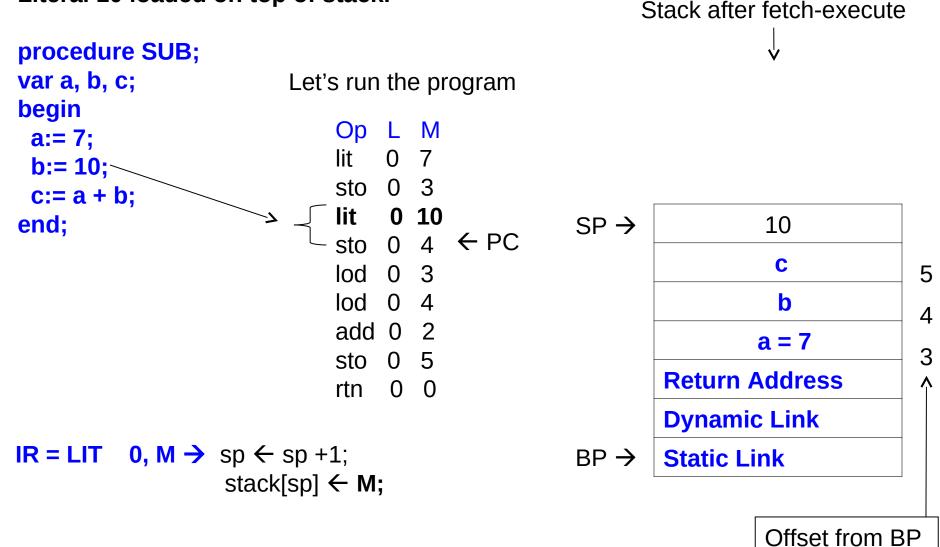
4

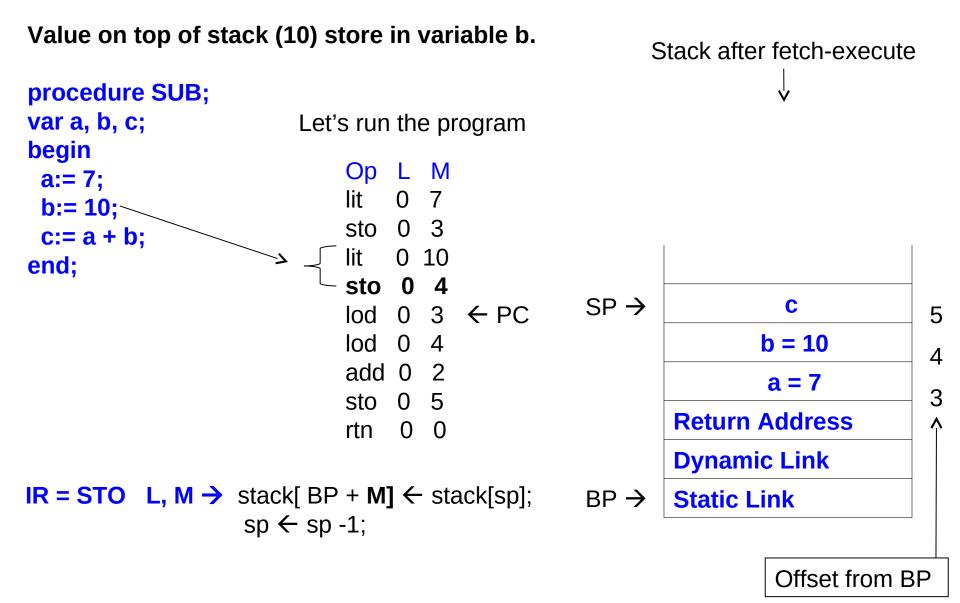
3

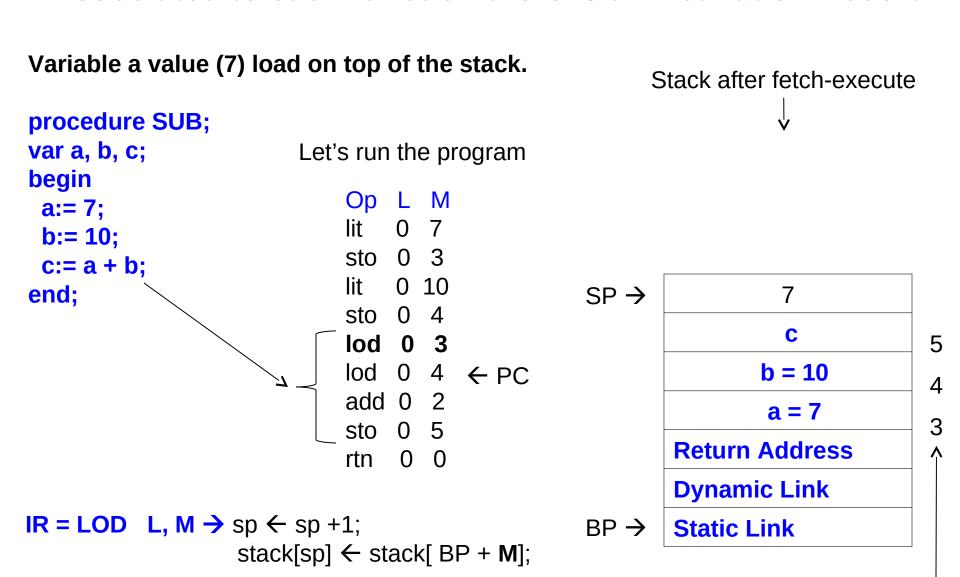
Stack after fetch-execute



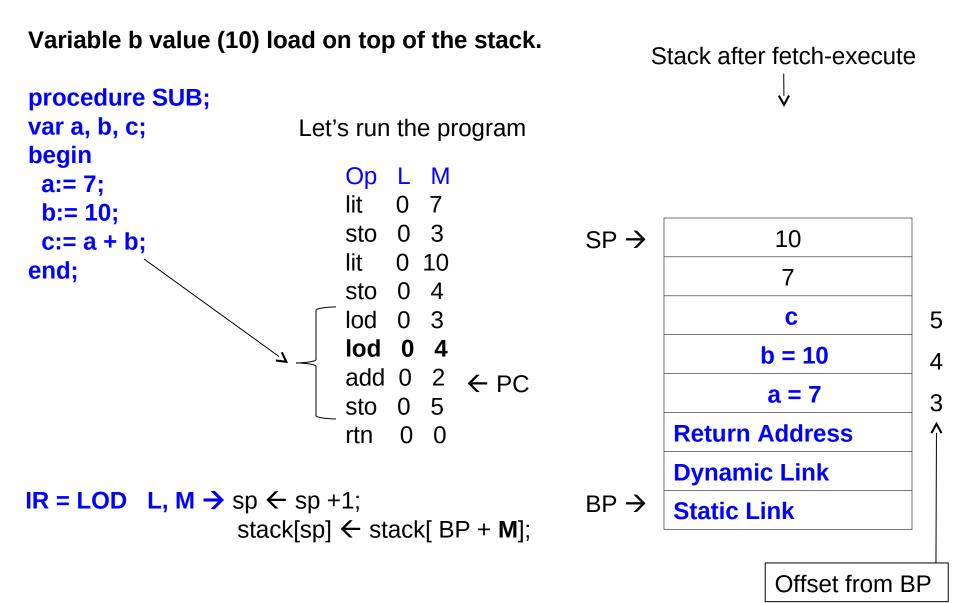
#### Literal 10 loaded on top of stack.

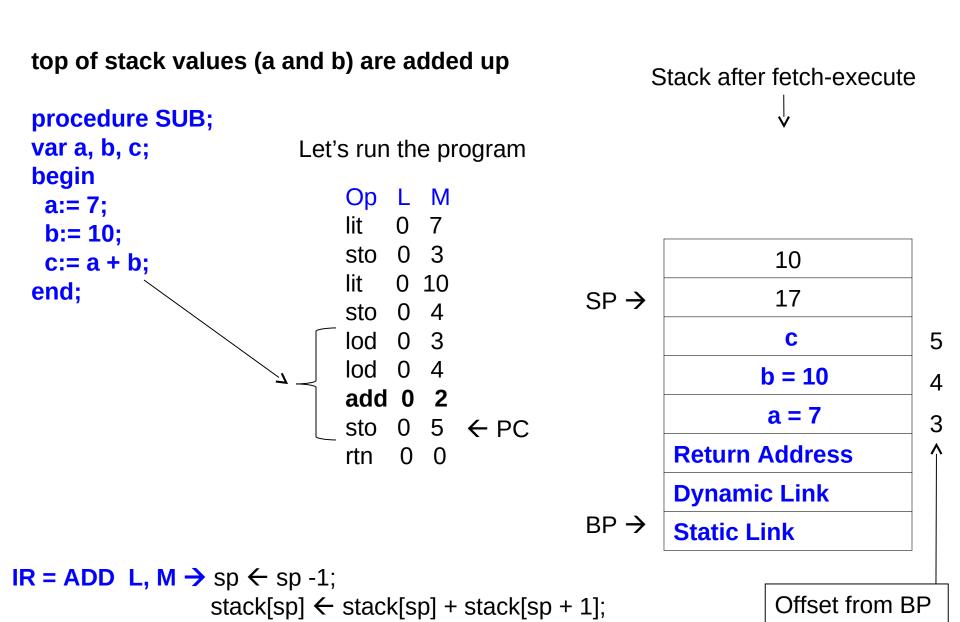






Offset from BP



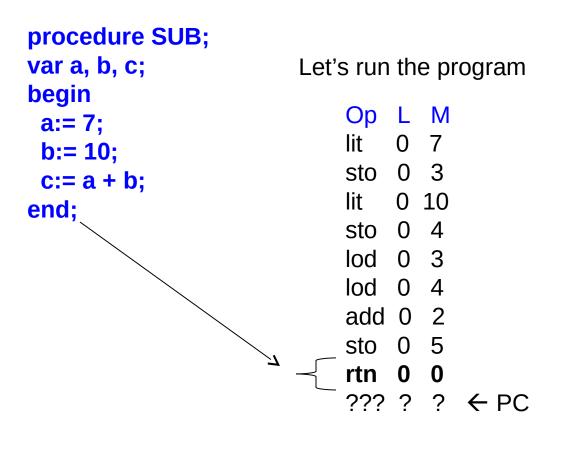


Top of stack value (17) is store in variable "c" Stack after fetch-execute procedure SUB; var a, b, c; Let's run the program begin M Op L a := 7;lit b:= 10; sto 0 3 10 c:= a + b;0 10 lit end; 17 sto 0 4  $SP \rightarrow$ c = 17lod 0 3 5 lod b = 104 add a = 73 sto 0 5  $0 \ 0 \leftarrow PC$ **Return Address** rtn **Dynamic Link**  $BP \rightarrow$ **Static Link**  $IR = STO L, M \rightarrow stack[BP + M] \leftarrow stack[sp];$ 

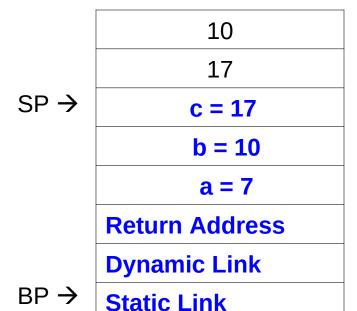
 $sp \leftarrow sp -1$ ;

Offset from BP

#### **Return from Subroutine (RTN)**



Stack after fetch-execute



 $IR = OPR \quad 0, 0 \rightarrow AR$  is deleted

Offset from BP

5

4

3

## P-machine: Code generation

In this example "functional value field" is not considered

#### **Programming example using PL/0**

#### P-code for the program on the left

```
0 jmp 0 10
                                                1 jmp 0 2
                   /* constant declaration
const n = 13;
                                                2 inc 0 5
var i,h;
                   /* variable declaration
procedure sub;
                                                3 lit 0 13
 const k = 7;
                                                4 sto 0 3
                                                5 lit 0 1
 var j,h;
                     /* procedure
 begin
                                                6 sto 13
                     /* declaration
  j:=n;
                                                7 lit 0 7
  i:=1;
                                                8 sto 0 4
  h:=k;
                                                9 opr 0 0
                                                10 inc 0 5
 end;
begin /* main starts here
                                                11 lit 0 3
 i:=3;
                                                12 sto 0 3
 h:=9;
                                                13 lit 0 9
 call sub;
                                                14 sto 0 4
                                                15 cal 0 2
end.
                                                16 opr 0 0
```

## Running a program on PM/0

		рс	bp	sp	stack	code	9
Initial v	alues	0	1	0	00000	0 jmp	0 10
						1 jmp	02
0 jmp	0, 10	10	1	0	00000	2 inc	0 5
10 inc	0, 5	11	1	5	00000	3 lit	0 13
11 lit	0, 3	12	1	6	000003	4 sto	0 3
12 sto	0, 3	13	1	5	00030	5 lit	0 1
13 lit	0, 9	14	1	6	000309	6 sto	13
14 sto	0, 4	15	1	5	00039	7 lit	0 7
15 cal	0, 2	2	6	5	00039 1116	8 sto	0 4
2 inc	0, 5	3	6	10	00039 111600	9 opr	0 0
3 lit	0, 13	4	6	11	0003911160013	10 inc	0 5
4 sto	0, 3	5	6	10	00039 1116130	11 lit	03
5 lit	0, 1	6	6	11	00039 11161301	12 sto	0 3
6 sto	1, 3	7	6	10	0 0 0 1 9 1 1 16 13 0	13 lit	0 9
7 lit	0, 7	8	6	11	00019 11161307	14 sto	0 4
8 sto	0, 4	9	6	10	0 0 0 1 9 1 1 16 13 7	15 cal	0 2
9 opr	0, 0	16	1	5	00019	16 sio	0 3

#### **The P-machine (Register Version)**

The ISA of the PM/0 (register version) has 22 instructions, a register file, and the instruction format has four components  $\langle op, r, l, m \rangle$ :

- **OP** is the operation code
- R Refers to a register.
- L indicates the lexicographical level or a register in arithmetic and relational instructions. (L or R)
- **M** depending of the operators it indicates:
  - A number (instructions: LIT, INC).
  - A program address (instructions: JMP, JPC, CAL).
  - A data address (instructions: LOD, STO)
  - A register in arithmetic and logic instructions. (e.g. ADD R[1], R[2], R[3]  $\rightarrow$  R[1] = R[2] + R[3])

#### **Instruction Set Architecture (ISA)**

There are 13 arithmetic/logical operations that manipulate the data within the register file. These operations will be explained after the 11 basic instructions of PM/0.

ISA: 01 - LIT	R, 0, M	Loads a constant value (literal) <b>M</b> into Register <b>R</b>
02 - <b>RTN</b>	O, <b>0, 0</b>	Returns from a subroutine and restore the caller environment
03 - <b>LOD</b>	R, L, M	Load value into a selected register from the stack location at offset ${\bf M}$ from ${\bf L}$ lexicographical levels down
04 - <b>STO</b>	R, <b>L, M</b>	Store value from a selected register in the stack location at offset ${\bf M}$ from ${\bf L}$ lexicographical levels down
05 - <b>CAL</b>	0, L, M	Call procedure at address $\mathbf{M}$ (generates new Activation Record and pc $\leftarrow \mathbf{M}$ )
06 - <b>INC</b>	0, 0, M	Allocate M words (increment sp by M). First four are Functional Value, Static Link (SL), Dynamic Link (DL), and Return Address (RA)
07 - <b>JMP</b>	0, 0, M	Jump to instruction M
08 - <b>JPC</b>	R, 0, M	Jump to instruction $\mathbf{M}$ if $\mathbf{R} = 0$
09 – <b>SIO</b>	R, <b>0, 1</b>	Write a register contents to the screen
10 <b>- SIO</b>	R, 0, 2	Read in a value from the user program and store it in a register
11- SIO	0, 0, 3	End of program (program stops running and call the OS)

#### **ISA Pseudo Code**

```
01 - LIT R, 0, M
                              R[i] \leftarrow M;
02 - RTN 0, 0, 0
                               sp \leftarrow bp - 1;
                               bp \leftarrow stack[sp + 3];
                               pc \leftarrow stack[sp + 4];
03 – LOD R, L, M
                               R[i] \leftarrow stack[base(L, bp) + M];
                               stack[base(L, bp) + M] \leftarrow R[i];
04 – STO R, L, M
05 - CAL 0, L, M
                               stack[sp + 1] \leftarrow 0;
                                                                             /* space to return value
                               stack[sp + 2] \leftarrow base(L, bp);
                                                                             /* static link (SL)
                               stack[sp + 3] \leftarrow bp;
                                                                             /* dynamic link (DL)
                                                                             /* return address (RA)
                               stack[sp + 4] \leftarrow pc;
                               bp \leftarrow sp + 1;
                               pc \leftarrow M;
06 - INC 0, 0, M
                               sp \leftarrow sp + M;
07 - JMP 0, 0, M
                              pc \leftarrow M;
08 - JPC R, 0, M
                               if R[i] == 0 then { pc \leftarrow M; }
09 - SIO R, 0, 1
                               print(R[i]);
10 - SIO R, 0, 2
                               read(R[i]);
11 - SIO R, 0, 3
                               Set Halt flag to zero, assuming that Halt = 1 controls the Fetch-execute loop; (End of
                               program)
```

#### ISA Pseudo Code (arithmetic and relational instructions)

12 - **NEG** (R[i] 
$$\leftarrow$$
 -R[i])

13 - **ADD** 
$$(R[i] \leftarrow R[j] + R[k])$$

14 - **SUB** (R[i] 
$$\leftarrow$$
 R[j] - R[k])

15 - **MUL** 
$$(R[i] \leftarrow R[j] * R[k])$$

16 - **DIV** 
$$(R[i] \leftarrow R[j] / R[k])$$

17 - **ODD** (R[i] 
$$\leftarrow$$
 R[i] mod 2) or ord(odd(R[i]))

18 - **MOD** (R[i] 
$$\leftarrow$$
 R[j] mod R[k])

19 - **EQL** 
$$(R[i] \leftarrow R[j] = = R[k])$$

20 - **NEQ** 
$$(R[i] \leftarrow R[j] != R[k])$$

21 - LSS 
$$(R[i] \leftarrow R[j] < R[k])$$

22 - **LEQ** 
$$(R[i] \leftarrow R[j] \leq R[k])$$

23 - **GTR** 
$$(R[i] \leftarrow R[j] > R[k])$$

24 - **GEQ** 
$$(R[i] \leftarrow R[j] >= R[k])$$

## P-machine: Code generation (Regs)

#### **Programming example using PL/0**

```
const n = 13; /* constant declaration
var i,h;
                  /* variable declaration
procedure sub; -
 const k = 7;
 var j,h;
 begin
                     /* procedure
  j:=n;
                     I* declaration
  i:=1;
  h:=k;
 end;
begin /* main starts here
 i:=3;
 h:=9;
 call sub;
end.
```

#### P-code for the program on the left

```
0 jmp 0 0 10
1 jmp 002
2 inc 006
3 lit 0 0 13
4 sto 0 0 4
5 lit 0 0 1
6 sto 0 1 4
7 lit 0 0 7
8 sto 005
9 opr 000
10 inc 006
11 lit 0 0 3
12 sto 0 0 4
13 lit 0 0 9
14 sto 005
15 cal 0 0 2
16 sio 003
```

## **Program on PM/0 with registers**

		рс	bp	sp	stack	code
Initial v	alues	0	1	0	00000	0 jmp 0 0 10
						1 jmp 002
0 jmp	0, 0, 10	10	1	0	00000	2 inc 006
10 inc	0, 0, 6	11	1	6	00000	3 lit 0 0 13
11 lit	0, 0, 3	12	1	6	00000	4 sto 0 0 4
R0 = 3, $R1 = 0$ , $R2 = 0$ , etc.					5 lit 001	
12 sto	0, 0, 4	13	1	6	00003	6 sto 014
13 lit	0, 0, 9	14	1	6	00003	7 lit 007
14 sto	0, 0, 5	15	1	6	000039	8 sto 005
15 cal	0, 0, 2	2	7	6	000039	9 opr 000
2 inc	0, 0, 6	3	7	12	00003901116	10 inc 006
3 lit	0, 0, 13	4	7	12	00003901116	11 lit 003
4 sto	0, 0, 4	5	7	12	0000390111613	12 sto 0 0 4
5 lit	0, 0, 1	6	7	12	0000390111613	13 lit 0 0 9
6 sto	0, 1, 4	7	7	12	0000190111613	14 sto 0 0 5
7 lit	0, 0, 7	8	7	12	0000190111613	15 cal 0 0 2
8 sto	0, 0, 5	9	7	12	0000190111613	716 sio 003
9 rtn	0, 0, 0	16	1	6	000019	
16sio	0, 0, 3	17	1	6	000019	

## **COP 3402 Systems Software**

Virtual Machines
as instruction
interpreters
(The End)