DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f11-07-2017)

Year: II/IV Semester: I Room No: IT- 211 Section: A

Day	9:30-10:30	10:30-11:30	BREAK	11:40-12:40	12:40-1:40	LUNCH	2:15-3:15	3:15-4:15
Mon	PRP (DBVR)	ME (CHS)		DM (KRM)	DELD (MK)		DS (TM)	
Tue	BE LAB(Batch-A)/MP-I LAB(Batch-B) (CHS,MK),(BP)/ (KRM,SCHVB,GUS),(AN)			ENS (KS)	DELD (MK)		DS (TM)	
Wed	ME (CHS)	PRP (DBVR)		PRP (DBVR)	DS (TM)		ENS (KS)	DM (KRM)
Thu	PRP (DBVR)	DELD (MK)		DS LAB(Batch-B)/MP-I LAB(Batch-A) (TM,GUS),(SKC)/(KRM,THS),(BK)			ME (CHS)	
Fri	DS LAB(Batch-A)/ BE LAB(Batch-B) (TM,KRM),(SKC)/(CHS,MK)(BP)			DM (KRM)			DELD (MK)	ENS (KS)

LEGEND:

Sub Code	Name of the Subject	Faculty Name
DM	Discrete Mathematics (PC 201 IT)	K. Ramya Madhavi
ME	Micro Electronics (PC 202 IT)	Ch. Srujana
DELD	Digital Electronics and Logic Design (PC 203 IT)	M. Kavitha
DS	Data Structures (PC 204 IT)	T. Mrunalini
PRP	Probability & Random process (PC 205 IT)	DBV. Ravi Sankar
ENS	Environmental Studies (HS 222 MC)	K.Shweta
DS LAB	Data Structures Lab (PC 231 IT)	T. Mrunalini,K.Ramya Madhavi(Batch-A),G.Ushasri(Batch-B), S.kalyan Chakravarthy
BE LAB	Basic Electronics Lab (PC 232 IT)	Ch.Srujana,M.Kavitha, B.Prasad (Batch-A&B)
MP-IILAB	Mini Project-I Lab (PC 233 IT)	K.Ramya Madhavi, S.Ch.Vijaya Bhaskar (Batch-A),G.Ushasri(Batch-A), T.Hari Singh, (Batch-B), A.Nirmala (Batch-B), B.Karunakar(Batch-B)

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL

DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f11-07-2017)

Year: II/IV Semester: I Room No: IT- 210 Section: B

Day	9:30-10:30	10:30-11:30	11:30-11:40BREAK	11:40-12:40	12:40-1:40	1:40- 2:15LUNCH	2:15-3:15	3:15-4:15
Mon	DM (PK)	DELD (MK)		DS (PAB)			PRP (DBVR)	ME (AVV)
Tue	ENS (STM)	PRP (DBVR)		DS LAB(Batch-A/MP-I LAB(Batch-B) (PAB,GUS),(SKC)/(THS,TM), (BP)			ME (AVV)	
Wed	ENS (STM)	DELD (MK)		DELD (MK)	ME (AVV)		DS (PAB)	PRP (DBVR)
Thu	DS LAB(Batch-B/BE LAB(Batch-A) (PAB,PK),(SKC)/(AVV,TM),(BP)			ME (AVV)	DS (PAB)		PRP (DBVR)	DM (PK)
Fri	DM (PK)			ENS (STM)	DELD (MK)		BE LAB(Batch-B)/MP-I LAB(Batch-A) (AVV,TM),(BP)/(THS,PK)(BK)	

LEGEND:

Sub Code	Name of the Subject	Faculty Name
DM	Discrete Mathematics (PC 201 IT)	P.Karthik
ME	Micro Electronics (PC 202 IT)	A.V.Vahini
DELD	Digital Electronics and Logic Design (PC 203 IT)	M.Kavitha
DS	Data Structures (PC 204 IT)	P.Amba Bhavani
PRP	Probability & Random process (PC 205 IT)	DBV.Ravi Sankar
ENS	Environmental Studies (HS 222 MC)	Shilpa Tiwari Mishra
DS LAB	Data Structures Lab (PC 231 IT)	P.Amba Bhavani,G.Ushasri(Batch-A),P.Karthik(Batch-B), S.kalyan Chakravarthy
BE LAB	Basic Electronics Lab (PC 232 IT)	A.V.Vahni, T.Mrunalini,B.Prasad
MP-1LAB	Mini Project-I Lab (PC 233 IT)	T.Hari Singh,P.Karthik (Batch-A),T.Mrunalini(Batch-B), B.Karunakar(Batch-A),B.Prasad (Batch-B)

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL

DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f11-07-2017)

Year: III/IV Semester: I Room No: IT - 119 Section: A

Day	9:45-10:35	10:35-11:25	11:25-12:15	12:15-1:00	1:00 - 1:45LUNCH	1:45-2:35	2:35-3:25	3:25-4:15
Mon	SE (AM)	DBMS LAB(Batch-A)/MP-III LAB(Batch-B) (DK,AM),(BK)/(KSL,AVV),(BU)				DBMS (DK)	DAA (GUS)	
Tue	TOC (JS)	SE (AM)	MEA (CHVR)	OS (KRM)		DBMS LAB(Batch-B)/OS LAB(Batch-A) (DK,AM),(BK)/(KRM,DM),(BU)		
Wed	DBMS (DK)	OS LAB(Batch-B)/MP-III LAB(Batch-A) (KRM,PAB)(BU)/(KSL,AM,GUS),(AN)				OS (KRM)		
Thu	DBMS (DK)		SE (AM)	MEA (CHVR)		TOC (JS)	OS (KRM)	
Fri	MEA (CHVR)		TOC (JS)			SE (AM)	DAA (GUS)	

LEGEND:

Sub Code	Name of the Subject	Faculty Name
MEA	Managerial Economics and Accountancy(CM371)	Ch Venkat Rao
SE	Software Engineering (BIT302)	A.Manasa
DAA	Design and Analysis of Algorithms (BIT303)	G.Ushasri
DBMS	Database Management Systems(BIT304)	K.Devaki
OS	Operating Systems (BIT305)	K.Ramya Madhavi
TOC	Theory of Computation (BIT306)	J.Sowjanya
OS LAB	Operating SystemsLab (BIT 331)	K.Ramya Madhavi,D.Muninder(Batch-A),P.Amba Bhavani (Batch-B),B.Uma Rani
DBMS LAB	DBMS Lab (BIT 332)	K.Devaki,T. Mrunalini, A. Manasa,B.Karunakar
MP-III LAB	Mini Project-III Lab(BIT 333)	K.Srilaxmi,A.Manasa(Batch-A),G.Ushasri(Batch-A),A.V.Vahini(Batch-B), A.Nirmala(Batch-A),B.Uma Rani (Batch-B)

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL

DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f 11-07-2017)

Year: III/IV Semester: I Room No: IT - 118 Section: B

Day	9:45-10:35	10:35-11:25	11:25-12:15	12:15-1:00	1:00 - 1:45LUNCH	1:45-2:35	2:35-3:25	3:25-4:15
Mon	DBMS (JS)		DAA (KN)			DBMS LAB(Batch-A/MP-III LAB(Batch-B) (JS,PK),(BK)/(DM,AM,MK),(BU)		
Tue	MEA (NS)	DBMS LAB(Batch-B)/OS LAB(Batch-A) (JS,PK),(BK)/(KSL,DM),(BU)				OS (KSL)	SE (PK)	
Wed	SE (PK)	MEA (NS)	TOC (VAK)			OS (KSL)		
Thu	OS (KSL)		DBMS (JS)	SE (PK)		DAA (KN)	TOC (VAK)	
Fri	DAA (KN)	OS LAB(Batch-B)/MP-III LAB(Batch-A) (KSL,PAB),(BU)/(DM,AM),(AN)				DBMS (JS)	MEA (NS)	

LEGEND:

Sub Code	Name of the Subject	Faculty Name
MEA	Managerial Economics and Accountancy (CM-371)	N.Sanju
SE	Software Engineering (BIT-302)	P.Karthik
DAA	Design and Analysis of Algorithms (BIT-303)	Dr.K.Nikitha
DBMS	Database Management Systems(BIT-304)	J.Sowjanya
OS	Operating Systems (BIT-305)	K.Srilaxmi
TOC	Theory of Computation(BIT-306)	V.Ashwini Kumar
OS LAB	Operating Systems Lab(BIT 331)	K.Srilaxmi, D.Muninder (Batch-A),P.Amba Bhavani(Batch-B)
DBMS LAB	DBMS Lab (BIT 332)	J.Sowjanya, P.Karthik, B.Karunakar
MP-III LAB	Mini Project-III Lab (BIT 333)	D.Muninder, A.Manasa, M.Kavitha(Batch-B) A.Nirmala, B. Uma Rani

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL

DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f 11 -07-2017)

Year: IV/IV Semester: I Room No: IT-117 Section: A

	9:45-10:35	10:35-11:25	11:25-12:15	12:15-1:00	1:00 - 1:45LUNCH	1:45-2:35	2:35-3:25	3:25-4:15
Mon	IS (DM)	MWT LAB(Batch-A)/VLSI LAB(Batch-B) (KCS,THS,GUS),(SKC)/(SCHVB,DBVR), (AN,BP)				MWT (KCS)		
Tue	SRT/SW (DK/THS)		WMC/IPR (AVV/VAK)			MWT LAB(Batch-B)/PS(Batch-A) (KCS,THS,GUS),(SKC)/(KN,CS,VAK,MK),(BP)		
Wed	IS (DM)		VLSI (SCHVB)			MWT (KCS)	WMC/IPR (AVV/VAK)	
Thu	IS (DM)	VLSI LAB(Batch-A)/PS(Batch-B) (SCHVB,DBVR),(AN)/(KN,CS,VAK,DM), (BK)				MWT (KCS)		
Fri	VLSI (SCHVB)		SRT/SW (DK/THS)					

LEGEND:

Sub Code	Name of the Subject	Faculty Name
VLSI	VLSI Design (BIT401)	S.Ch.Vijaya Bhaskar
MWT	Middleware Technologies (BIT402)	K.Chandra Sekhar
IS	Information Security (BIT403)	D.Muninder
WMC (ELEC-II)	Wireless and Mobile Communications(BIT404)	A.V.Vahini
IPR (ELEC-II)	Intellectual Property Rights (LA473)	V.Ashwini Kumar
SemWeb (ELEC-III)	Semantic Web (BIT 4)	T.Hari Singh
SRT (ELEC-III)	Software Reuse Techniques (BIT 411)	K.Devaki
VLSI LAB	VLSI Design Lab(BIT 431)	S.Ch.Vijaya Bhaskar, DBV. Ravi Sankar,A.Nirmala,B.Prasad
MWT LAB	Middleware Technologies Lab (BIT 432)	K.Chandra Sekhar,T.Harisingh,G.Ushasri,S.Kalyana Chakravarthy
PS	Project Seminar (BIT433)	Dr.K.Nikitha,Dr.Ch.Samson,V.Ashwini Kumar,M.Kavitha(Batch-A), D.Muninder(Batch-B), B.Karunakar(Batch-B), B.Prasad(Batch-A)

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL

DEPT OF INFORMATION TECHNOLOGY
M.V.S.R. Engineering College, Nadergul, Hyderabad
Time Table for the Academic Year 2017-2018(w.e.f 11 -07-2017)

Year: IV/IV Semester: I Room No: IT- 209 Section: B

Day	9:45-10:35	10:35-11:25	11:25-12:15	12:15-1:00	1:00 - 1:45LUNCH	1:45-2:35	2:35-3:25	3:25-4:15
Mon			IS (CS)			VLSI LAB(Batch-A)/PS(Batch-B) (SCHVB,CHS),(AN)/(KN,CS,THS,PAB),(BP)		
Tue	SRT/SW (DK/THS)		WMC/IPR (AVV/VAK)			VLSI (CHS)		
Wed	MWT LAB(Batch-B)/ PS(Batch-A) (KCS,JS),(SKC)/(KN,CS,AVV,TM),(BK)			MWT (KCS)		VLSI (CHS)	WMC/IPR (AVV/VAK)	
Thu	VLSI (CHS)	MWT (KCS)		IS (CS)				
Fri	MWT (KCS)	IS (CS)	SRT/SW (DK/THS)			MWT LAB(Batch-A)/VLSI LAB(Batch-B) (KCS,DK),(SKC)/(SCHVB,CHS),(AN)		

LEGEND:

Sub Code	Name of the Subject	Faculty Name
VLSI	VLSI Design (BIT 401)	Ch. Srujana
MWT	Middleware Technologies (BIT 402)	K.Chandra Sekhar
IS	Information Security (BIT 403)	Ch.Samson
WMC (ELEC-II)	Wireless and Mobile Communications(BIT 404)	A.Vijaya Vahini
IPR (ELEC-II)	Intellectual Property Rights (LA473)	V.Ashwini Kumar
SemWeb (ELEC-III)	Semantic Web (BIT 4)	T.Hari Singh
SRT (ELEC-III)	Software Reuse Techniques (BIT 411)	K.Devaki
VLSI LAB	VLSI Design Lab(BIT 431)	S.Ch.Vijaya Bhaskar,Ch.Srujana,A.Nirmala
MWT LAB	Middleware Technologies Lab (BIT 432)	K.Chandra Sekhar, J.Sowjanya,S.Kalyan Chakravarthy
PS	Project Seminar (BIT 433)	K.Nikitha,Sh.Samson, A.Vijaya Vahini, T.Mrunalini(Batch-A), P.Amba Bhavani(Batch-B), B.Karunakar(Batch-A), B.Prasad(Batch-B)

TIME-TABLE CO-ORDINATOR (Dept) TIME-TABLE CO-ORDINATOR (College) HOD PRINCIPAL