Nome -> Newwy kumor Grupta MCA 1(B) Emollment no. -> PV-21010128. Student 10 -> 21711080

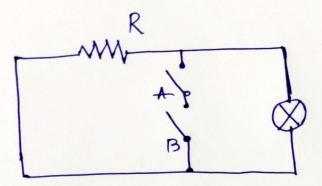
## COA Mid term Practical.

Quel

A NANDgate is a logic gate that produces a low output (0) only if all its inpute accelerate, and high output (1) otherwise. Hence the NAND gate is the atherwise inverse of on AND gate, and its circuit is produced by connecting and AND gate to a NOT gate.

The NAND gate performs the logical NAND operation. NAND gates are known as universal gates (along with NOR gates)

## Circuit Diagram of MAND Diagram



Lomp DEFZ 2'0'

Switch A - Open = '0', Closed = '1'
Switch B - Open = '0', Closed = '1'