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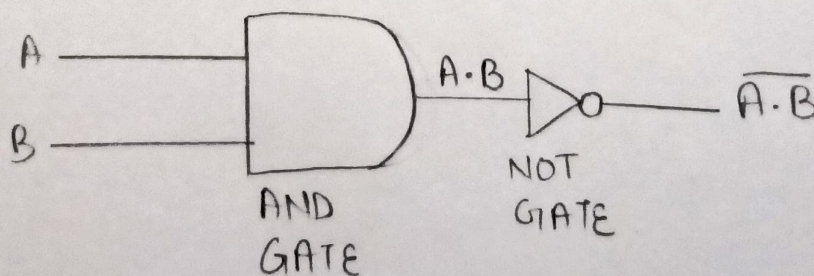
Subject:- Computer Organisation and Architecture

Ans1. A NAND gate ("not AND gate") is a logic gate that produces a low output 0 only if all its inputs are true, and high output 1 otherwise. Hence the NAND gate is inverse of an AND gate, and its circuit produced by connecting an AND gate to a NOT gate.

Just like an AND gate, a NAND gate may have any number of input probes but only one output probe.

The NAND gate perform the logical NAND operation. NAND gates are known as universal gates, which means it is a logic gate which can implement any Boolean function without the need to use any other gate type.

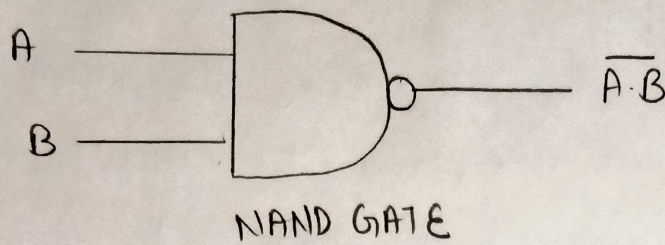
The basic logical construction of the NAND gate is:-



Circuit diagram of NAND



There are two input A and B after passing AND logic gate ② is produced an output  $A \cdot B$  then it is pass through NOT gate then it produced an output  $\overline{A \cdot B}$ .  
OR we can make NAND gate by second method that is:-



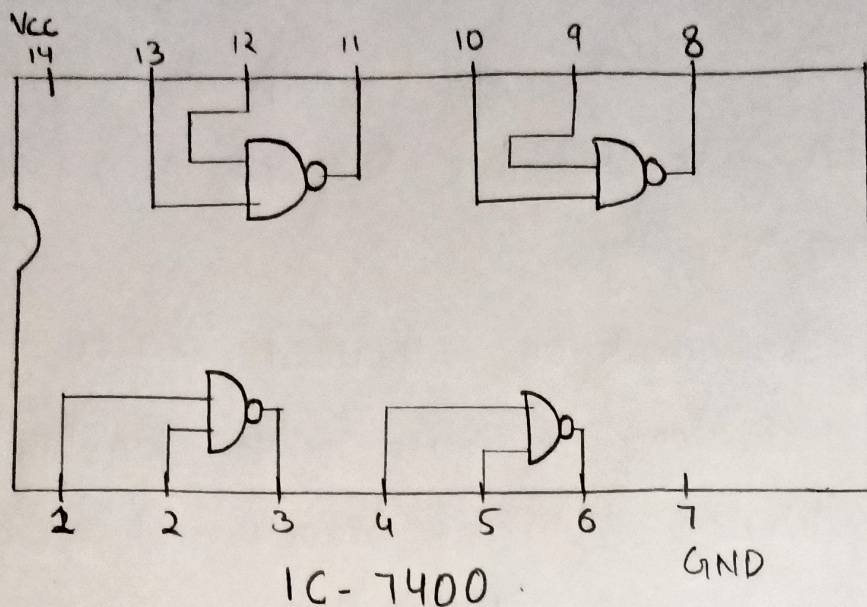
### TRUTH TABLE

Inputs		Output
A	B	$x = A \cdot B$
0	0	1
0	1	1
1	0	1
1	1	0

OR

INPUT		OUTPUT	
A	B	$A \cdot B$	$\overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0





$$Y = \overline{A \cdot B}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

In this circuit input is given or pass through the NAND Gate and produce output that store onto next pin. PIN 7 is grounded and pin 14 is Vcc.

We Can Also pass three input to a NAND Gate. Then there are 3 input A, B, C. Then output will be  $\overline{A \cdot B \cdot C}$ .



This is a two-input NAND gate IC that has 14 pins. The IC consists of 4 independent gates where each gate perform Negated AND logic gate functionality.

These gates work on Advanced silicon gate CMOS technology to gain higher functional speed utilizing minimal power and every gate has buffered outputs.

The 74LS logic family is in Compatibility with the 74HC family in regards to functionality and pin-out.

The inputs of every gate in the IC are safeguarded from damage because of static discharge by internally present diode clamps to the power supply and ground.