

ENROLL NO. > PV-18210082

And NAND gate is AND gate succeeded by NOT gate. A NAND gate constitutes one or more intends with single output. NAND gate has an output that is resmally at logic high and only goes to logic law when all its inputs are at logic high.

The Bodean Expression for NAND gate > (A.B) = 4

2 Input NAND gate

In this NAND gate there are only two input values and an output value.

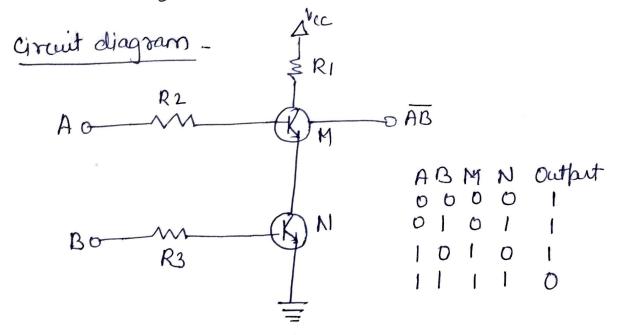
logic Design -

Hom



	Input	Output
A	B	Y
0	O	1
0	1	1
1	O	1
1	,]	0

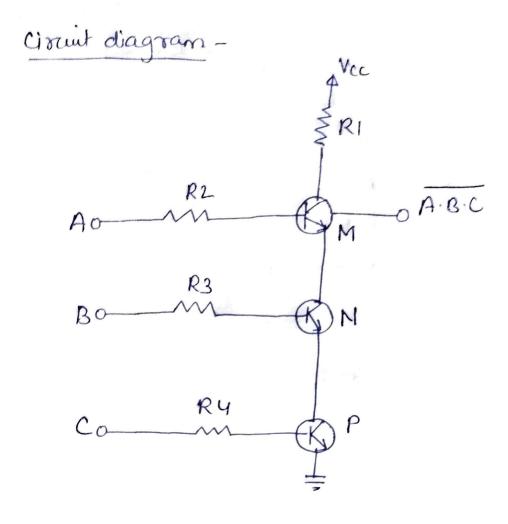
When value of A and B is 0 then A B = 0 and A B = 1 when value of A is 0 and B is 1 then A B = 0 and A B = 1 when value of A is 1 and B is 0 then A B = 0 and A B = 1 when value of A is 1 and B is 1 then A B = 1 and A B = 0 when value of A is 1 and B is 1 then A B = 1 and A B = 0



3 Input NAND gate

3 Input NAND gate has 3 inputs and loutput

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nuth Table -						
n	B	C	M	N	P	Output
A	1)	0	O	0	0	1
0	O	1	O	0	1	
0	O	- 1		1	D	1
O		0	0	i	1	1
O	1	1	0	ı	-	·
1	0	0	1	0	0]
1	0	1		0		1
1		()	1		O	
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for

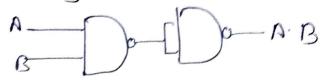
When value of A,B,C is 0 then A.B.C = 0 and AB.C = 1

When value of A = 0, B = 0 and C = 1 A.B.C = 0 and A.B.C = 1

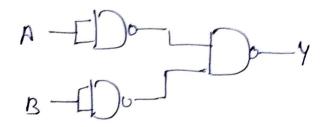
When value of A = 0, B = 1, C = 0? A.B.C = 0? A.B.C = 1 A = 0 B = 1 C = 1 A.B.C = 0 \overline{A} .B.C = 1 A = 1 B = 0 C = 0 A.B.C = 0 \overline{A} .B.C = 1

$$A = 0$$
 $B = 1$ $C = 1$ $A \cdot B \cdot C = 0$ $A \cdot B \cdot C = 1$
 $A = 1$ $B = 0$ $C = 0$ $A \cdot B \cdot C = 0$ $A \cdot B \cdot C = 1$
 $A = 1$ $B = 0$ $C = 0$ $A \cdot B \cdot C = 0$ $A \cdot B \cdot C = 1$
 $A = 1$ $B = 1$ $C = 0$ $A \cdot B \cdot C = 0$ $A \cdot B \cdot C = 1$

AND wing HAND

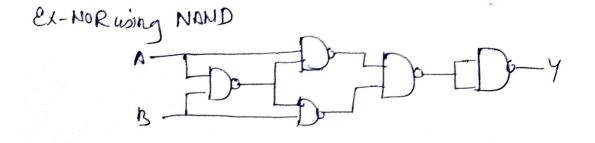


OR using NAND



NOR using NAND A-[DO-DO-Y
B-DO-LDO-Y

EX-OR using NAND A DO DO Y



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