

Total No. of printed pages = 3

MCA 202 E 22

Roll No. of candidate

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2021

MCA. 3rd Semester End-Term Examination

Elective – II – ADVANCED COMPUTER ARCHITECTURE

(New Regulation(w.e.f 2020-21) &
(New syllabus (w.e.f 2020-21))

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

(Answer Q1. And any Four from the rest)

1. A. Choose the correct options for the following questions $(6 \times 1 = 6)$

- (i) A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____.
 - (a) super-scaling
 - (b) pipe-lining
 - (c) parallel computation
 - (d) none of these

- (ii) Which one of the following hazard is also called antidependency ?
 - (a) RAW
 - (b) WAR
 - (c) WAW
 - (d) RAR

- (iii) Speed up of a 'n' stage pipeline system in processing 'k' tasks is:
 - (a) $nk/n+(k-1)$
 - (b) $nk/n-(k+1)$
 - (c) $nk/n+(k+1)$
 - (d) $nk/n-(k-1)$

- (iv) The grain of parallelism in both vector and array processor is of type:
 - (a) Job level
 - (b) Program level
 - (c) Instruction level
 - (d) Intrainstruction level

- (v) Some of the characteristics of vector and array processors are combined in:
 - (a) Multiprocessor
 - (b) Systolic processor
 - (c) Uniprocessor
 - (d) Scalar processor

[Turn over

(vi) A common synchronization mechanism used in multiprocessor operating system is:

- | | |
|-------------|--------------|
| (a) Complex | (b) Lockstep |
| (c) Clock | (d) Locks |

(B) State True or False.

$(4 \times 1 = 4)$

- (i) Pipeline reduces the execution time of an individual instruction.
- (ii) Presence of multiple caches in multiprocessor system introduces the cache coherence problem.
- (iii) Data hazard arises when two instructions refer to the same memory locations.
- (iv) In a multiprocessor system, if one processor fails the system will halt.

2. (a) Discuss the architectural classification scheme which is based on multiplicity of instruction stream and data stream. (8)

(b) What is pipelining ?

What are instruction pipelining and arithmetic pipelining? Explain. $(2+5=7)$

3. (a) What is the role of a pipeline Stage and a Latch. How is the clock period set in designing a synchronous pipelined system? $(3+2=5)$

(b) What do you mean by a Hazard ? How does dependency hazard differ from collision hazard? $(2+3=5)$

(c) Explain the forwarding technique used to resolve RAW hazard. (5)

4. (a) What is the use of Virtual functional unit? Explain with example and timing diagram. (7)

(b) Distinguish between static and dynamic approaches of hazard detection. Which one is suitable and why? $(3+2=5)$

(c) What are blocking and Non-blocking networks? (3)

5. (a) What are the different fields used to specify a vector instruction? (3)

(b) Compare vector processor with array processor. (6)

(c) Clearly discuss the concept of Vector chaining. (6)

6. (a) Show the structural components of the CRAY-1 vector super computer with the help of a diagram and explain the functions of each subsystem. (9)

(b) How can you distinguish vector processing from scalar processing? How is vector processing advantageous? Mention the different types of vector instructions with one example for each type. (6)

7. (a) Write down the main characteristics of a multiprocessor system. (5)
- (b) Briefly discuss any one category of interconnection networks in SIMD array processors. (3)
- (c) What do you mean by process synchronization? Discuss any one technique of process synchronization based on shared variable. (7)
8. (a) Distinguish between the following: $(2 \times 3.5 = 7)$
- (i) Data flow and Control flow computers
 - (ii) Static and dynamic model of data flow computation
- (b) Write short notes on *any two* of the following. $(2 \times 4 = 8)$
- (i) Architecture of SIMD array processor with block diagram
 - (ii) Advantages and disadvantages of the cross-bar interconnection scheme
 - (iii) Delayed branch scheme
 - (iv) Memory latency problem and its solution

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MCA 18250 E 22

Roll No. of candidate

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2021

M.C.A. 5th Semester End-Term Examination

Elective - II

COMPUTER ARCHITECTURE

(New Regulation and New Syllabus)

(W.e.f. 2018-19)

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer Q. 1 and any five from the rest.

1. (Write brief answer for any *Five* of the following) $(5 \times 2 = 10)$

- (a) Define parallel processing.
- (b) What do you mean by a Hazard?
- (c) What is a pipelining? Define.
- (d) List the different levels of parallel processing in the order of hardware involvement.
- (e) Give the reason of using latches in between the two stages of pipeline system.
- (f) What are blocking and Non-blocking networks?
- (g) Mention any two differences between multiprocessors and multicollectors.
- (h) Draw a Gantt chart of a four stage instruction pipelining system.

2. (a) On what basis different architectural classifications of computers are made?
Discuss Flynn's classification in detail. (8)

- (b) Explain the terms 'throughput' and 'speed up' in a pipeline system. (4)

3. (a) Describe any two methods used to conduct parallel processing in uniprocessor system. (6)
- (b) Distinguish between the following: (6)
- (i) Multiprogramming and Multiprocessing
- (ii) Serial processing and Parallel processing
4. (a) Explain different types of data dependency hazards with example. (7)
- (b) Illustrate the concept of Vector chaining clearly. (5)
5. (a) Show the structural components of the CRAY-1 vector super computer with the help of a diagram and explain the functions of each subsystem. (9)
- (b) Mention any three major points to distinguish between Vector processor and Array processor. (3)
6. (a) Describe the advantages and disadvantages of the cross-bar interconnection scheme. (6)
- (b) Mention the main characteristics of a multiprocessor system. (6)
7. (a) Explain the architecture of SIMD array processor with block diagram. (9)
- (b) Write down the main differences between Data flow and Control flow computers. (3)
8. (a) Give the concept of Data flow computer. State the difference between static and dynamic model of data flow computation. (3+3=6)
- (b) Draw a Data flow graph for the following: (6)

Input x, n

$Y = 1; I = 1;$

While $i < n$ do

Begin

$Y = y * x;$

$I = I + 1;$

End

$z = y$

output z

9. Write brief notes on any *three* of the following: $(3 \times 4 = 12)$
- (a) Conceptual view of a typical multiprocessor organization.
 - (b) Blocking Network and Non-blocking Network.
 - (c) Delayed branch scheme
 - (d) Omega network
 - (e) Parallel algorithm for array processor
 - (f) Multifunctional pipelining
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