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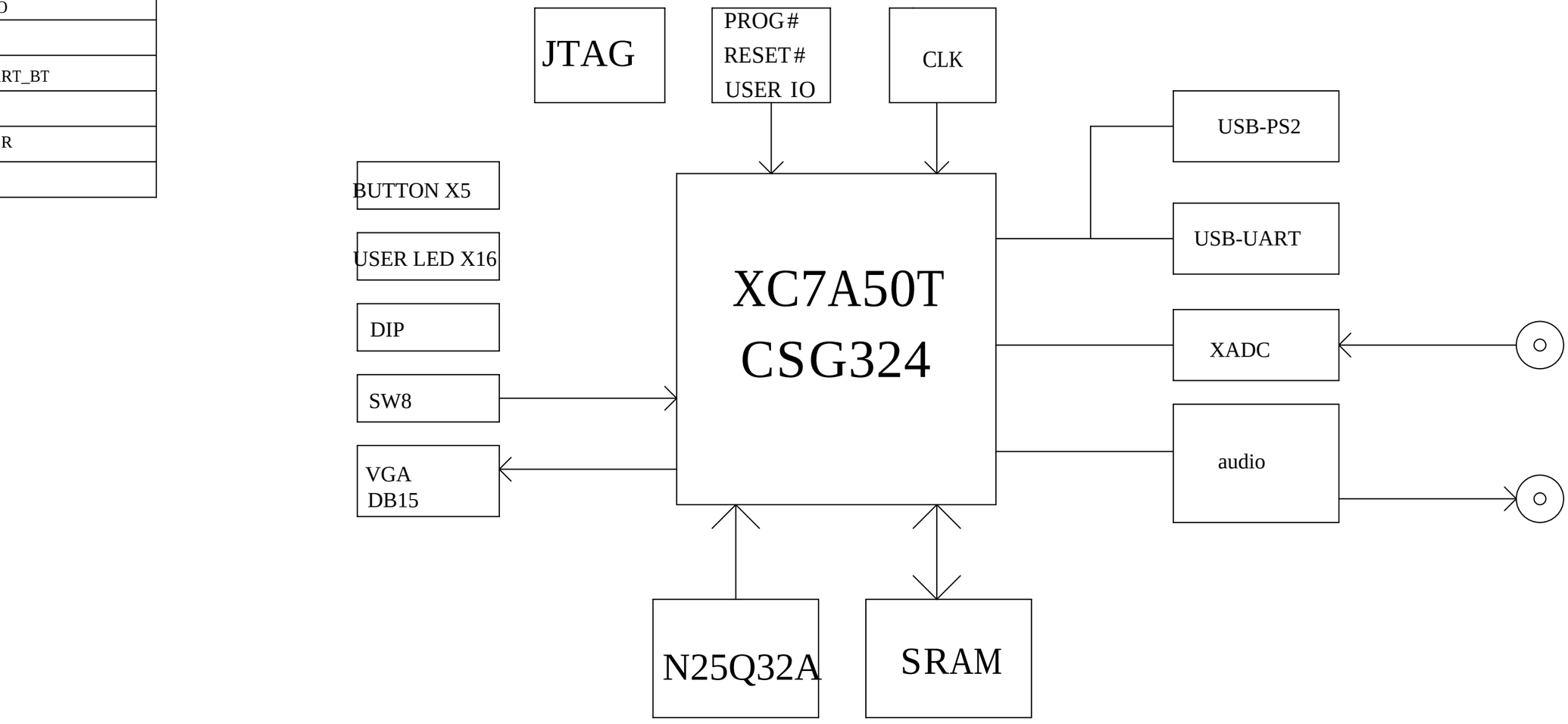

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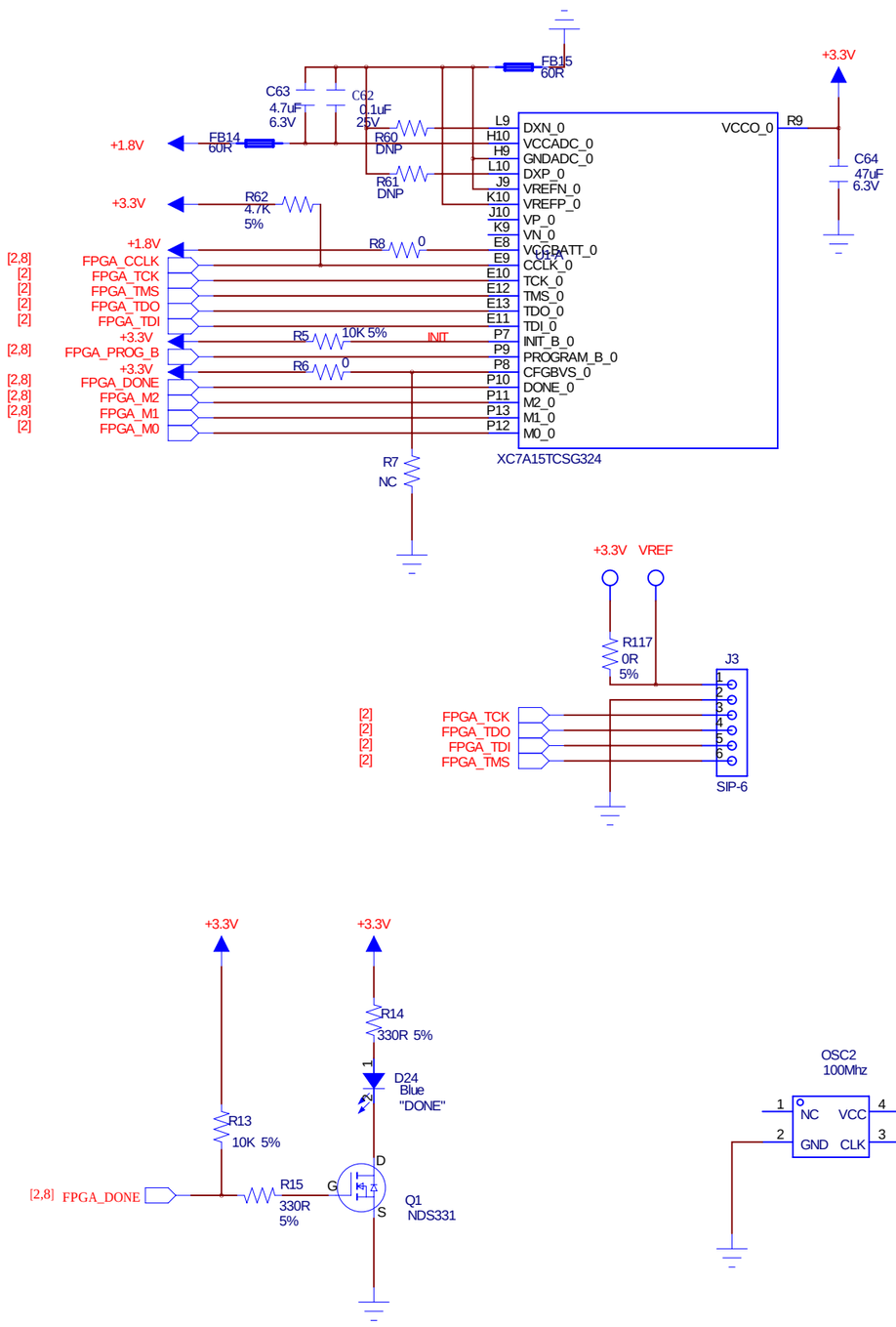
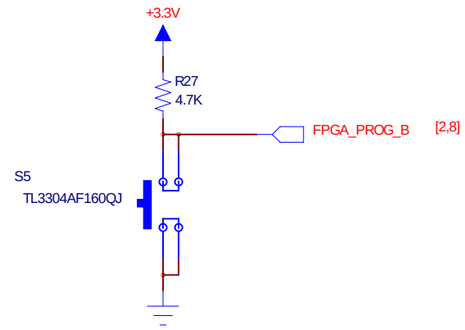
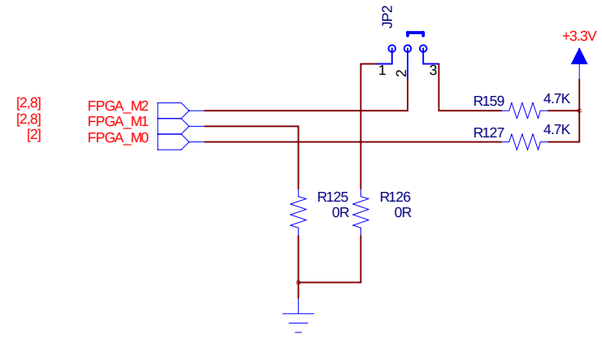
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 1 OF 10
RELEASED:		E-ELEMENTS			

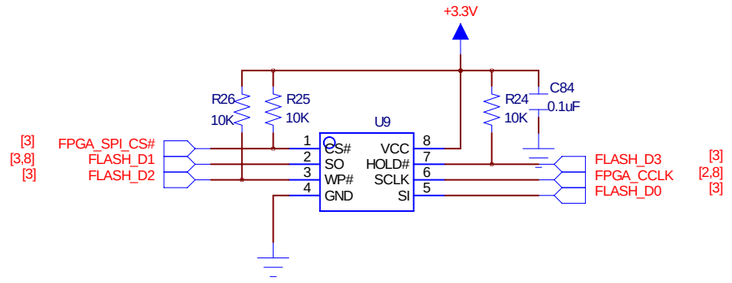
Table 2-1: **7 Series FPGA Configuration Modes**

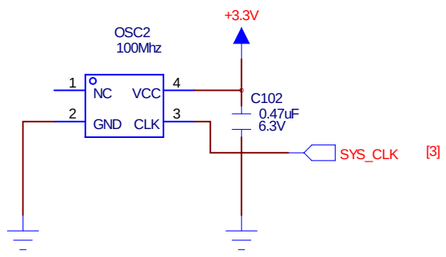
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input











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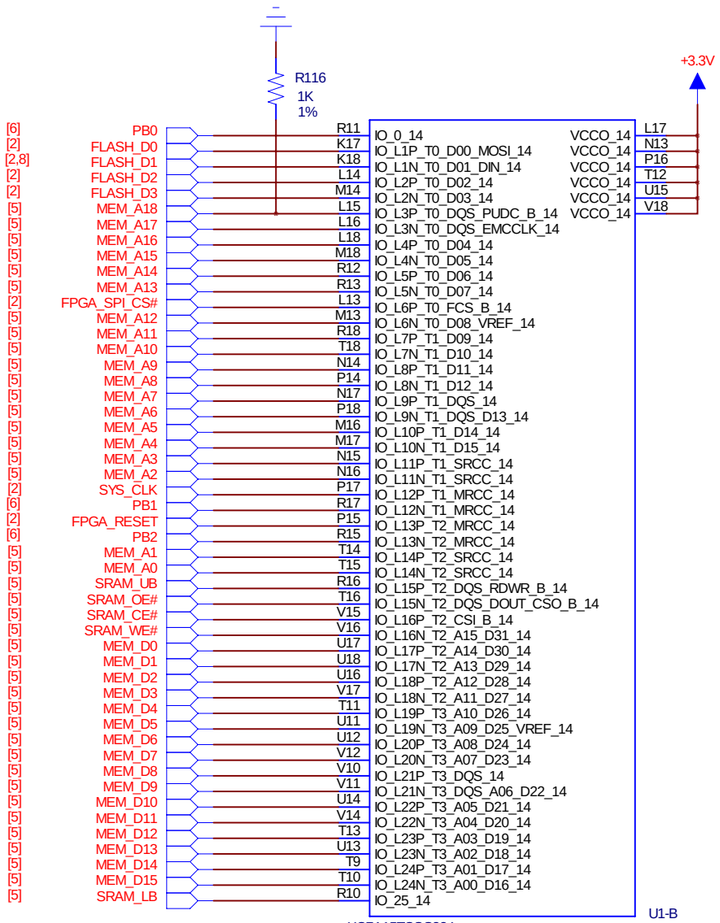

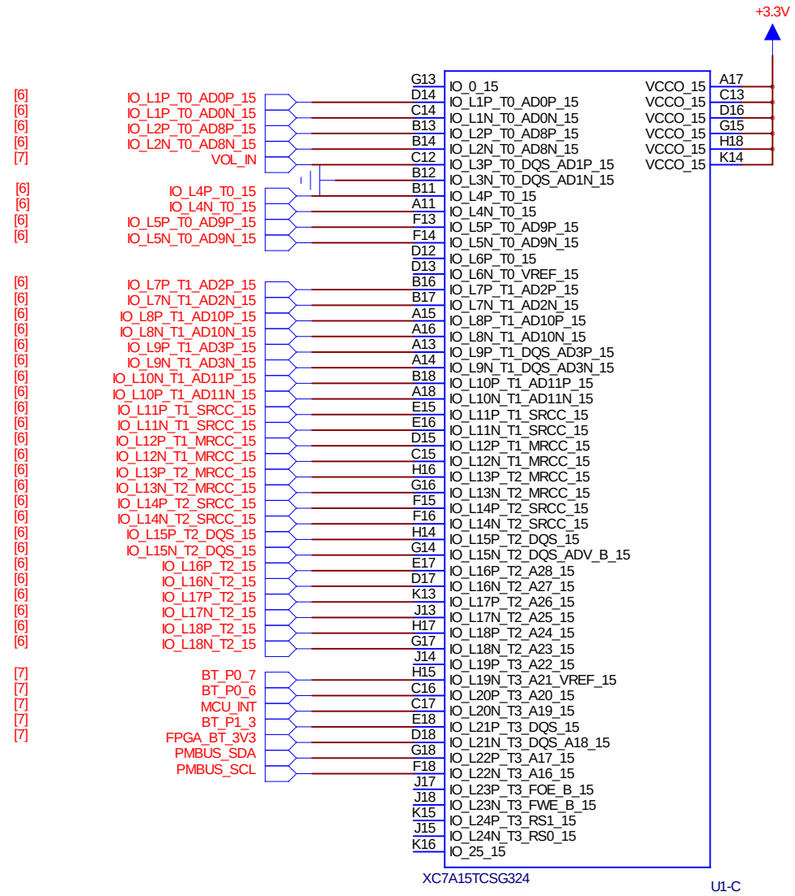

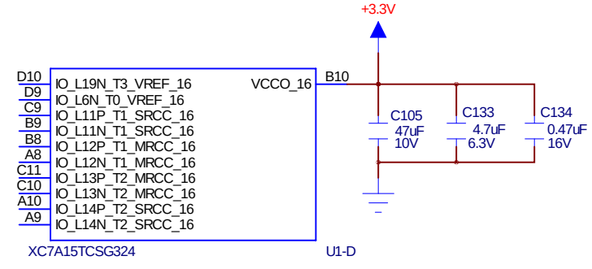

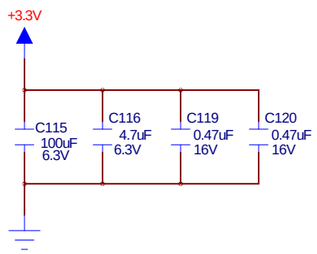

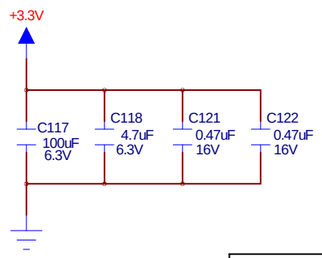

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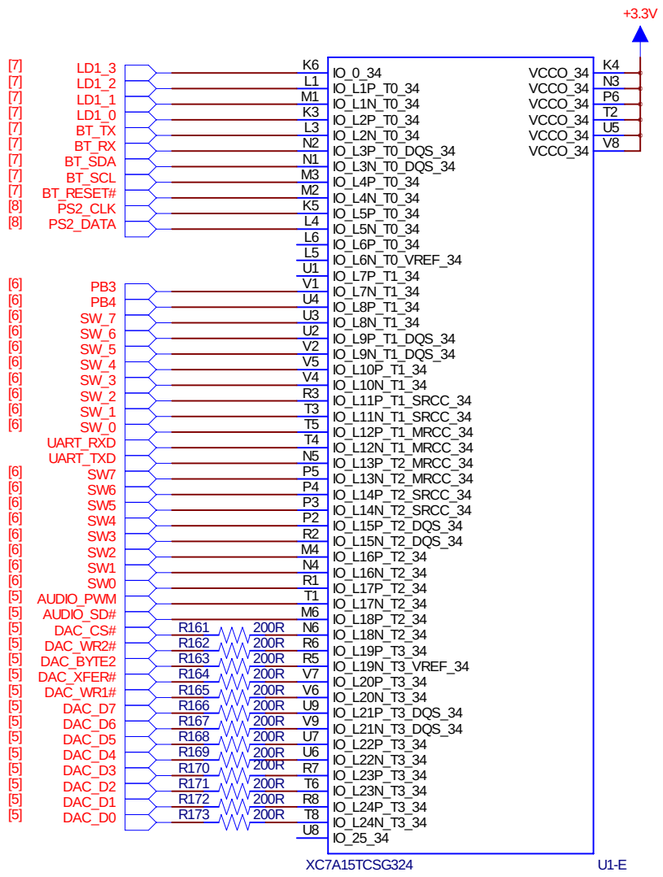

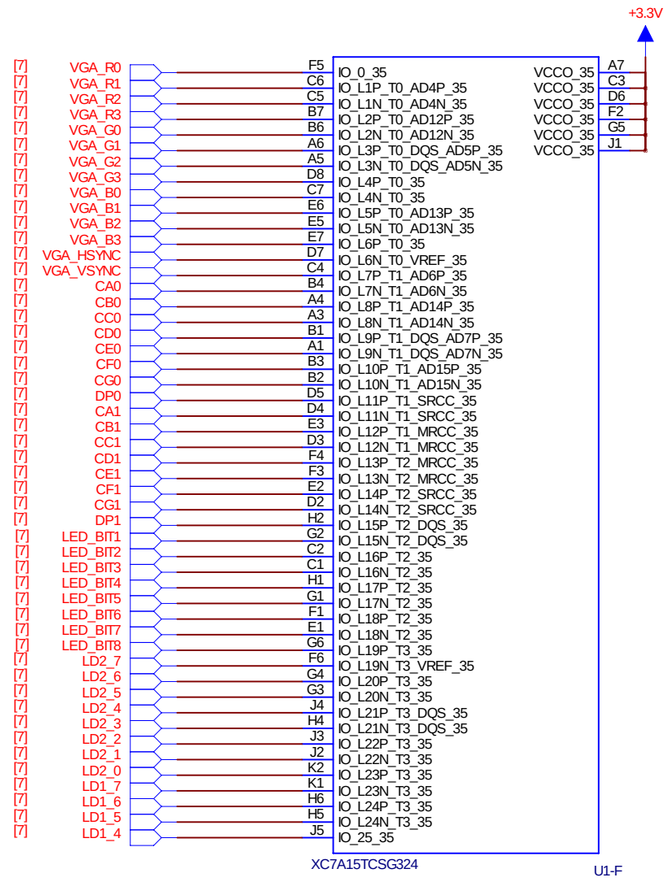

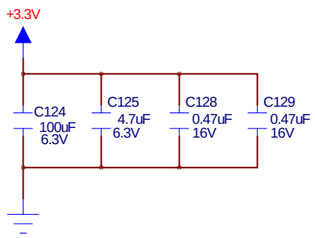

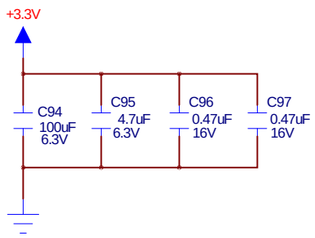

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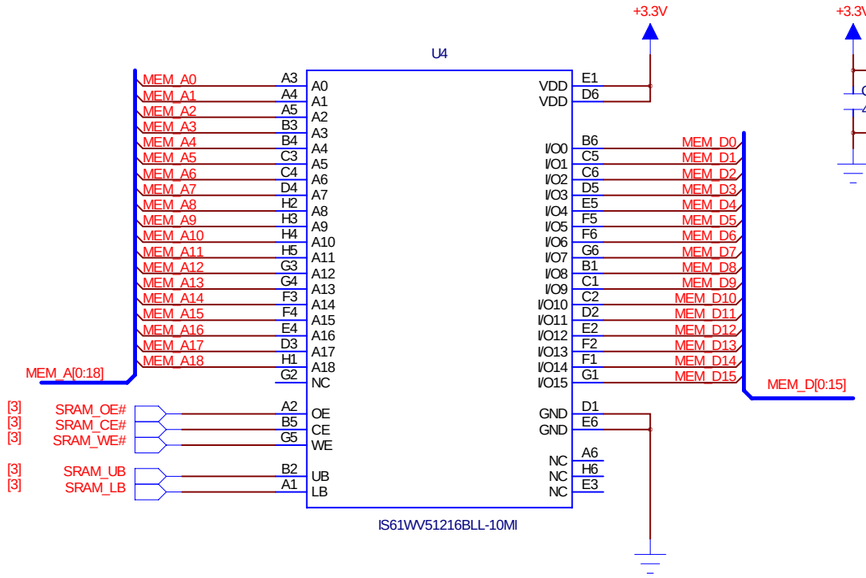

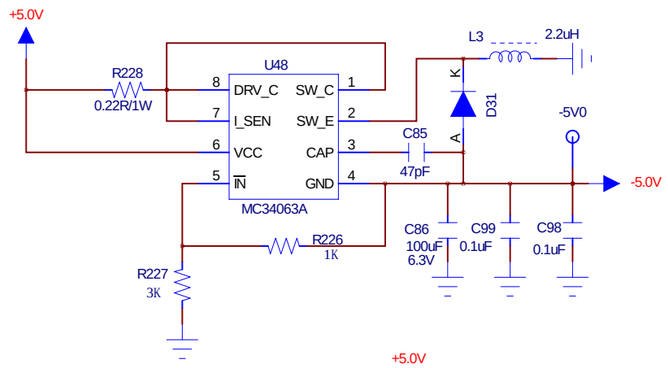

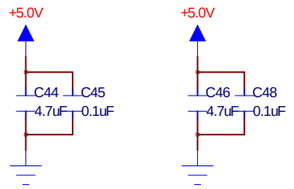

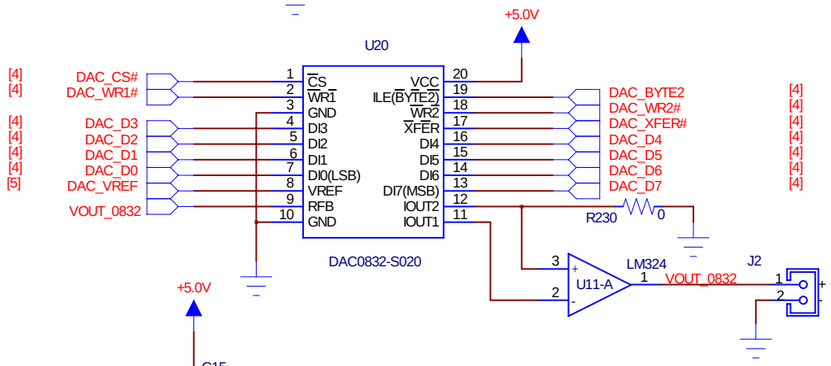

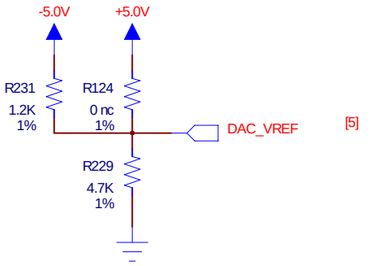

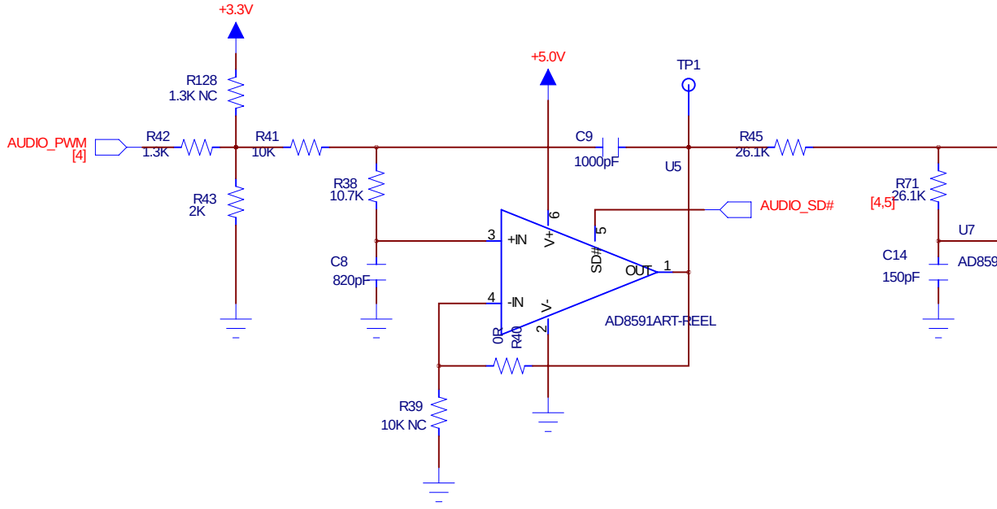

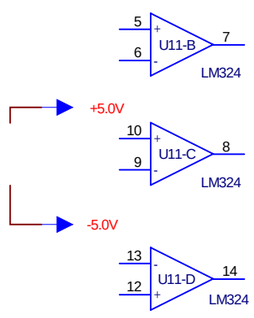

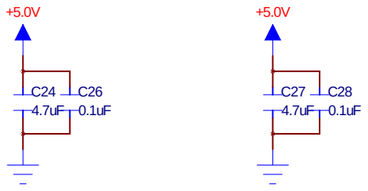

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REVISION RECORD			
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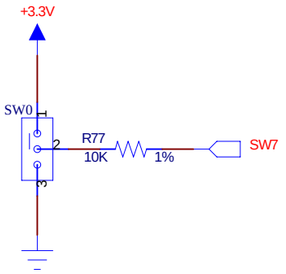

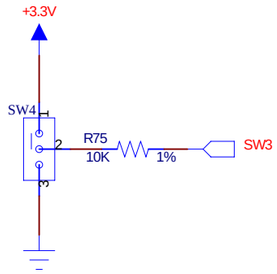

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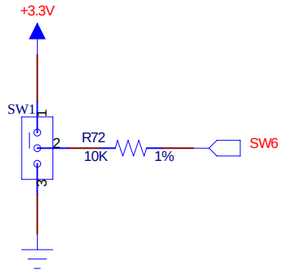

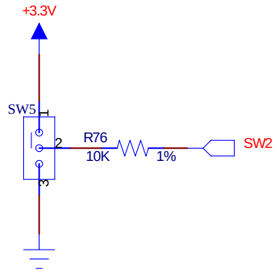

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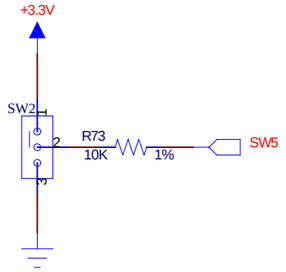

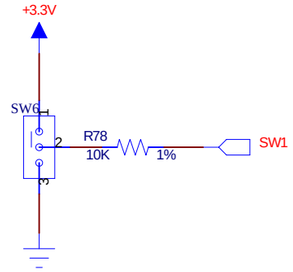

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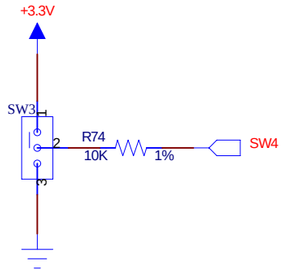

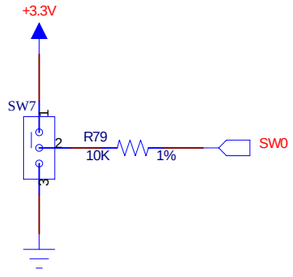

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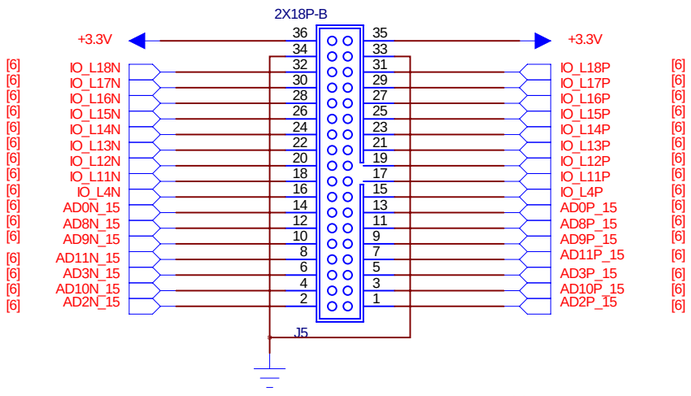
[3] IO_L1P_T0_AD0N_15 — R135 100R — C40 NC — AD0N_15 [6]
[3] IO_L2P_T0_AD8P_15 — R120 100R — C37 — AD8P_15 [6]
[3] IO_L2N_T0_AD8N_15 — R131 100R — C37 NC — AD8N_15 [6]
[3] IO_L5P_T0_AD9P_15 — R118 100R — C34 — AD9P_15 [6]
[3] IO_L5N_T0_AD9N_15 — R119 100R — C34 NC — AD9N_15 [6]
[3] IO_L7P_T1_AD2P_15 — R136 100R — C41 — AD2P_15 [6]
[3] IO_L7N_T1_AD2N_15 — R137 100R — C41 NC — AD2N_15 [6]
[3] IO_L8P_T1_AD10P_15 — R140 100R — C43 — AD10P_15 [6]
[3] IO_L8N_T1_AD10N_15 — R141 100R — C43 NC — AD10N_15 [6]
[3] IO_L9P_T1_AD3P_15 — R138 100R — C42 — AD3P_15 [6]
[3] IO_L9N_T1_AD3N_15 — R139 100R — C42 NC — AD3N_15 [6]
[3] IO_L10N_T1_AD11P_15 — R132 100R — C38 — AD11P_15 [6]
[3] IO_L10P_T1_AD11N_15 — R133 100R — C38 NC — AD11N_15 [6]



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[3] IO_L17P_T2_15 — R142 200R — IO_L17P [6]
[3] IO_L17N_T2_15 — R143 200R — IO_L17N [6]
[3] IO_L16P_T2_15 — R144 200R — IO_L16P [6]
[3] IO_L16N_T2_15 — R145 200R — IO_L16N [6]
[3] IO_L15P_T2_DQS_15 — R146 200R — IO_L15P [6]
[3] IO_L15N_T2_DQS_15 — R147 200R — IO_L15N [6]
[3] IO_L14P_T2_SRCC_15 — R148 200R — IO_L14P [6]
[3] IO_L14N_T2_SRCC_15 — R149 200R — IO_L14N [6]
[3] IO_L13P_T2_MRCC_15 — R150 200R — IO_L13P [6]
[3] IO_L13N_T2_MRCC_15 — R151 200R — IO_L13N [6]
[3] IO_L12P_T1_MRCC_15 — R152 200R — IO_L12P [6]
[3] IO_L12N_T1_MRCC_15 — R153 200R — IO_L12N [6]
[3] IO_L11P_T1_SRCC_15 — R154 200R — IO_L11P [6]
[3] IO_L11N_T1_SRCC_15 — R155 200R — IO_L11N [6]
[3] IO_L4P_T0_15 — R156 200R — IO_L4P [6]
[3] IO_L4N_T0_15 — R157 200R — IO_L4N [6]

D23 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
IO_L4P [6]
IO_L4N [6]
AD0P_15 [6]
AD0N_15 [6]

D22 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
AD8P_15 [6]
AD8N_15 [6]
AD9P_15 [6]
AD9N_15 [6]

D21 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
AD2P_15 [6]
AD2N_15 [6]
AD10P_15 [6]
AD10N_15 [6]

D20 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
AD3P_15 [6]
AD3N_15 [6]
AD11P_15 [6]
AD11N_15 [6]

D25 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
IO_L18P [6]
IO_L18N [6]
IO_L17P [6]
IO_L17N [6]

D26 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
IO_L15P [6]
IO_L16N [6]
IO_L16P [6]
IO_L15N [6]

D27 TPD4E002DRLR
2 GND; IO4 IO3 IO2 IO1 5 4 3 1
IO_L14P [6]
IO_L14N [6]
IO_L13P [6]
IO_L13N [6]

D28 TPD4E002DRLR
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IO_L12N [6]
IO_L11P [6]
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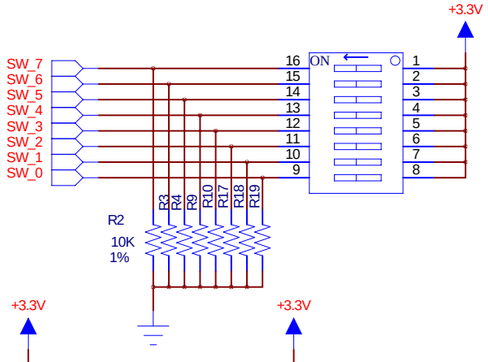

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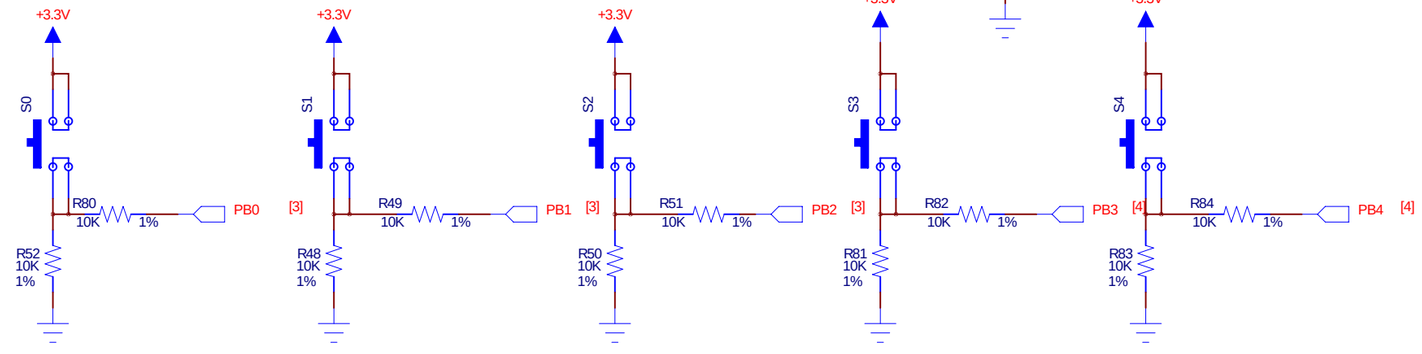

TITLE: IO

Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 6 OF 10
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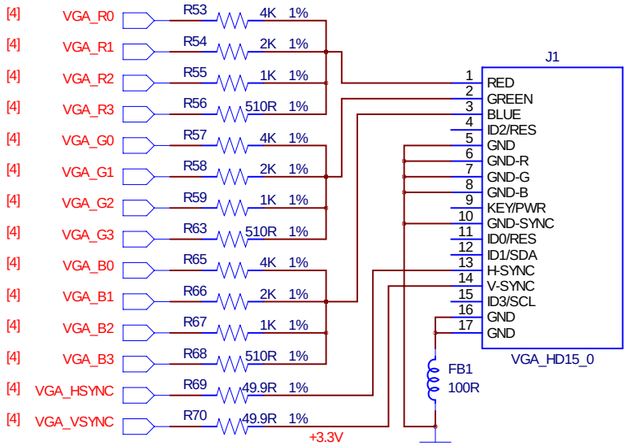
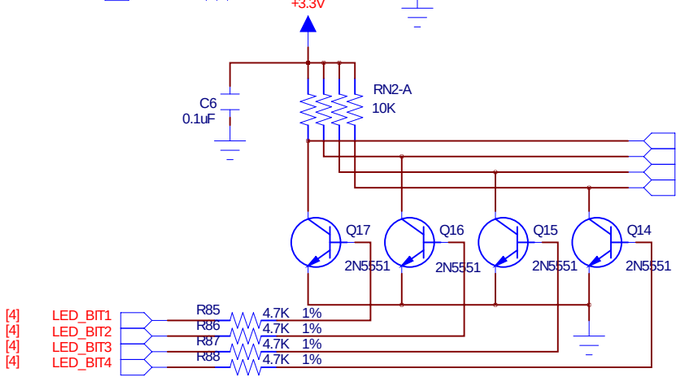
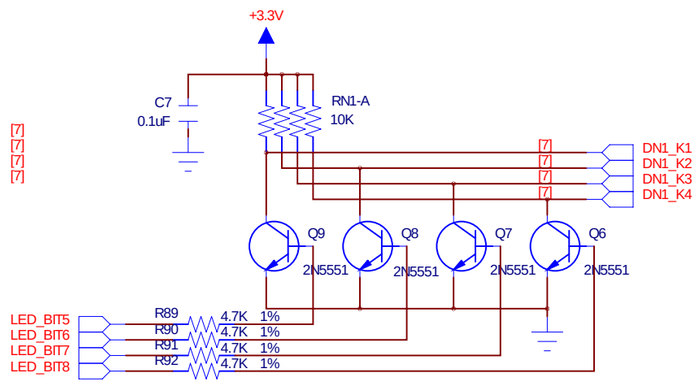
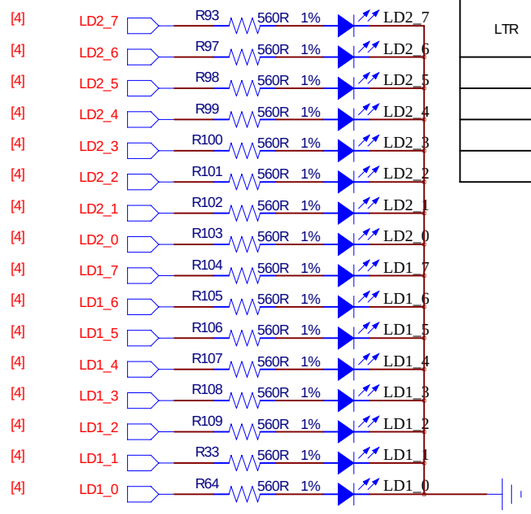
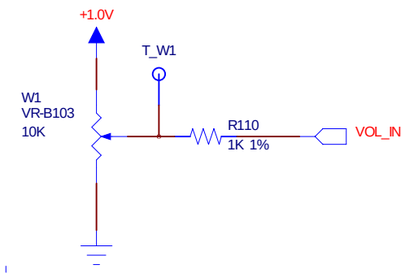
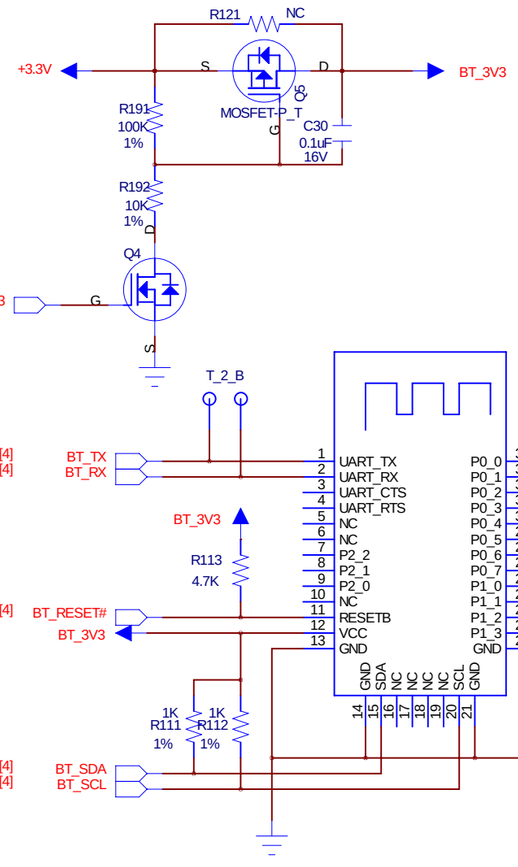


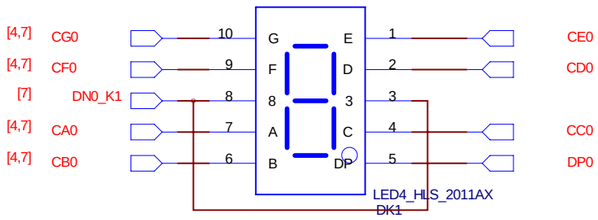


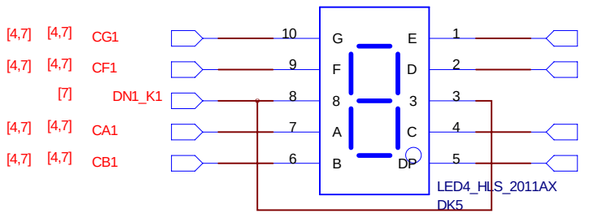


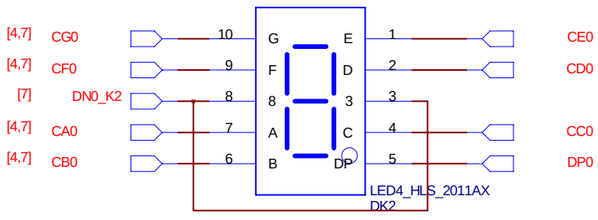


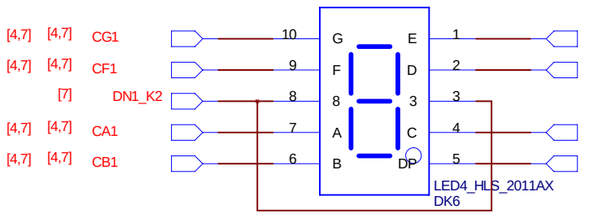


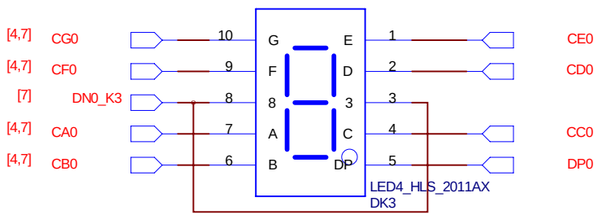


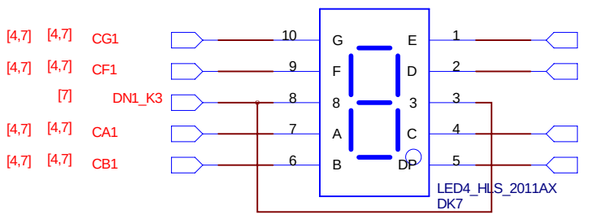


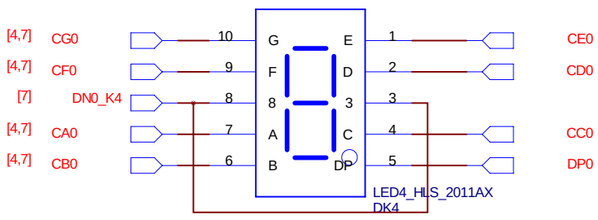


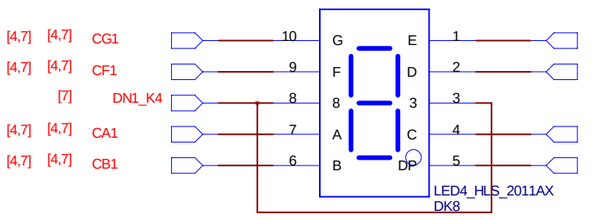












TITLE: DISPLAY_UART_BT

Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 7 OF 10
RELEASED:		E-ELEMENTS			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

+3.3V

C65 10uF C66 0.1uF

U12 PIC24FJ128GB106

1 PMD5/CN63/RE5
2 SCL3/PMD6/CN64/RE6
3 SDA3/PMD7/CN65/RE7
4 C1IND/RP21/PMA5/CN8/RG6
5 C1INC/RP26/PMA4/CN9/RG7
6 C2IND/RP19/PMA3/CN10/RG8
7 /MCLR
8 RP27/PMA2/C2INC/CN11/RG9
9 VSS
10 VDD
11 PGEC3/AN5/C1INA/VBUSON/RP18/CN7/RB5
12 PGED3/AN4/C1INB/USBOEN/RP28/CN6/RB4
13 AN3/C2INA/VPIO/CN5/RB3
14 AN2/C2INB/VMIO/RP13/CN4/RB2
15 PGEC1/AN1/VREF-/RP1/CN3/RB1
16 PGED1/AN0/VREF+/RP0/PMA6/CN2/RB0
17 PGEC2/AN6/RP6/CN24/RB6
18 PGED2/AN7/RP7/RCV/CN25/RB7
19 AVDD
20 AVSS
21 AN8/RP8/CN26/RB8
22 AN9/RP9/PMA7/CN27/RB9
23 TMS/CVREF/AN10/PMA13/CN28/RB10
24 TDO/AN11/PMA12/CN29/RB11
25 VSS
26 VDD
27 TCK/AN12/PMA11/CTED2/CN30/RB12
28 TDI/AN13/PMA10/CTED1/CN31/RB13
29 AN14/CTPLS/RP14/PMA1/CN32/RB14
30 AN15/RP29/REFO/PMA0/CN12/RB15
31 SDA2/RP10/PMA9/CN17/RF4
32 SCL2/RP17/PMA8/CN18/RF5
33 RP16/USBID/CN71/RF3
34 VBUS
35 VUSB
36 D-/RG3
37 D+/RG2
38 VDD
39 OSCI/CLKI/CN23/RC12
40 OSCO/CLKO/CN22/RC15
41 VSS
42 RTCC/DMLN/RP2/CN53/RD8
43 DPLN/SDA1/RP4/CN54/RD9
44 SCL1/RP3/PMCS2/CN55/RD10
45 RP12/PMCS1/CN56/RD11
46 DMH/RP11/INT0/CN49/RD0
47 SOSCI/C3IND/CN1/RC13
48 SOSCO/T1CLK/C3INC/RPI37/CN0/RC14
49 PCPCON/RP24/CN50/RD1
50 DPH/RP23/CN51/RD2
51 RP22/PMBE/CN52/RD3
52 RP25/PMWR/CN13/RD4
53 C3INB/CN15/RD6
54 C3INA/CN16/RD7
55 VCAP/VDDCORE
56 ENVREG
57 VBUSST/VCMPST1/CN68/RF0
58 VCMPST2/CN69/RF1
59 PMD0/CN58/RE0
60 PMD1/CN59/RE1
61 PMD2/CN60/RE2
62 PMD3/CN61/RE3
63 PMD4/CN62/RE4
64

[8] PIC_MCLR
+3.3V
[2] INIT R176 100R
[4] PS2_DATA
[4] PS2_CLK
+3.3V R174 330R D29

R177 100R 5%
R178 100R 5%
R179 100R 5%
R180
R181
R182

PIC_PGC2 [8]
PIC_PGD2 [8]
+3.3V
FPGA_M1 [2]
FPGA_M2 [2]
+3.3V
FPGA_DONE [2]
FPGA_PROG_B [2]
FLASH_D1 [2,3]
FPGA_CCLK [2]

R232 0
PIC_12M [8]
C49 20pF NC
C51 20pF NC
U13 8Mhz NC
USB0_D+ [8]
USB0_D- [8]
+3.3V

U10
+3.3V
C100 0.47uF 6.3V
PIC_12M [8]

USB0_VBUS_SEL
R183 NL
+5.0V_IN
MOSFET-P_T
R184 100K 1%
C68 0.1uF 16V
R185 47K
[8]
[8]
USB0_D-
USB0_D+
FB4 100R
C67 1uF 16V
J4
VBUS DM DP GND

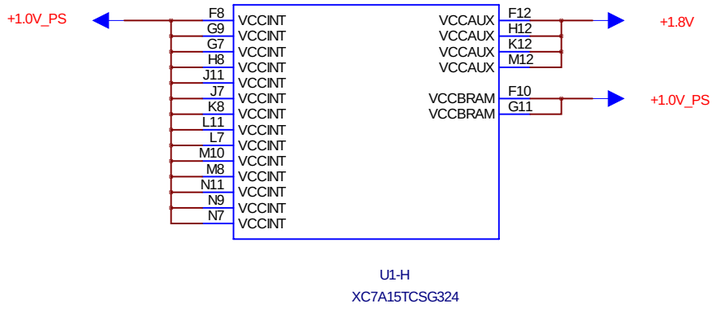
+5.0V
R233 10K 1%
R234 3.3K 1%
R186 10K 1%
Q2

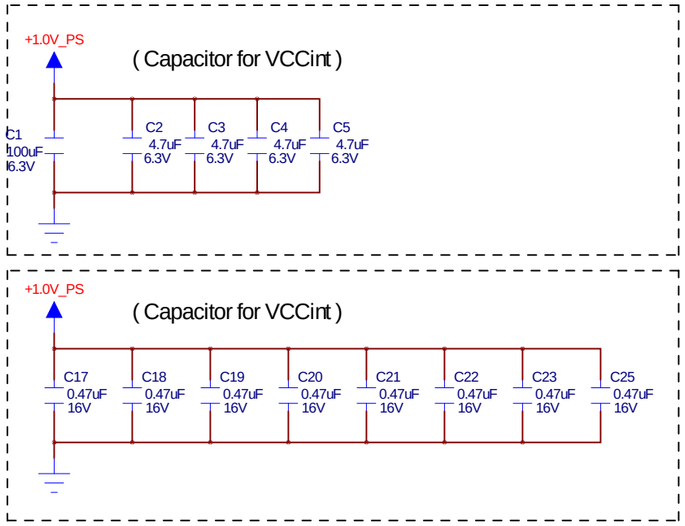
+3.3V
R190 100R
J10
SIP-6
R189 100R PIC_MCLR [8]
R188 100R PIC_PGD2 [8]
R187 100R PIC_PGC2 [8]

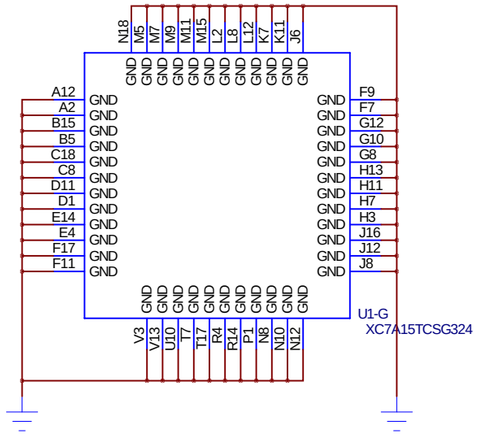
+3.3V
C53 0.1uF
C54 0.1uF
C57 0.1uF
C58 0.1uF
C60 0.1uF
C61 0.1uF

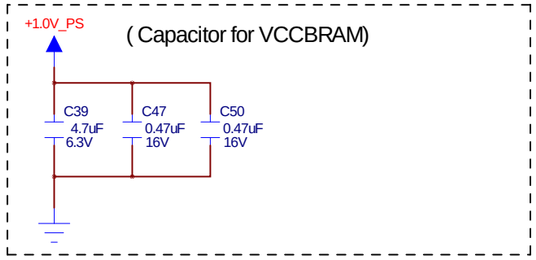
TITLE: PIC_USB					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 8 OF 10
RELEASED:		E-ELEMENTS			

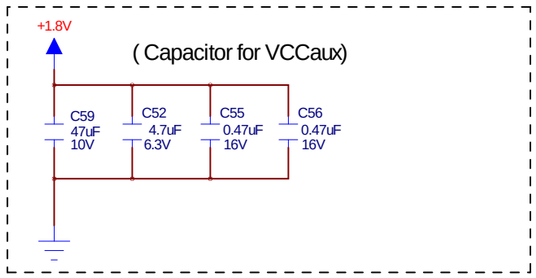
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





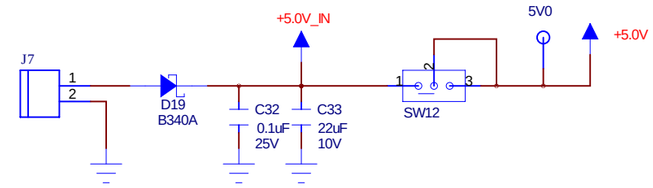


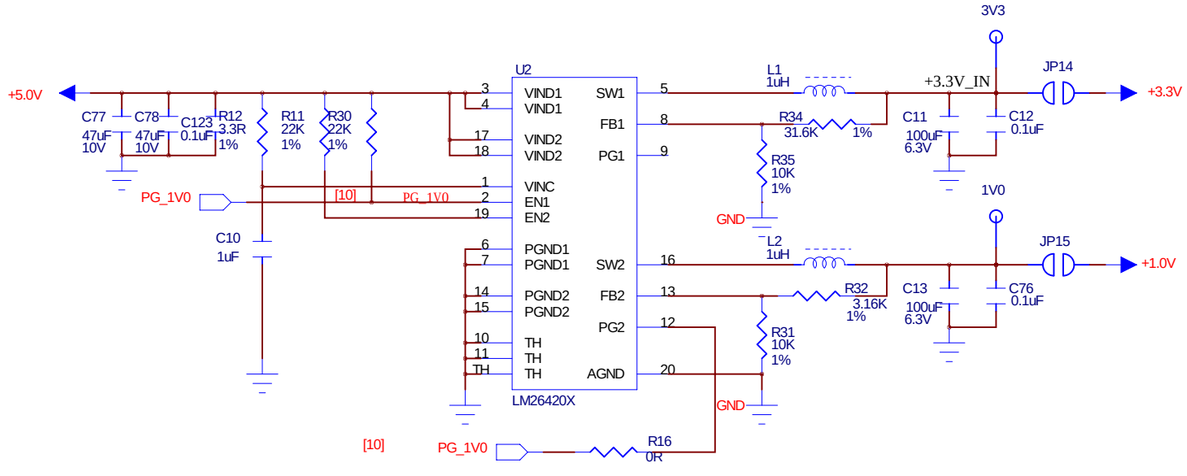


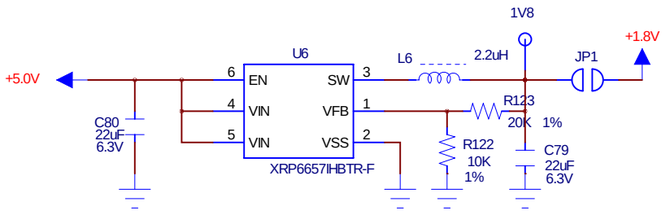


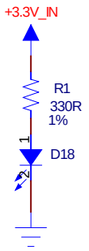
TITLE: FPGA_POWER					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 9 OF 10
RELEASED:		E-ELEMENTS			

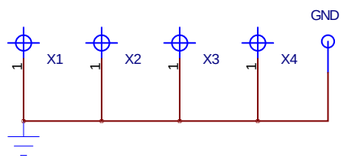
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:











TITLE:	POWER				
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 10 OF 10
RELEASED:		E-ELEMENTS			