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Cache miss simulator report

INTRODUCTION:

This report discusses the implementation of cache miss simulator in C.The goal of this code is to simulate the cache to identify which accesses would cause a cache hit and which accesses would cause a cache miss.

Coding Approach:

Code will open cache.config file using fopen() function and reads first 3 lines and store it in arr[ ] integer array and next 2 lines in str[ ][ ] string array.Then it will find the number of sets,offset bits,index bits,tag bits.It is initialising the cache[ ] [ ] array to -1.It will open the cache.access file using fopen( ) function and read every line.Then it will store the mode in “y” and convert the hexadecimals to integers and store that in decimal variable.It will then find the values of tag and set index by bitwise operations.For FIFO and RANDOM when cache hits i.e; when the tag matches with the tag in the array then it will print the hit there.For LRU when cache hits then it will update the tag value to last index of that array so that first index will be the least used index.For FIFO when cache misses and the cache is full then it will remove the first index tag and shift the array and insert the tag on the last index of the array. If cache is not full then it will just insert.For LRU it will shift array by one and insert the tag at the last index.For Random it will randomly select one index and replace it with the tag.

I had checked with few test cases to check whether my code is correct or not.