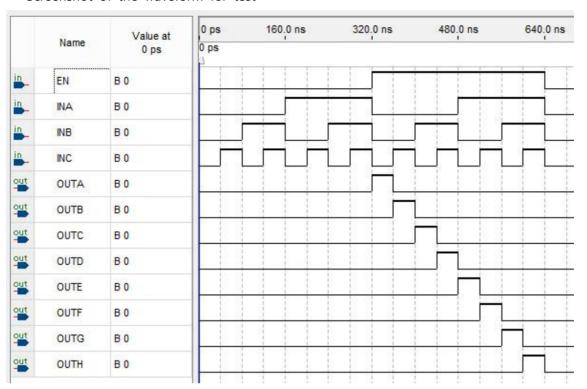
VHDL code

```
decoder3 8.vhd
                                                                                                               ×
                         Home
       66 (7) II II | 10 10 10 10 267 =
          library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
 2
 3
 4
        □entity decoder3_8 is
  5
        □port (
 6
               INA : in std_logic;
               INB : in std_logic;
INC : in std_logic;
 8
 9
10
               EN : in std_logic;
11
12
               OUTA : out std_logic;
               OUTB : out std_logic;
13
14
               OUTC : out std_logic;
               OUTD : out std_logic;
OUTE : out std_logic;
15
16
17
               OUTF : out std_logic;
               OUTG : out std_logic;
OUTH : out std_logic);
18
19
20
          end decoder3_8;
21
22
        □architecture Behavioral of decoder3_8 is
23
        ⊟begin
24
        □process(INA, INB, INC, EN)
25
26
27
       | begin

if(EN = '1') then
               OUTA <= (not INA) and (not INB) and (not INC);
OUTB <= (not INA) and (not INB) and INC;
OUTC <= (not INA) and INB and (not INC);
OUTD <= (not INA) and INB and (not INC);
OUTD <= (not INA) and INB and (not INC);
28
29
30
               OUTE <= INA and (not INB) and (not INC);
OUTF <= INA and (not INB) and INC;
OUTG <= INA and INB and (not INC);
31
32
33
34
               OUTH <= INA and INB and INC;
35
               Se -- EN = '0'
OUTA <= '0';OUTB <= '0';OUTC <= '0';OUTD <= '0';
OUTE <= '0';OUTF <= '0';OUTG <= '0';OUTH <= '0';
36
37
38
        end if;
end process;
39
40
          end Behavioral;
41
```

- INA, INB, INC for input
- EN for input (enable signal)
- OUTA, OUTB, OUTC, OUTD, OUTE, OUTF, OUTG, OUTH for output

Screenshot of the waveform for test



• Explanation

- Truth Table for decoder 3 to 8

INA	INB	INC	EN	OUTA	OUTB	OUTC	OUTD	OUTE	OUTF	OUTG	OUTH
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. 3 to 8 decoder has 3 inputs(INA, INB, INC), 8 possible input binary numbers that match with OUTA, OUTB, OUTC, OUTD, OUTE, OUTF, OUTG, OUTH. 'EN' is enable signal. when 'EN' is 0, decoder dose not work.