- VHDL source code

BCD.vhd | Compilation Report - BCD

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3   USE ieee.std_logic_unsigned.all;
4
5   ENTITY BCD IS
6   PORT (
7       clk, clear : IN STD_LOGIC;
8       MSB, LSB : OUT STD_LOGIC_VECTOR (0 to 3));
9   END BCD;
10
11  ARCHITECTURE BEHAVIOAL OF BCD IS
12  signal temp1, temp2: STD_LOGIC_VECTOR(0 to 3); -- count 0 to 10
13  BEGIN
14  PROCESS(clk, clear)
15
16  BEGIN
17
18  IF (clear = '0') THEN
19      temp1 <= "0000";
20      temp2 <= "0000";
21
22  ELSIF (clk'EVENT AND clk='1') THEN
23      temp1 <= temp1 + '1';
24      IF(temp1 = "1001") THEN
25          temp1 <= "0000";
26          temp2 <= temp2 + 1;
27          IF(temp2 = "1010") THEN
28              temp2 <= "0000";
29          END IF;
30      END IF;
31  END IF;
32  END PROCESS;
33
34      LSB(0) <= temp1(0); LSB(1) <= temp1(1); LSB(2) <= temp1(2); LSB(3) <= temp1(3);
35      MSB(0) <= temp2(0); MSB(1) <= temp2(1); MSB(2) <= temp2(2); MSB(3) <= temp2(3);
36
37  END BEHAVIOAL;
38
```

- Simulation result