Digital Electronics - Electronics, Devices and Circuits

Kevalee Shah

April 13, 2019

1 Electricity

- In metals drift speed of electrons is low, as the free electrons collide with the metal ions often, but when the battery is applied the electrons start moving together
- *Coulomb* (C) is the unit of charge (Q)
- $I = \frac{Q}{t}$
- emf is a property of the battery, which is volts + volts wasted in the battery. (used interchangeably in notes) - rate at which battery gives energy to charge
- $V = \frac{E}{Q}$
- $P = \frac{E}{t}$
  Using $E = QV$, we get $P = \frac{QV}{t}$
  Using $Q = It$, we get $P = IV$

2 Semiconductors

Whether a material is a conductor or a insulator depends on how strongly the valence electrons are bonded to the nucleus.
Conductors have weakly bonded electrons and therefore when voltage is applied charge flows.

- Have a low electron density and therefore easier to control properties.
- Made out of silicon, a group 4 element and therefore forms 4 covalent bonds. As temp rises the covalent bonds break and free electrons are able to move through the crystal - leaves behind a hole

2.1 n-type

- n-type silicon doped with a Group 5 element, e.g. Arsenic
- Extra electron cant form bonds with the silicon and therefore free to move through the structure.

- Overall the semiconductor is still neutral, but relative to the silicon model, electron-wise there are more electrons and therefore it is called n-type.
- Arsenic is called a donor

2.2 p-type

- p-type silicon doped with Group 3 element, e.g. Boron
- Has one less electron and therefore and therefore there is a hole in the lattice
- Boron is called an acceptor

3 p-n Junctions

- Connect a p-type semiconducotr and a n-type semiconductor.
- The free electrons in the n-type diffuse across to fill the p-type holes.
- This leaves negative ions in the p-type semiconductor and positive ions in the n-type semiconductor. This region is called the **space-charge/ depletion region**
- The space-charge region causes an electric field to form which stops further diffusion from happening
- Acts as a diode, as the reverse bias allows no current through, but the forward bias does

3.1 Reverse Biased p-n Junction

- Connect the **positive** terminal to the **n-type** and the negative to the p-type terminal
- Therefore free electrons in the n-type are attracted to the positive and the holes are attracted to the positive.
- This means that the depletion region is increased
- As a result there is very little current through the junction

3.2 Forward Biased p-n Junction

- Connect the **positive** terminal to the **p-type** and the negative to the n-type terminal
- This means the electrons in the n-type are repelled away from the terminal and the holes are repelled from the terminal, causing the holes and the electrons to be pushed into the middle
- As a result the depletion zone is decreased.
- There is a large current across the junction as the associated field is small

4 Circuit Theory

- The greater the resistance, the larger the potential difference
- Ohms law: $V = IR$
- An ohmic conductor is one where V is proportional to I
- **Resistors** are conductors that are made to have a specific resistance.
- Kirchhoff's Laws[:

  Current Law: The sum of currents entering a junction is zero

  Voltage Law: The sum of directed potiential differences around a closed loop is zero
- Potential Dividor Formula: $V_x = V(\frac{R_2}{R_1+R_2})$ - Voltage at a point x betweem component 1 and component 2, for a linear circuit
- Can be done using a graph approach - for component 1, which is connected to 0Vs, plot current as you increase voltage along the x axis. For component 2, start from the other end of the x axis and increase voltage, but plot current against $totalvoltage - v$. Where the two lines intersect, that's the voltage between the two components.
  This can also be applied to non-linear components

5 MOSFETS

Metal Oxide Semiconductor Fiedl Effect Transistor
In this way, the gate of the FET controls the flow of carriers (electrons or holes) flowing from the source to drain. It does this by controlling the size and shape of the conductive channel.

- A FET is a three terminal device that uses an electric field to control the current through a device
- Consists of a semiconductor channel with electrodes at either end - drain and source
- Control electrode - the gate - close to the channel and therefore the electric charge can affect it
- The gate controls the flow of electrons/holes by controlling the size and shape of the channel

6 n-channel MOSFET

- p-type body, with two highly doped n-type regions (n+)
- Drain connected to V_D and sink connected to 0
- When G is connected to 0 the transistor is **off**

- When G is raised to a positive voltage, say V_G then the G plate is positively charges, so the electrons can form a channel between S and D, allowing there to be a current
- There is a threshold V_G for this to occur
- Electrons diffuse faster than holes

6.1 n-Characteristics

- Plotting V_DS against current for different V_G shows that as V_DS increases , for V_G above a certain level, current increases greatly as well. Below the certain V_GS the current is close to zero, however much you increase V_DS

7 p-channel MOSFET

- n-type body, with two highly doped p-type regions (p+)
- Drain connected to 0 and sink connected to V_D
- When G is connected to V_S the transistor is **off**
- This is because the G plate is positively charged and therefore the holes in the p-type regions are repelled from the plate
- When G is lowered to a zero voltage, then the G plate is relatively negatively charged, and therefore a channel forms, and the holes are able to diffuse across, and therefore there is a
- Overall, when G is connected to a voltage there is no current, but when connected to zero there is a a current

8 n-MOS

(How i think they work...not really sure)

- One terminal connected to ground, one terminal connected to V_DD
- Output near V_DD
- When the input is 0, the G plate doesnt connect the two terminals, and therefore the output is connected to V_DD and shows an output of 1
- When the input is 1, the G plate connects the two terminals and therefore output is grounded, and has a reading of $0V$, giving an output of 0
- Therefore this acts as an inverter
- However the n-mos doesnt have total binary behaviour - needed for an inverter, it is more gradual and changes over a range
- n-mos isn't really used for logic gates because:

  Low speed of operation - due to stray capacitance as a result of the extra metal plates needed to connect input and output

  Power of consumption

9 Capacitor

- A device that stores energy
- Two metal plates separated by a non-conductor, therefore charge builds up until it is released, when the non-conductor is released
- $Q = VC$ where Q = charge stored in capacitor, V = voltage, C = capacitance (constant)
  Current is the rate of flow of charge - $\frac{dQ}{dt} = I$, $Q = \int I dt$
  $V = \frac{1}{C} \int I dt$
- Capacitor Equations, where $I_0 = \ln(\frac{V_D D}{R_1})$

  Current Charging: $I = I_0 e^{\frac{-t}{CR_1}}$

  Voltage Charging: $V = V_D D(1 - e^{\frac{-t}{CR_1}})$

  Voltage Discharging: $V = V_D D e^{\frac{-t}{CR_2}}$

  CR - is a time constant, with units seconds and is different for each resistor

10 Complementary MOS (CMOS)

- Both p and n channel MOS transistors are used
- p-mos transistor is an n-mos transistor but with polarities reversed
- A CMOS Inverter has much more binary behaviour compared to just the n-mos.
- Only dissipates power when switching
- Can make logic gates from CMOS, e.g. a NAND gate requires 2 CMOSes

11 Noise Margins

- Signals between input and outputs are susceptible to corruption by noise - as they are analogue and not completely binary
- Tolerance to noise is quantified by **noise margins**
- Logic 0 Noise Margin = $V_I L(max) - V_O L(max)$
- Logic 1 Noise Margin = $V_O H(max) - V_I H(max)$

12 Analogue vs Digital

ADCs and DACs are used to convert between analogue and digital signals. Need to consider:
Conversion Speed
Resolution
Power Consumption

12.1 ADCs

- Regular sampling every T seconds
- These samples are still analogue so constrain them to only take one of M possible amplitude values
- Each discrete amplitude level is given a n-bit binary code
- For a n-bit ADC there are $M = 2^n$ amplitude levels

Trade off between the number of amplitude levels (lower the quantisation error) and the bit rate (makes it slower)
Nyquist Rate - sample rate must be at least twice the highest frequency in the analogue signal being sampled. If not satisfied the signal will be subject to alias distortion.
First passed through a low filter to remove anything above the max freq wanted
Amplification of the analogue signal is required to ensure the digital signal is not of poor quality

12.2 DACs

Converts digitized sample back to analogue
Following the DAC low pass filters and amplifiers are used

13 Operational Amplifiers

Have two inputs, and a single ouput
Used for different operations in the cicuit - amplifying signals, adding, subtracting, filters etc
Assume - infinite input resistance and infinite gain
Types:

- Inverting Amplifier: Voltage gain: $\frac{V_out}{V_in} = -\frac{R_2}{R_1}$
- Non-inverting Amplifier: $\frac{V_out}{V_in} = 1 + \frac{R_2}{R_1}$
- Buffer Amplifier: $\frac{V_out}{V_in} = 1$ - unity gain

Op-amps use split power supplies - +ve and -ve connections