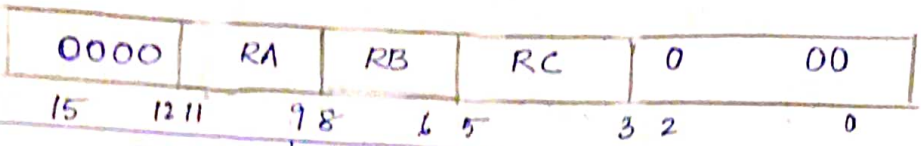
EE-224 PROJECT

(1) ADD
SUB
MUL



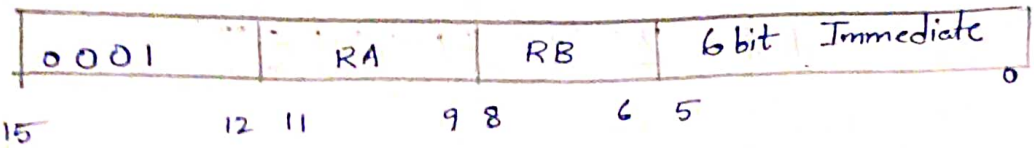
S1	PC ⟶ M_Address	
	M_data ⟶ IR PC ⟶ ALU:A +2 ⟶ ALU_B ALU_C ⟶ PC	Memory_Read Add IR write PC W
S2	IR_{7-11} ⟶ RF_A1 IR_{6-8} ⟶ RF_A2 RF_D1 ⟶ T1 RF_D2 ⟶ T2	T1-W T2-W 1
S3	T1 ⟶ ALU_A T2 ⟶ ALU_B ALU_C ⟶ T3	Add T3-W
S4	T3 ⟶ RF_D3 IR_{3-5} ⟶ RF_A3	RF_W

GROUP MEMBERS	
K. Yashaswini	22B3911
Pyla Ramya	22B1305
Lokesh Chandra	22B3906
Krishna Kant Naik	22B3934

(2) SUB (0010)

(3) MUL (0011)

(4) ADI



PE $S_1 \rightarrow S_5 \rightarrow S_3 \rightarrow S_6$

S5

$IR_{9-11} \rightarrow RFA1$ $IR_{0-5} \rightarrow SE6 \rightarrow T2$ $RFD1 \rightarrow T1$	T_1-W T_2-W

S6

$T3 \rightarrow RFD3$ $IR_{6-8} \rightarrow RFA3$	RF_W

(5) AND (0100)

$S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$

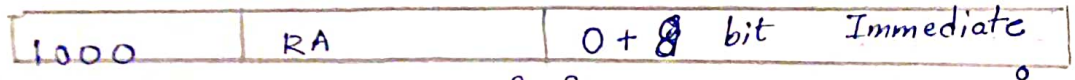
(6) ORA (0101)

$S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$

(7) IMP (0110)

$S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$

(8) LHI



$S_1 \rightarrow S_7$

S7

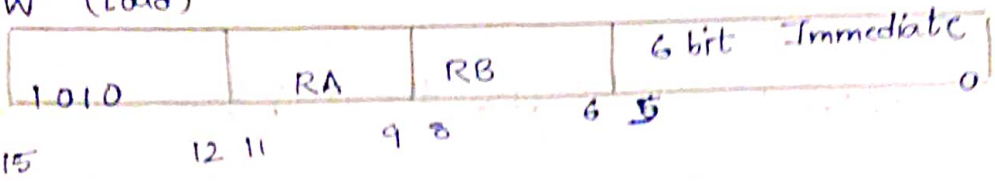
$IR_{0-8} \rightarrow$ Data Extension $\rightarrow RFD3$ $IR_{9-11} \rightarrow RFA3$	RF_W

RA = IM9 0000000

(9) LLI (1001)

RA = 0000000 Im9

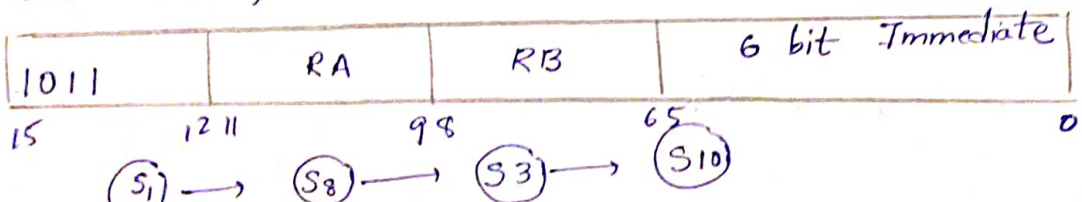
(10) LW (Load)



S8	$IR_{6-8} \rightarrow RFA2$ $IR_{0-5} \rightarrow SEG \rightarrow T2$ $RFD2 \rightarrow T1$	T_1-W T_2-W

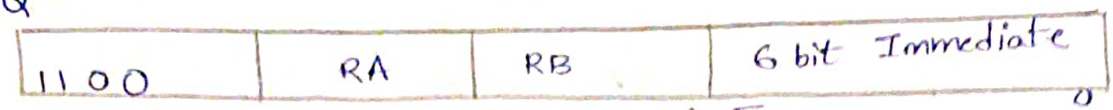
S9	$T3 \rightarrow Mem\_Address$ $Mem\_data \rightarrow RFD3$ $IR_{9-11} \rightarrow RFA3$	Memory R RF_W

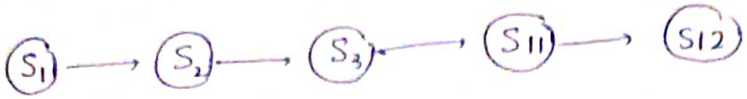
(11) SW (store)



S10	$IR_{9-11} \rightarrow RFA1$ $RFD1 \rightarrow Mem\_data$ $T3 \rightarrow Mem\_address$	RF_R Memory-Write

(12) BEQ





S_3 (subtraction and modifies the zero flag)

(Z = 1) (Z = 0) next instruction

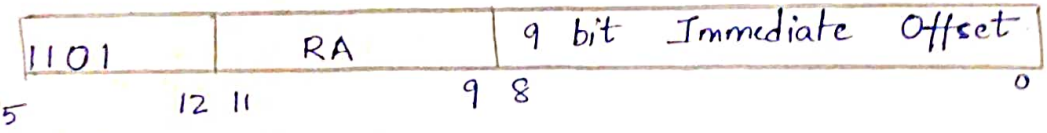
S11

PC → ALU_A (shift by 1)	PC_W
IR_{0-5} → SEG → ALU_B	Add
ALU_C → PC	

S12

PC → ALU_A	PC_W
-2 → ALU_B	Add
ALU_C → PC	

(13) JAL



S13

PC → ALU_A (shift by 1)	PC_W
IR_0_8 → SE9 → ALU_B	Add
ALU_C → PC	

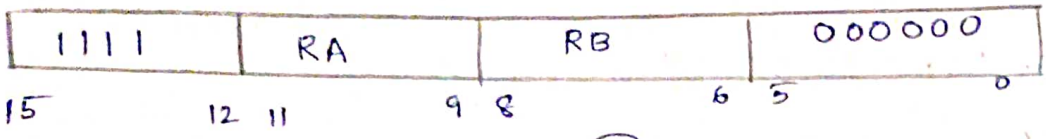
S14

PC → ALU_A	PC_W
-2 → ALU_B	Add
ALU_C → PC	

S15

PC → RF_D3	RF_W
IR_{9-11} → RFA3	

JLR

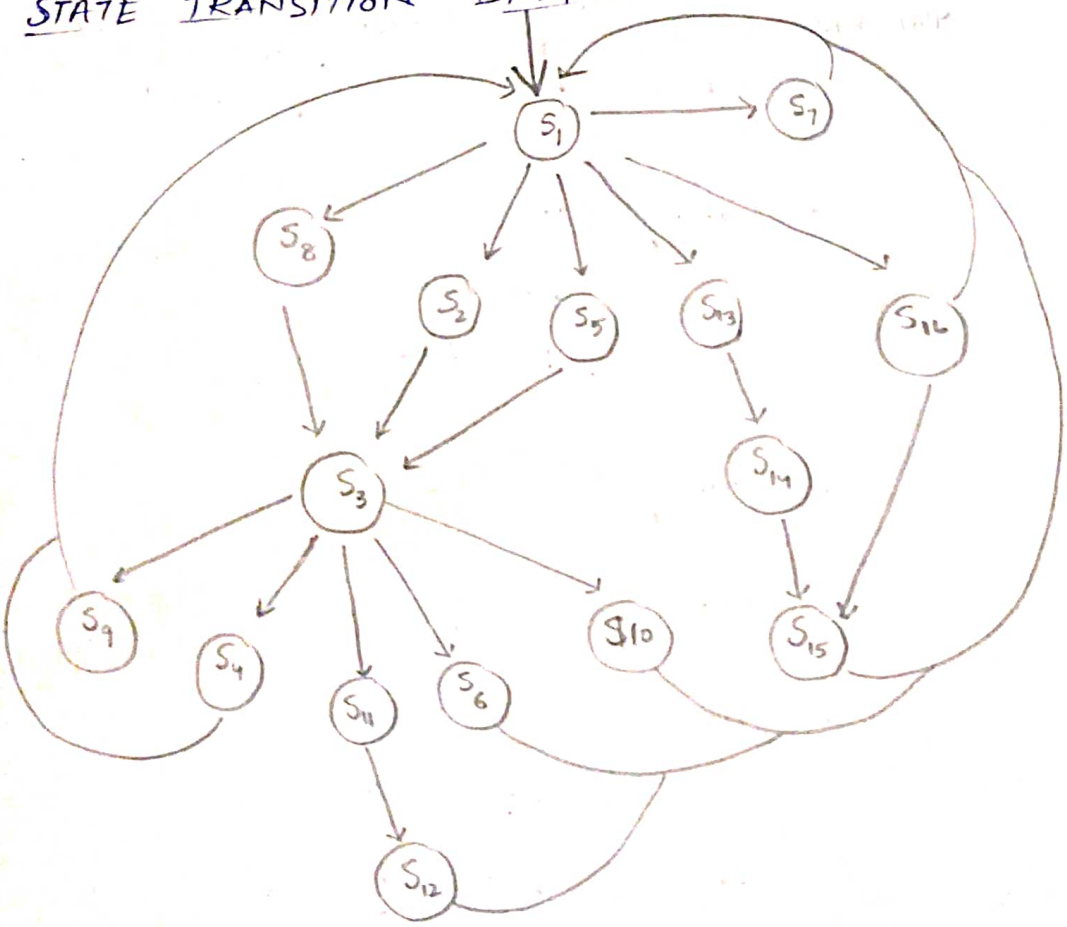


S16

$IR_{6\to8}$ → RFA2 RF_D2 → PC	PC_W

PC → P

STATE TRANSITION DIAGRAM :



CONNECTIONS

* to RFA1 and RFA2

IR_{9-11} ⟶ RFA1

IR_{6-8} ⟶ RFA2

* ~~Cor~~ to RF_A3

IR_{3-5} ⟶ RF_A3 00

IR_{6-8} ⟶ RF_A3 01

IR_{9-11} ⟶ RF_A3 10

* to RF_D3

T3 ⟶ RF_D3 00

IR_0-8 ⟶ DE ⟶ RF_D3 01

Memory_data ⟶ RF_D3 10

PC ⟶ RF_D3 11

* to PC

ALU_C ⟶ PC 0

RF_D2 ⟶ PC 1

* to T1

RF_D1 ⟶ T1 0

RF_D2 ⟶ T1 1

* to T2

RF_D2 ⟶ T2 0

IR_{0-5} ⟶ SE6 ⟶ T2 1

* to T3

ALU_C ⟶ T3

* to ALU_A

PC ⟶ ALU_A 0

T1 ⟶ ALU_A 1

* to ALU_B

T2 ⟶ ALU_B 00

+2 ⟶ ALU_B 01

-2 ⟶ ALU_B 11

IR_0-8 ⟶ SE9 ⟶ shift ⟶ ALU_B 10

IR_0-5 ⟶ SE_6 ⟶ shift ⟶ ALU_B

* Memory_Address

T3 ⟶ Mem_Add 0

PC ⟶ Mem_Add 1

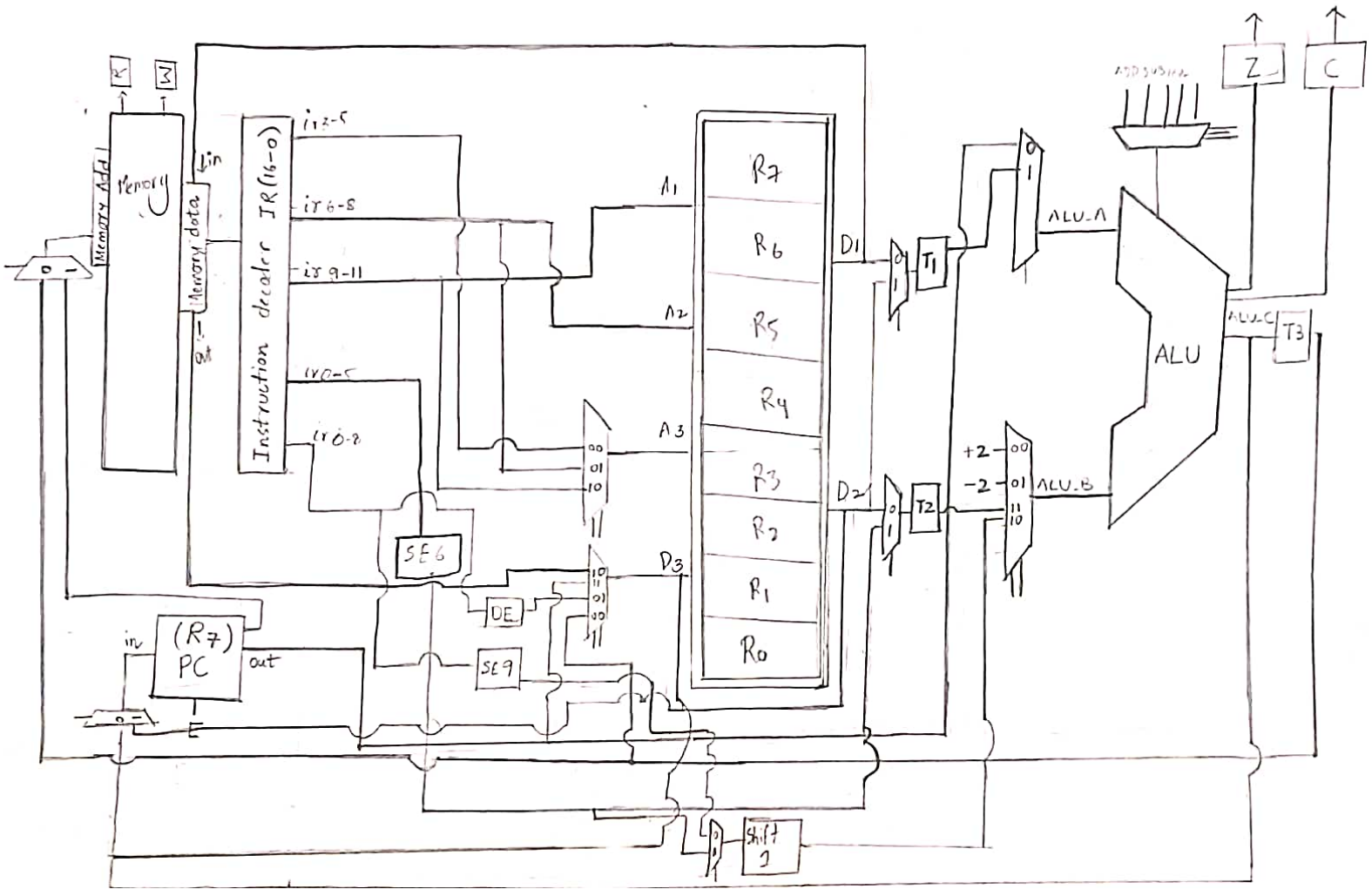
* Memory_data

RFD1 ⟶ Memory_data

* Shift

SE9 ⟶ shift 0

SE6 ⟶ shift 1


R
W
Memory
Memory Add
Memory data
in
out
Instruction decoder IR(16-0)
ir 2-5
ir 6-8
ir 9-11
ir 0-5
ir 0-8
A1
A2
A3
D1
D2
D3
R7
R6
R5
R4
R3
R2
R1
R0
SE6
SE9
DE
(R7)
PC
in
out
T1
T2
T3
+2
-2
ALU.A
ALU.B
ALU.C
ALU
Z
C
Shift
1

	R_Mem	W_Mem	W_PC	WIR	W_RF	RF_A3	RF_D3	PC	T1	T2	ALU_A	ALU_B	Mem_Add	Shift
S1	1	0	1	1	0	xx	xx	0	x	x	0	00	x	x
S2	0	0	0	0	0	xx	xx	x	0	0	x	xx	x	x
S3	0	0	0	0	0	xx	xx	x	x	x	1	11	x	x
S4	0	0	0	0	1	00	00	x	x	x	x	xx	x	x
S5	0	0	0	0	0	xx	xx	x	0	1	x	xx	x	x
S6	0	0	0	0	1	01	00	x	x	x	x	xx	x	x
S7	0	0	0	0	1	10	01	x	x	x	x	xx	x	x
S8	0	0	0	0	0	xx	xx	x	1	1	x	xx	x	x
S9	1	0	0	0	1	10	10	x	x	x	x	xx	0	x
S10	0	1	0	0	0	xx	xx	x	x	x	x	xx	0	x
S11	0	0	1	0	0	xx	xx	0	x	0	x	10	x	1
S12	0	0	1	0	0	xx	xx	0	x	x	0	01	x	x
S13	0	0	1	0	0	xx	xx	0	x	x	0	10	x	0
S14	0	0	1	0	0	xx	xx	0	x	x	0	01	x	x
S15	0	0	0	0	1	10	11	x	x	x	x	xx	x	x
S16	0	0	1	0	0	xx	xx	1	x	x	x	xx	x	x