VLSI Design Project Report

Standard Cell Library Characterization

EE 671: VLSI Design (2024)

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Contents

Chapter 1

Introduction

This project focuses on the comprehensive design, characterization, and verification of three fundamental standard cells: **Buffer (buf)**, **Delay Flip-Flop with positive edge trigger (dfxtp)**, and **2-input NOR with one inverted input (nor2b)**. The cells were meticulously designed using **NGSpice** for circuit simulation and **Magic** for layout creation. Key performance parameters such as timing, power consumption, and input capacitance were thoroughly characterized to ensure optimal functionality and efficiency.

The report is structured into three distinct sections, each dedicated to one of the cells. For each cell, the circuit design, layout, performance characterization, and HDL implementation are detailed, accompanied by simulation results, timing analysis, and power measurements.

Chapter 2

Cell 1: Buffer (buf)

2.1 Circuit Design in NGSpice

2.1.1 Schematic Diagram

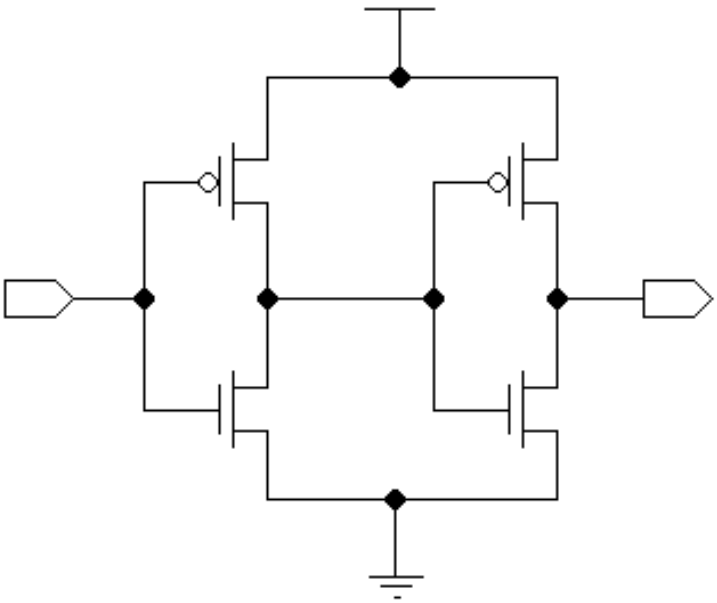


Figure 2.1: Schematic of Buffer

2.1.2 Buffer Specifications

Device	Width (µm)	Length (µm)
NMOS	0.42	0.15
PMOS	0.80	0.15

Table 2.1: Buffer Output Dimensions

2.2 Screenshot of the PEX netlist Buffer

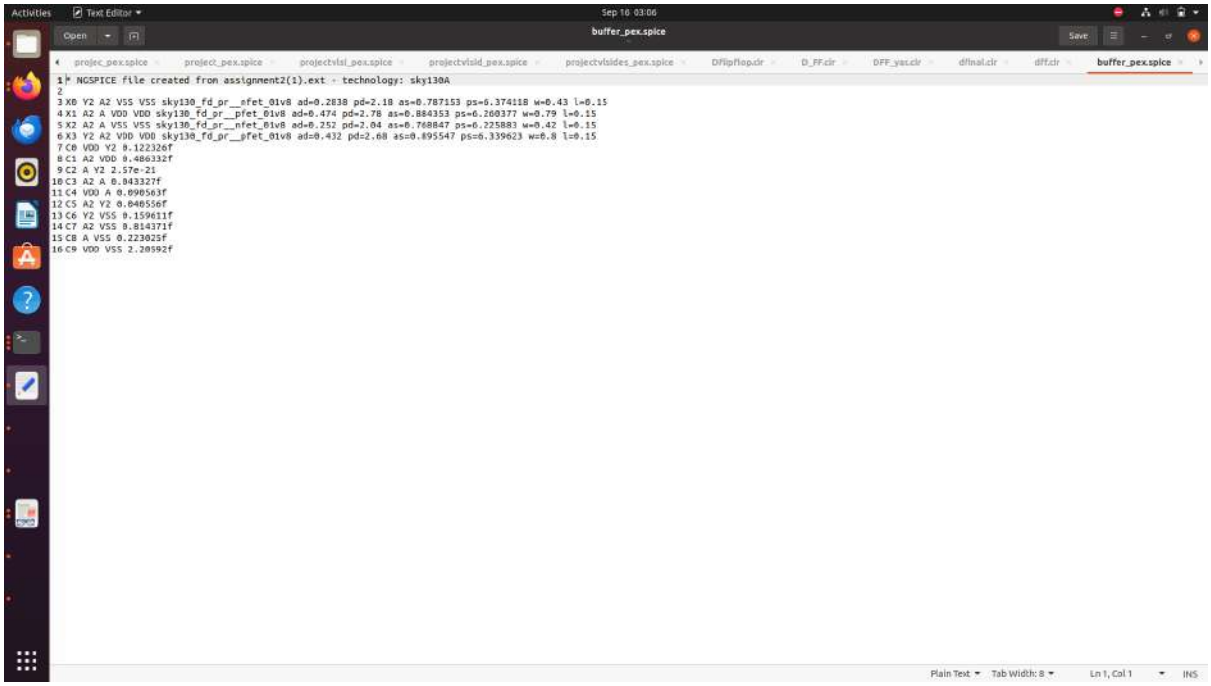


Figure 2.2: Screenshot of the PEX netlist

2.3 Layout Design in Magic

2.3.1 Layout Diagram

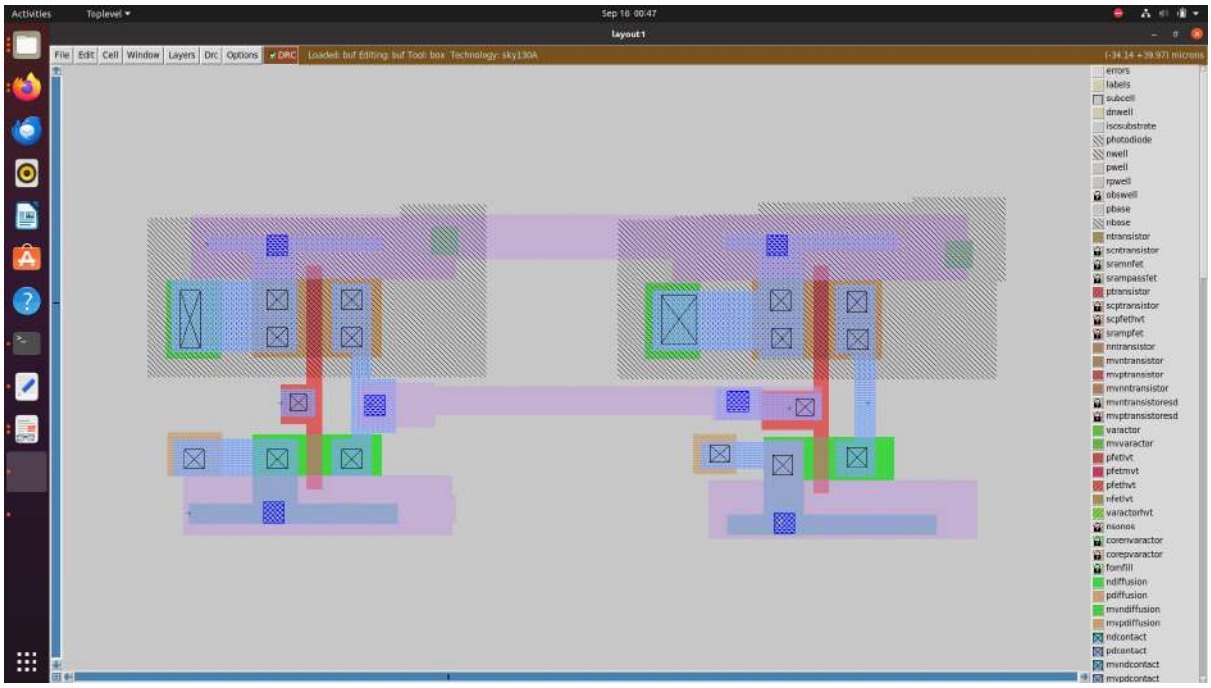


Figure 2.3: Layout of Buffer (buf)

2.3.2 DRC and LVS Verification

The layout was verified against the design rules using DRC and checked for connectivity using LVS.

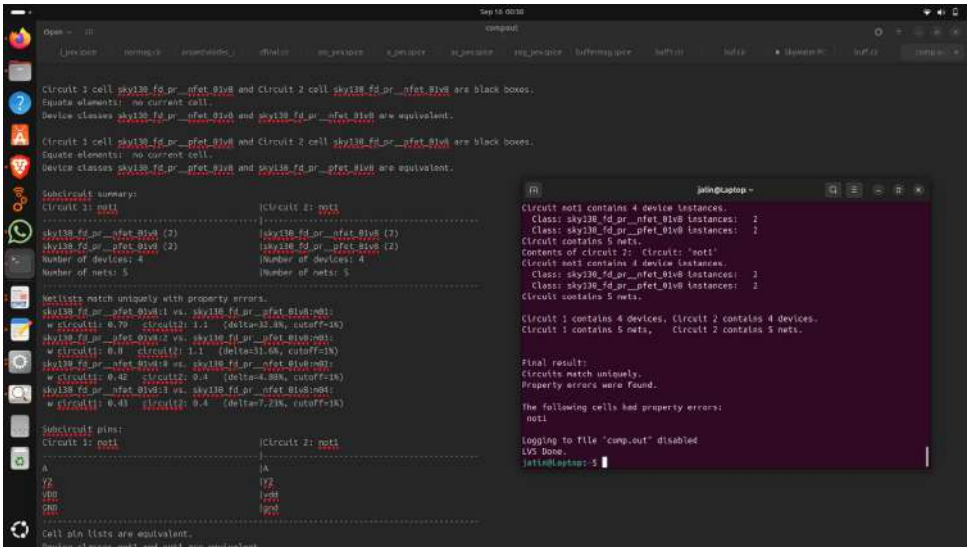


Figure 2.4: LVS Verification for Buffer (buf)

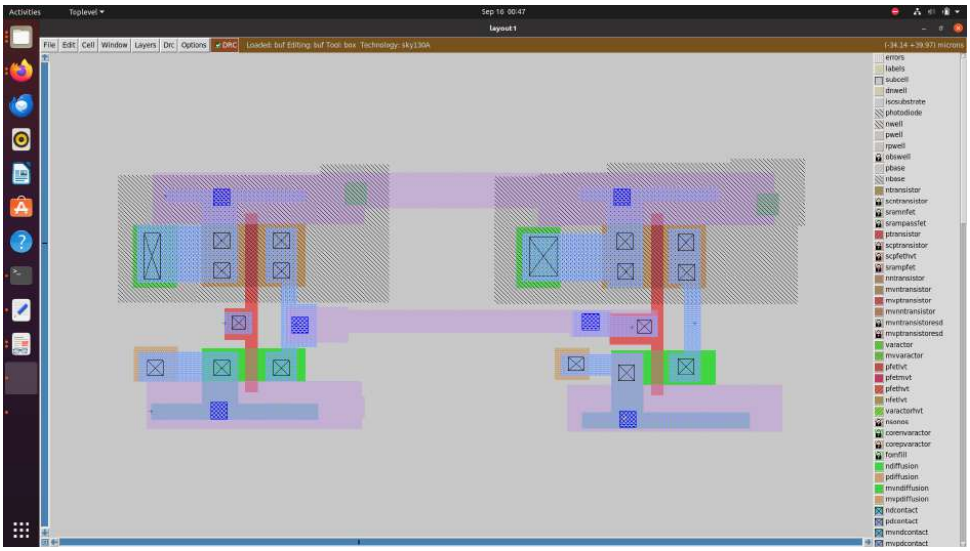


Figure 2.5: DRC Verification for Buffer (buf)

2.4 Timing, Power, and Capacitance Characterization

2.4.1 Input Pin Capacitances

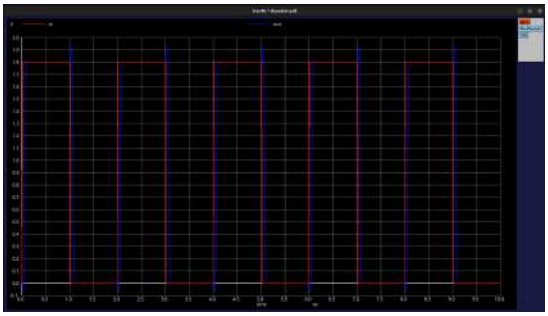
Input Pin	Rise Cap (fF)	Fall Cap (fF)	Average Cap (fF)
A	4.23	3.64	3.935

Table 2.2: Input Pin Capacitances for Buffer (buf)

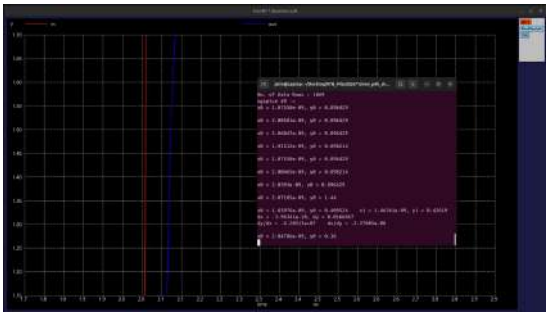
2.4.2 Transition Time Table

Capacitance (fF)	10 ps Slew (ns)	100 ps Slew (ns)	1000 ps Slew (ns)
Output Rise Transitions			
0.5 fF	0.02319	0.02284	0.0395
10 fF	0.10607	0.1095	0.1116
100 fF	0.9377	0.9401	0.938
Output Fall Transitions			
0.5 fF	0.02177	0.020935	0.0373
10 fF	0.09716	0.0985	0.0987
100 fF	0.820	0.845	0.878

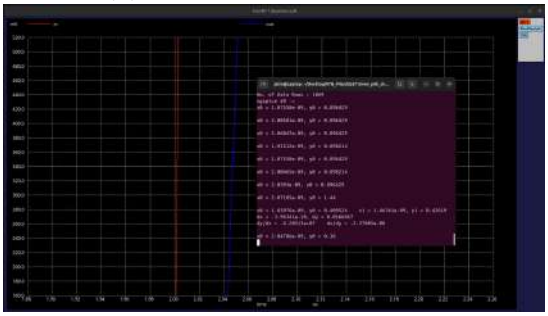
Table 2.3: Transition Time Table for Buffer (buf)



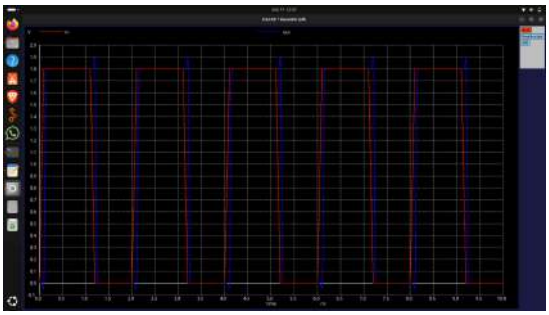
(a) Buffer 0.5f10ps Overall



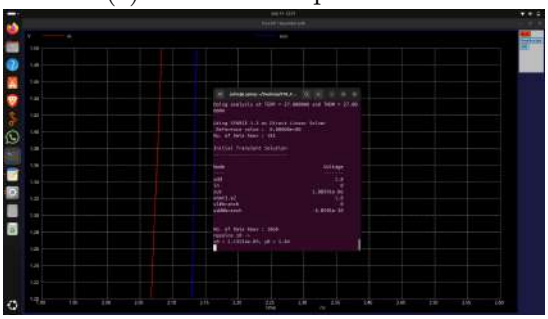
(b) Buffer 0.5f10ps Rise 80



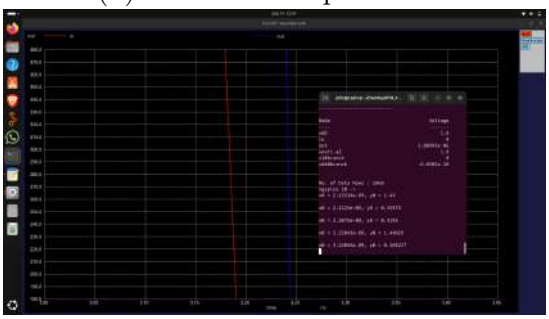
(c) Buffer 0.5f10ps Rise 20



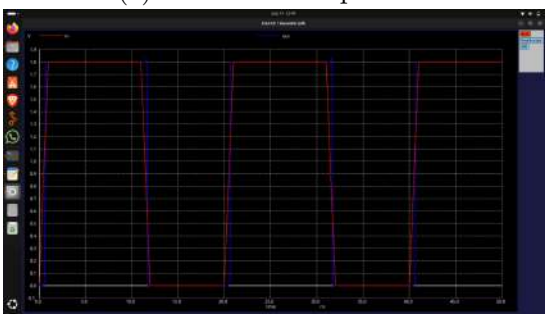
(d) Buffer 0.5f100ps Overall



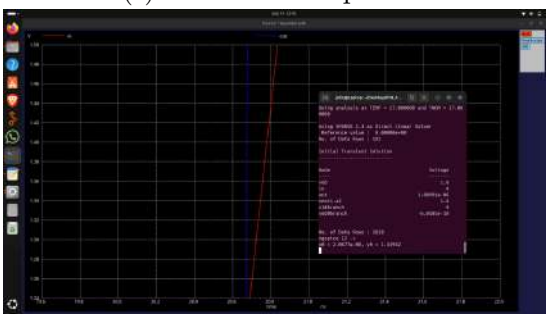
(e) Buffer 0.5f100ps Rise



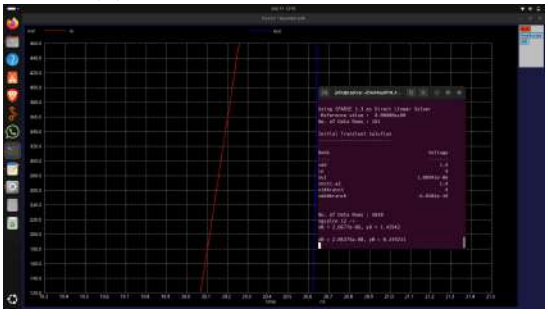
(f) Buffer 0.5f100ps Fall



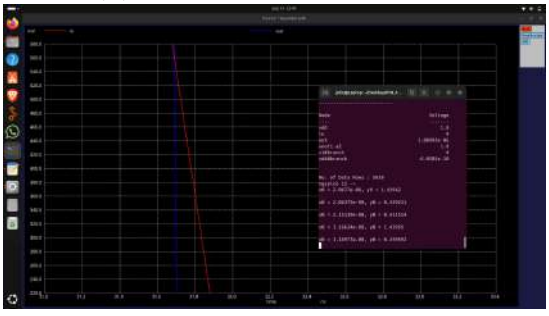
(g) Buffer 0.5f1000ps Overall



(h) Buffer 0.5f1000ps Rise80

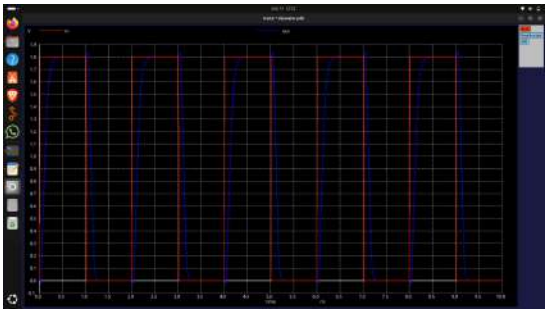


(i) Buffer 0.5f1000ps Rise20

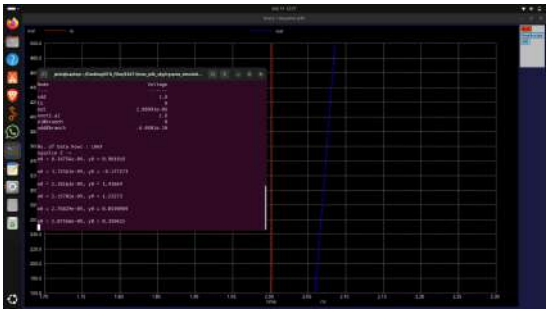


(j) Buffer 0.5f1000ps Fall

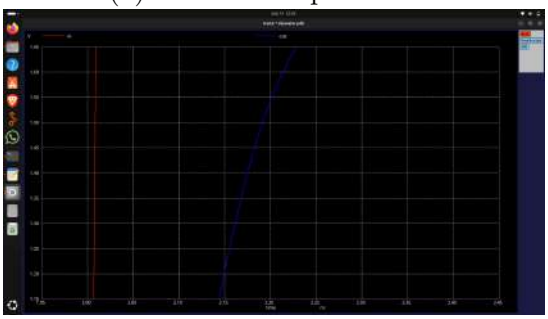
Figure 2.6: Buffer Characterization for 0.5f Capacitance



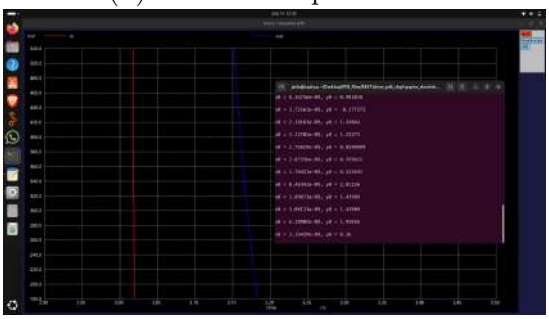
(a) Buffer 10f10ps Overall



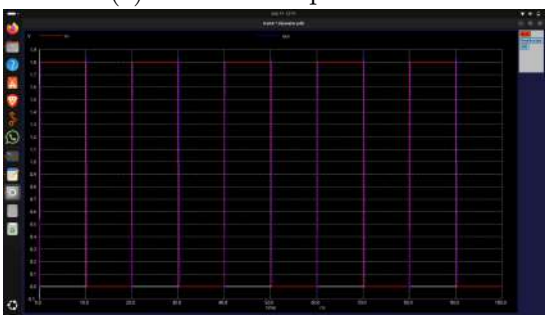
(b) Buffer 10f10ps Rise 80



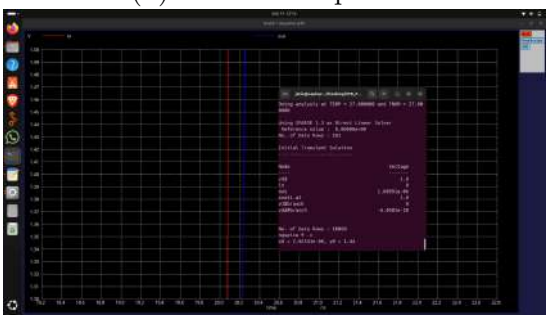
(c) Buffer 10f10ps Rise 20



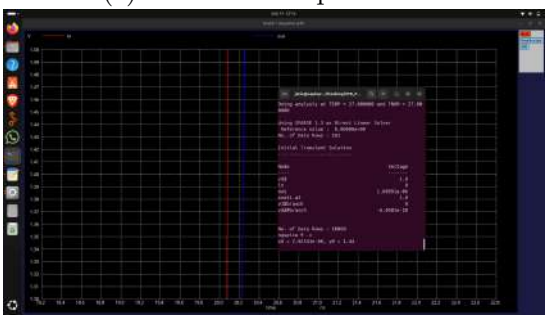
(d) Buffer 10f10ps Fall



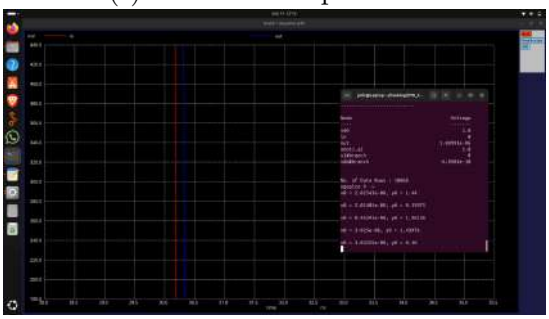
(e) Buffer 10f100ps Overall



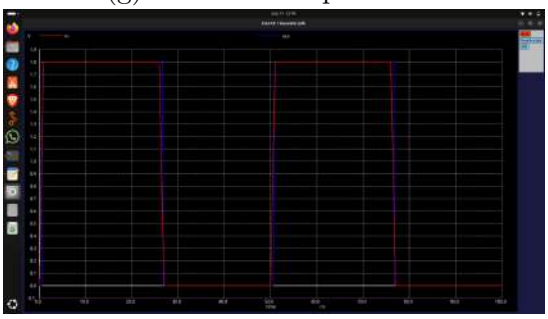
(f) Buffer 10f100ps Rise80



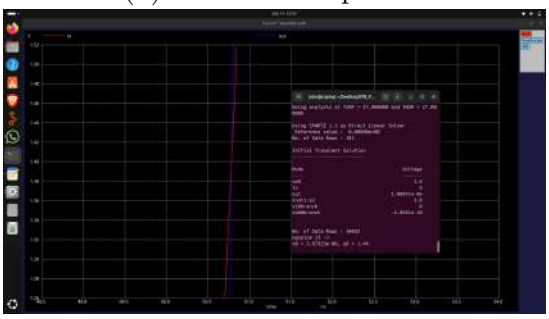
(g) Buffer 10f100ps Rise20



(h) Buffer 10f100ps Fall

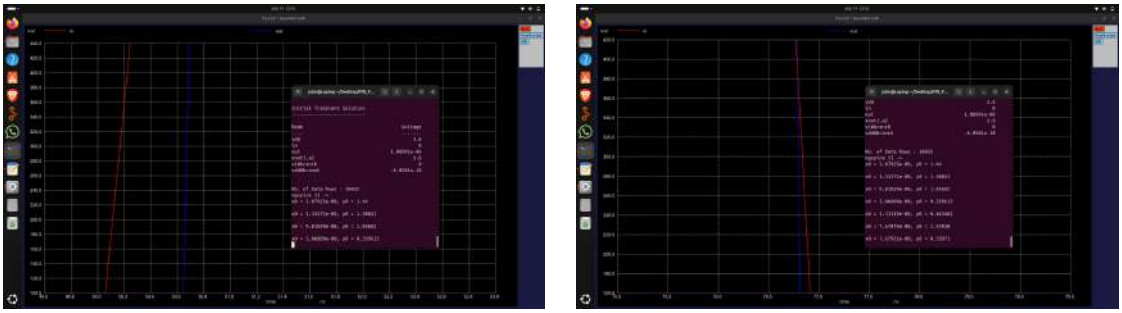


(i) Buffer 10f1000ps Overall



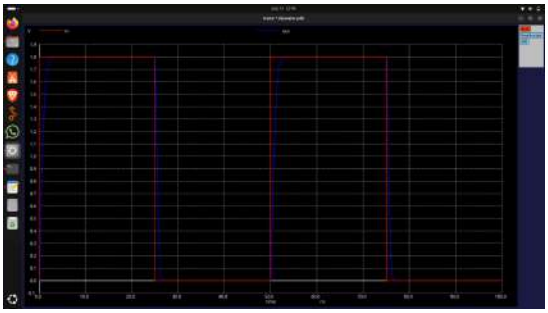
(j) Buffer 10f1000ps Rise80

Figure 2.7: Buffer Characterization for 10f Capacitance

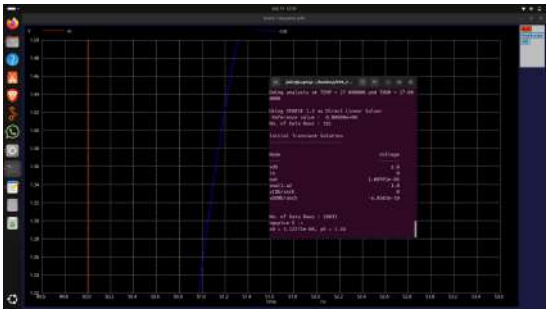


(a) Buffer 10f1000ps Rise20 (b) Buffer 10f1000ps Fall

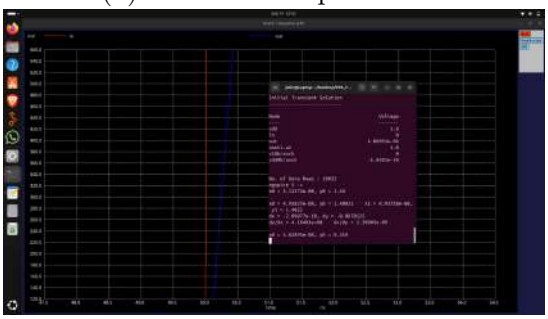
Figure 2.8: Buffer Characterization for 10f Capacitance



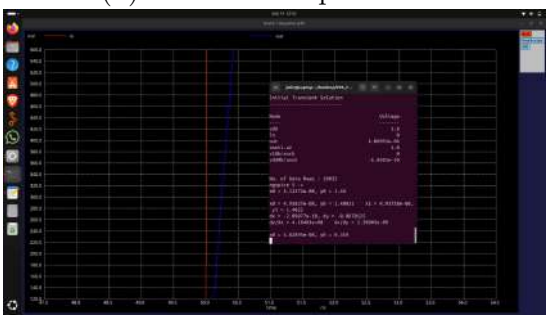
(a) Buffer 100f10ps Overall



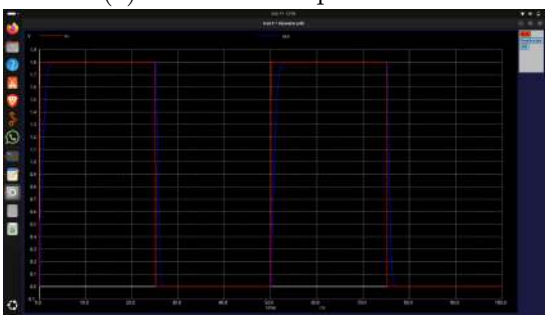
(b) Buffer 100f10ps Rise 80



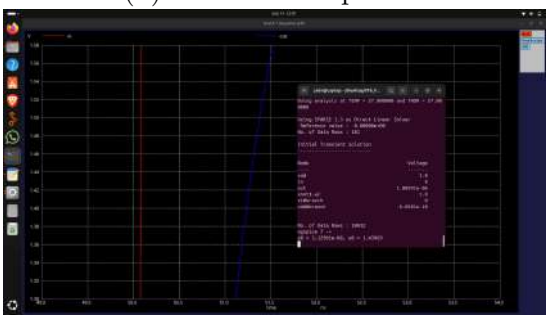
(c) Buffer 100f10ps Rise 20



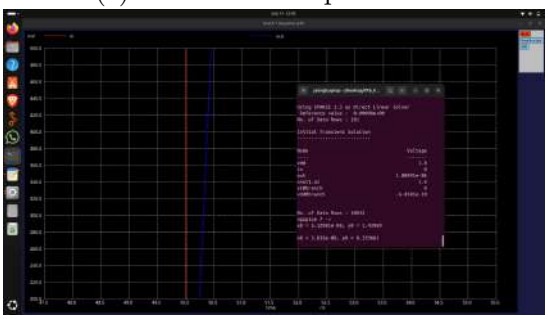
(d) Buffer 100f10ps Fall



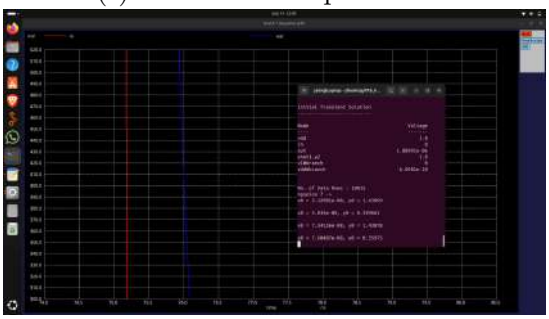
(e) Buffer 100f100ps Overall



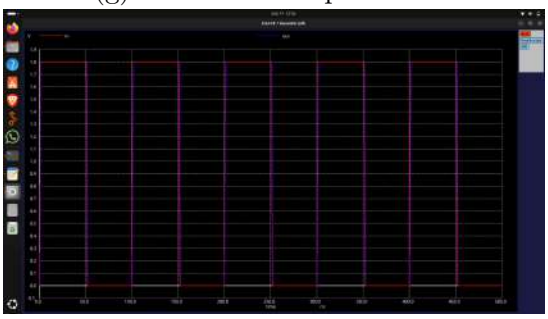
(f) Buffer 100f100ps Rise 80



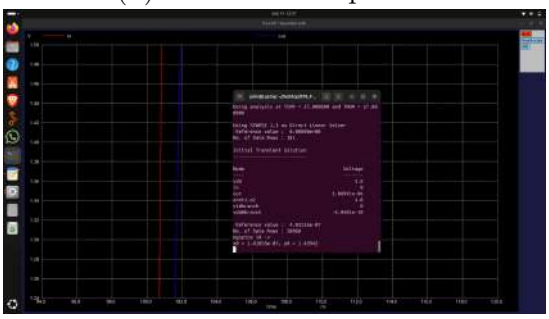
(g) Buffer 100f100ps Rise 20



(h) Buffer 100f100ps Fall

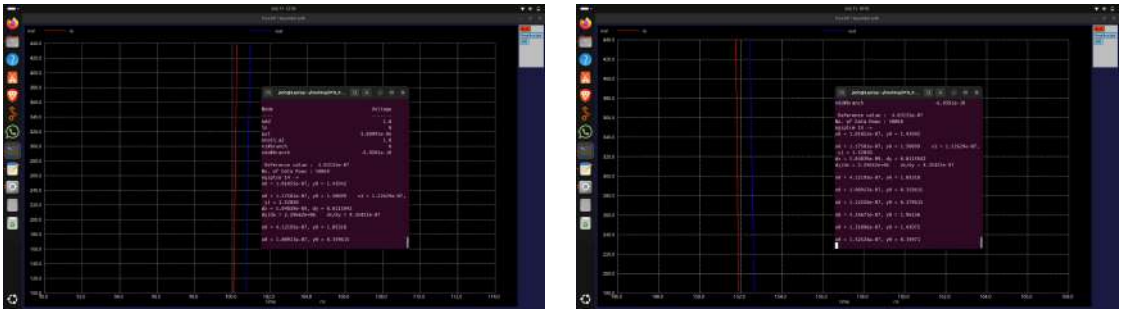


(i) Buffer 100f1000ps Overall



(j) Buffer 100f1000ps Rise80

Figure 2.9: Buffer Characterization for 100f Capacitance



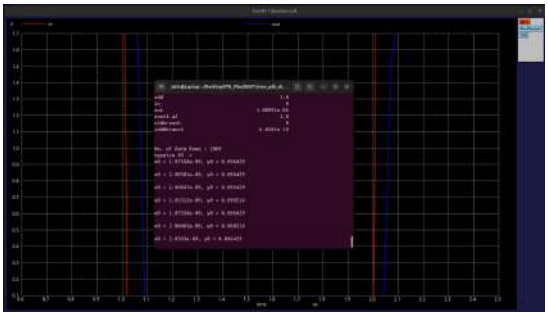
(a) Buffer 100f1000ps Rise20 (b) Buffer 100f1000ps Fall

Figure 2.10: Buffer Characterization for 100f 1000ps Capacitance

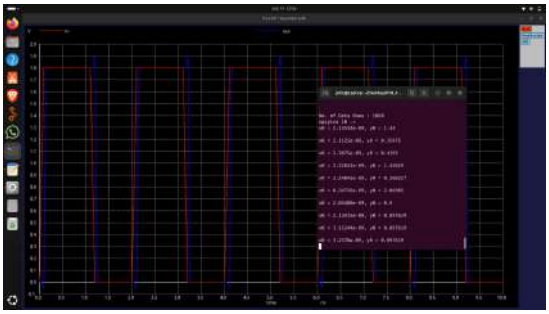
2.4.3 Propagation Delay Time Table

Capacitance (fF)	10 ps Slew (ns)	100 ps Slew (ns)	1000 ps Slew (ns)
Cell Rise Delay			
0.5 fF	0.05465	0.07927	0.15
10 fF	0.11555	0.1369	0.2341
100 fF	0.7158	0.6737	0.851
Cell Fall Delay			
0.5 fF	0.06046	0.08536	0.18
10 fF	0.11333	0.1368	0.2978
100 fF	0.5895	0.5474	0.745

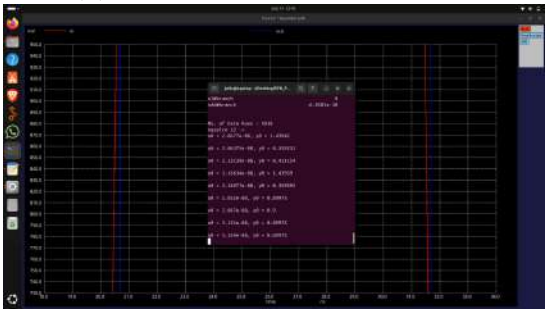
Table 2.4: Propagation Delay Time Table for Buffer (buf)



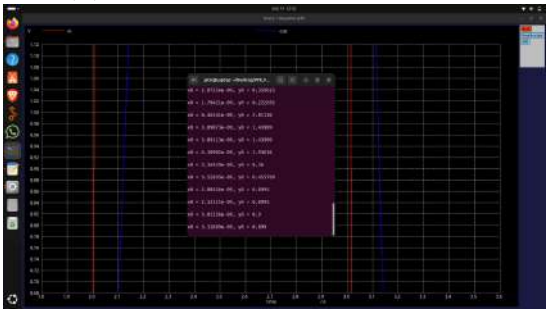
(a) Buffer 0.5f10ps Propagation



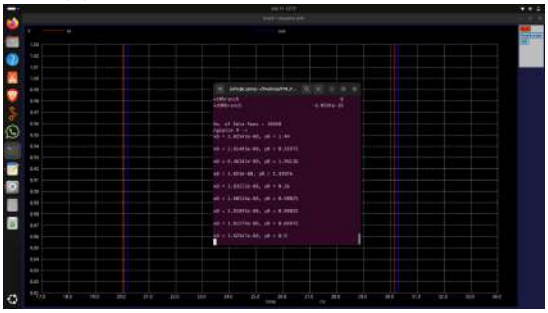
(b) Buffer 0.5f100ps Propagation



(c) Buffer 0.5f1000ps Propagation

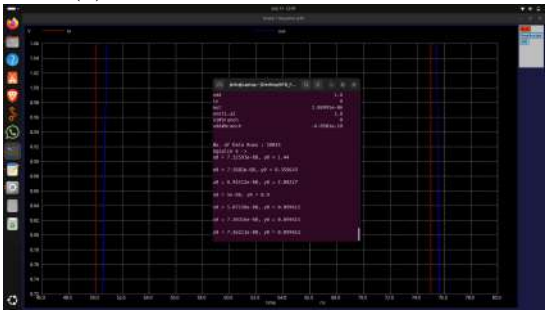


(d) Buffer 10f10ps Propagation

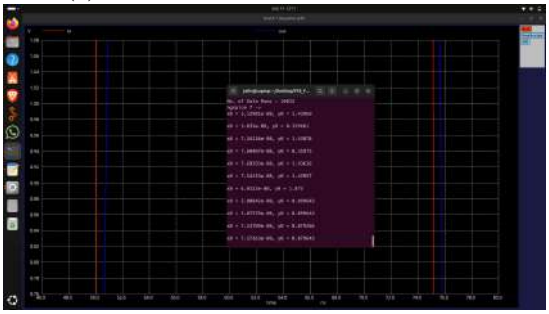


(e) Buffer 10f100ps Propagation

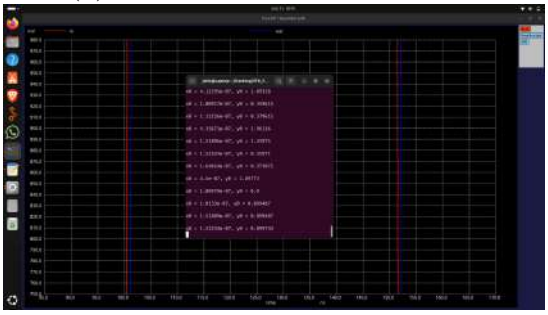
(f) Buffer 10f1000ps Propagation



(g) Buffer 100f10ps Propagation



(h) Buffer 100f100ps Propagation



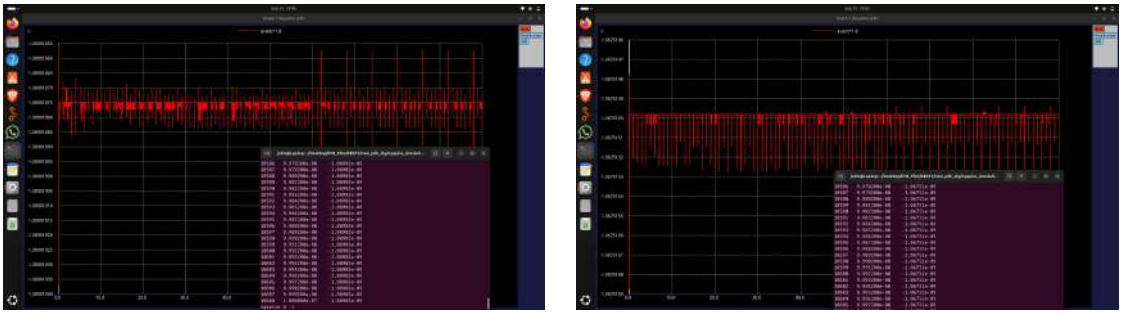
(i) Buffer 100f1000ps Propagation

Figure 2.11: Propagation Delay Simulation for Buffer

2.4.4 Static Power

Condition (A)	Power (nW)
0	1.08902
1	1.06751

Table 2.5: Static Power for Buffer (buf)



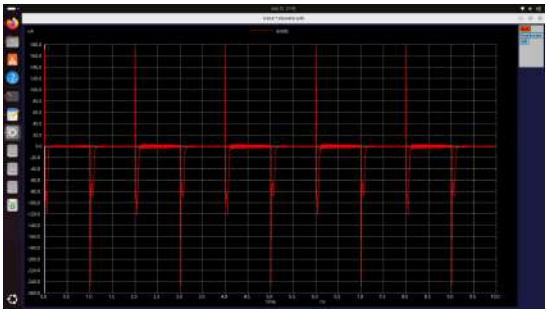
(a) Buffer Condition 0 (b) Buffer Condition 1

Figure 2.12: Static Power Simulation for Buffer

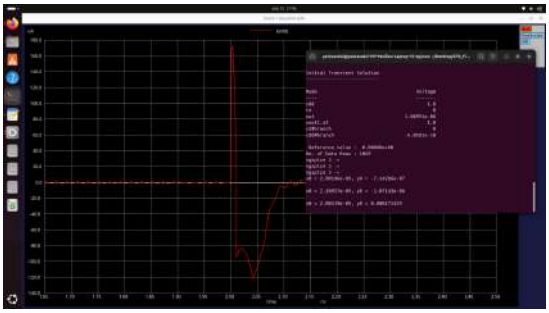
2.4.5 Dynamic Power Table

Capacitance (fF)	10 ps Slew (nW)	100 ps Slew (nW)	1000 ps Slew (nW)
Rise Power			
0.5 fF	16,741	3,500	1,190
10 fF	1,138.79	1,527.93	24,410
100 fF	1,031.4	11,297.2	13,101
Fall Power			
0.5 fF	31,360	16,530	9,180
10 fF	3,674	648.8	8,835.24
100 fF	2,418.6	2,418.6335	1,008.4

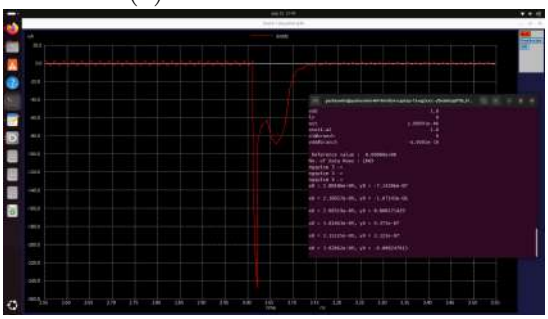
Table 2.6: Dynamic Power Table for Buffer (buf)



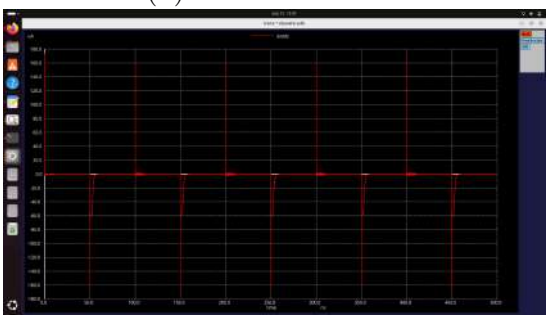
(a) DP0.5f10ns Overall



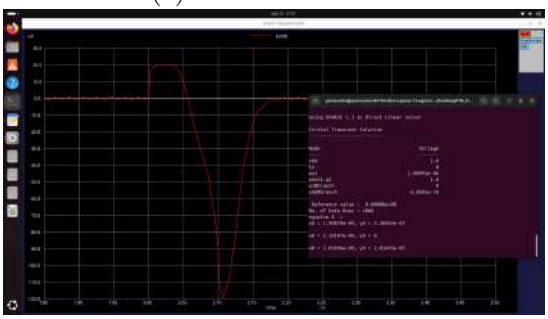
(b) DP0.5f10ns Rise



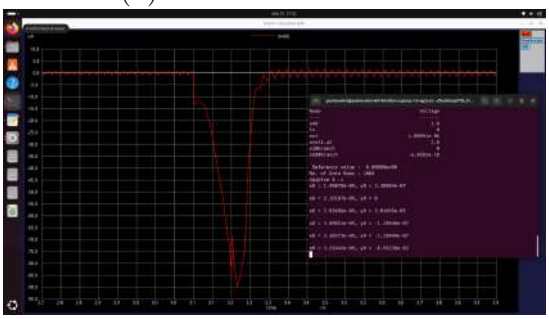
(c) DP0.5f10ns Fall



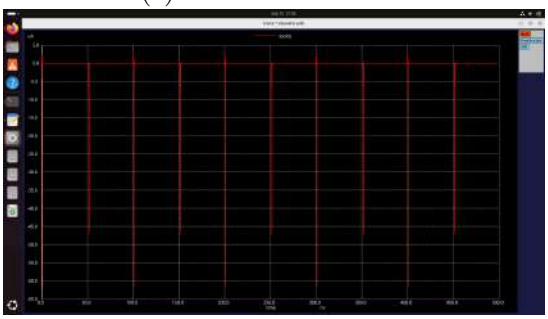
(d) DP0.5f100ns Overall



(e) DP0.5f100ns Rise

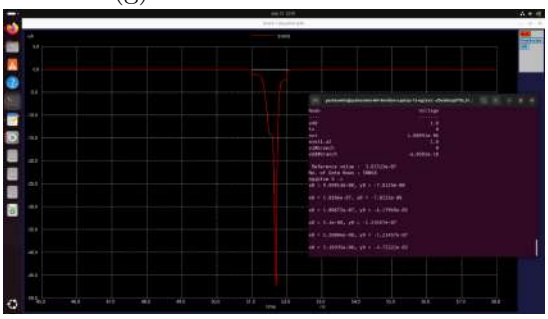


(f) DP0.5f100ns Fall



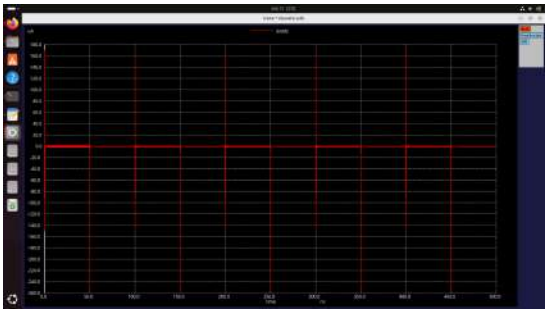
(g) DP0.5f1000ns Overall

(h) DP0.5f1000ns Rise

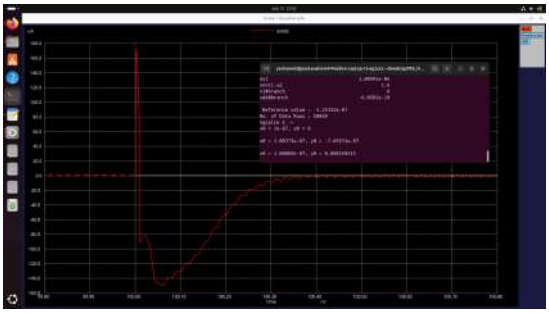


(i) DP0.5f1000ns Fall

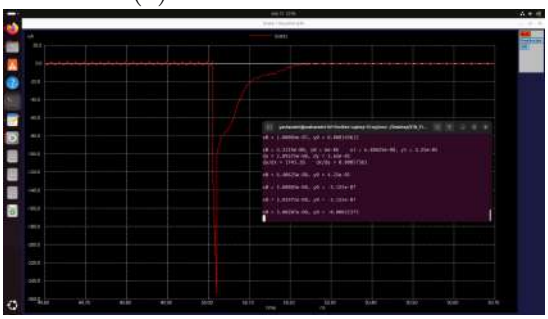
Figure 2.13: Dynamic Power Simulations for Various 0.5fF and various slews



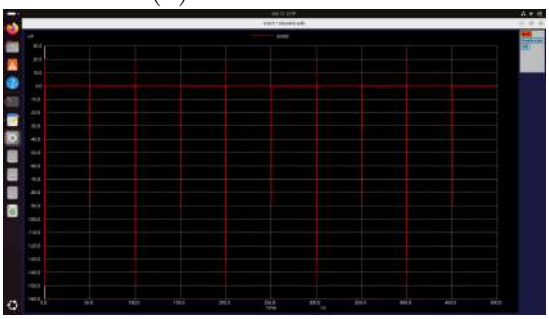
(a) DP10f10ns Overall



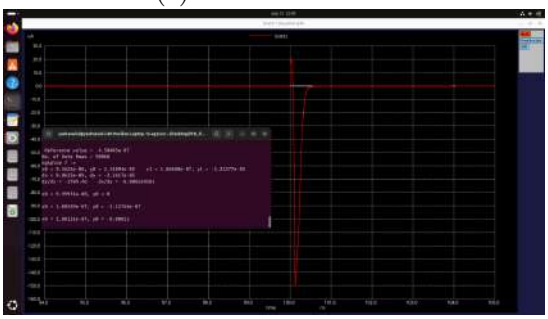
(b) DP10f10ns Rise



(c) DP10f10ns Fall

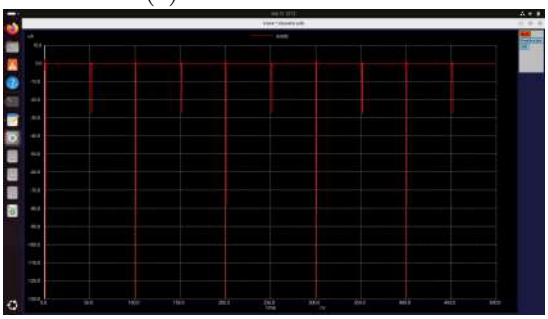


(d) DP10f100ns Overall

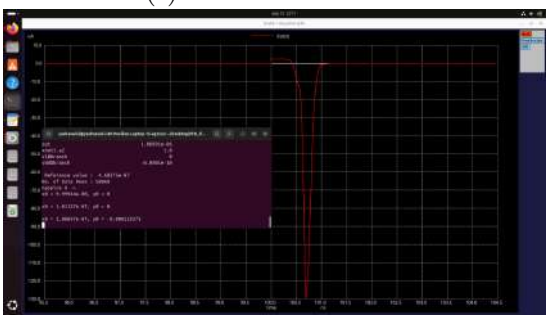


(e) DP10f100ns Rise

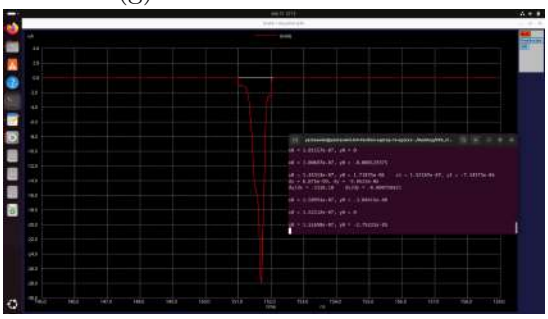
(f) DP10ff100ns Fall



(g) DP10f1000ns Overall

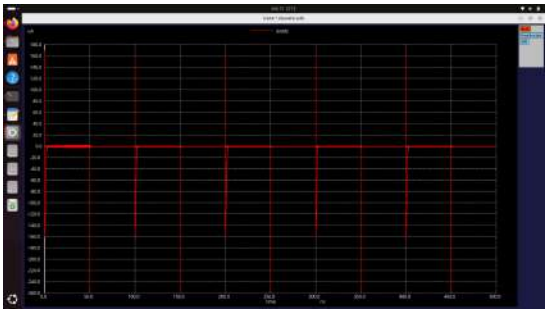


(h) DP10f1000ns Rise

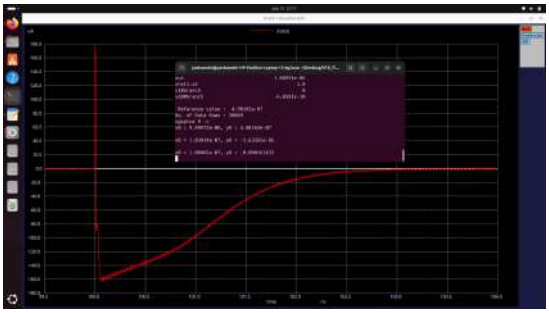


(i) DP10ff1000ns Fall

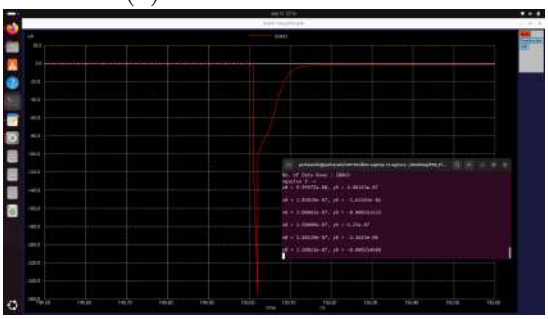
Figure 2.14: Dynamic Power Simulations for Various 10fF and various slews



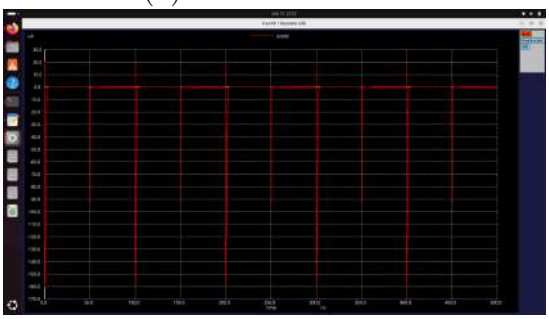
(a) DP100f10ns Overall



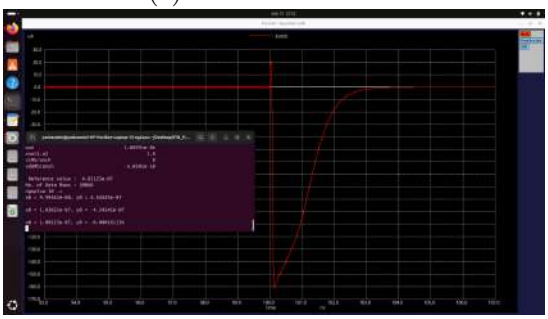
(b) DP100f10ns Rise



(c) DP100f10ns Fall

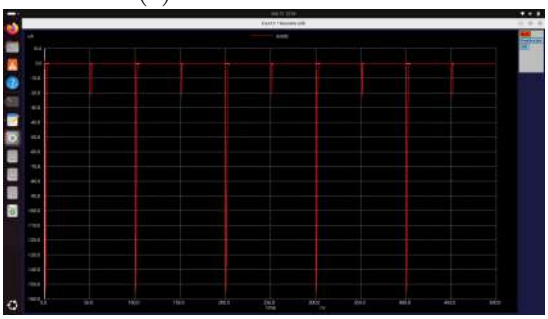


(d) DP100f100ns Overall

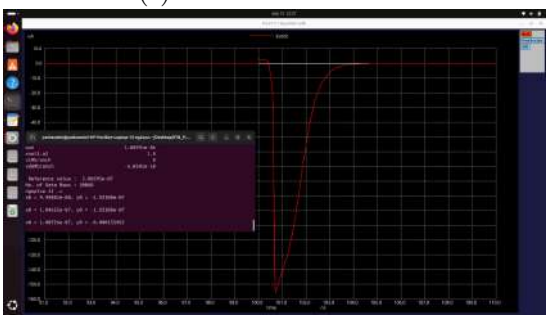


(e) DP100f100ns Rise

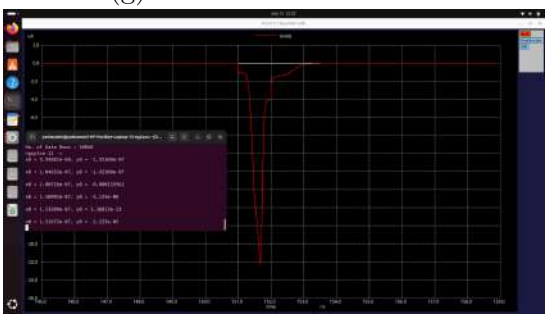
(f) DP100ff100ns Fall



(g) DP100f1000ns Overall



(h) DP100f1000ns Rise



(i) DP100f1000ns Fall

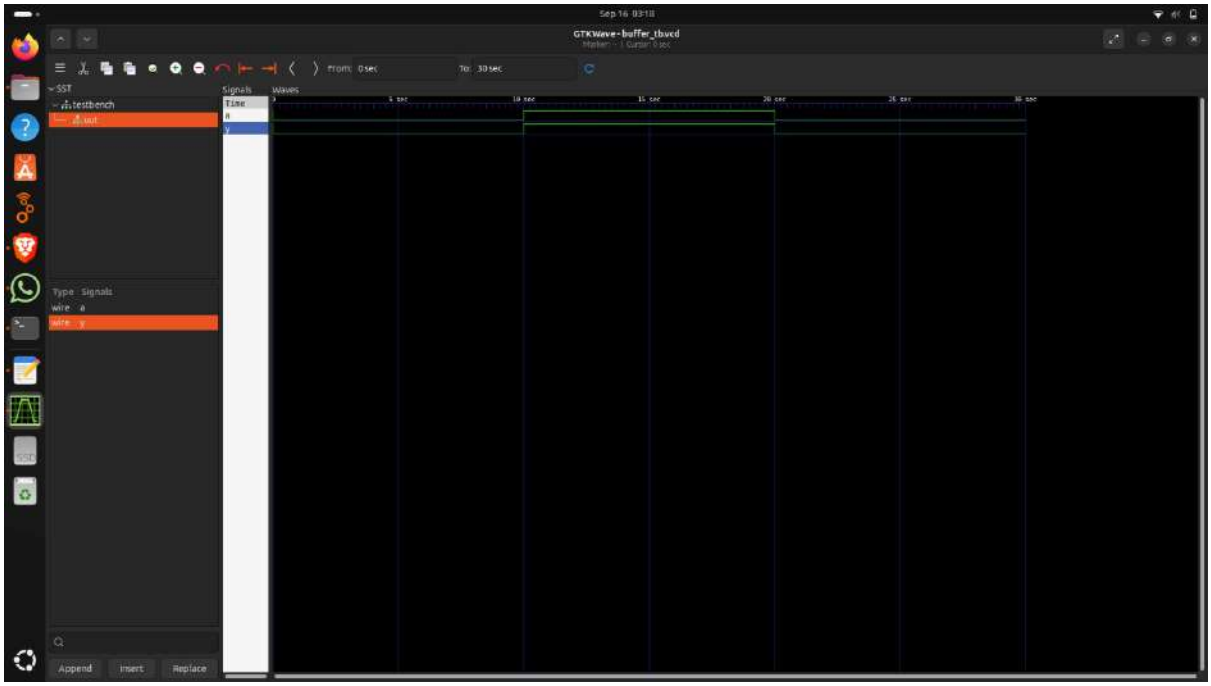
Figure 2.15: Dynamic Power Simulations for Various 100fF and various slews

2.5 HDL Functional Definition

The following Verilog code implements the buffer.

```
module buffer (
    input wire a,   // Input signal
    output wire y   // Output signal (same as input)
);

// Continuous assignment for buffer (just passes input to output)
assign y = a;

endmodule

// Testbench for Buffer
module testbench;

    reg a;          // Input for buffer
    wire y;         // Output from buffer

    // Instantiate the buffer
    buffer uut (
        .a(a),
        .y(y)
    );

    // Test stimulus
    initial begin
        $dumpfile("buffer_tb.vcd");  // Dump file for waveform
        $dumpvars(0, testbench);

        // Test cases
        a = 0; #10;
        a = 1; #10;
        a = 0; #10;

        $finish;
    end

endmodule
```

2.5.1 VHDL Output for Buffer



(a) VHDL Output for Buffer

Figure 2.16: VHDL Output for Buffer

Chapter 3

Cell 2: 2-input NOR with Inverted Input (nor2b)

3.1 Circuit Design in NGSpice

3.1.1 Schematic Diagram

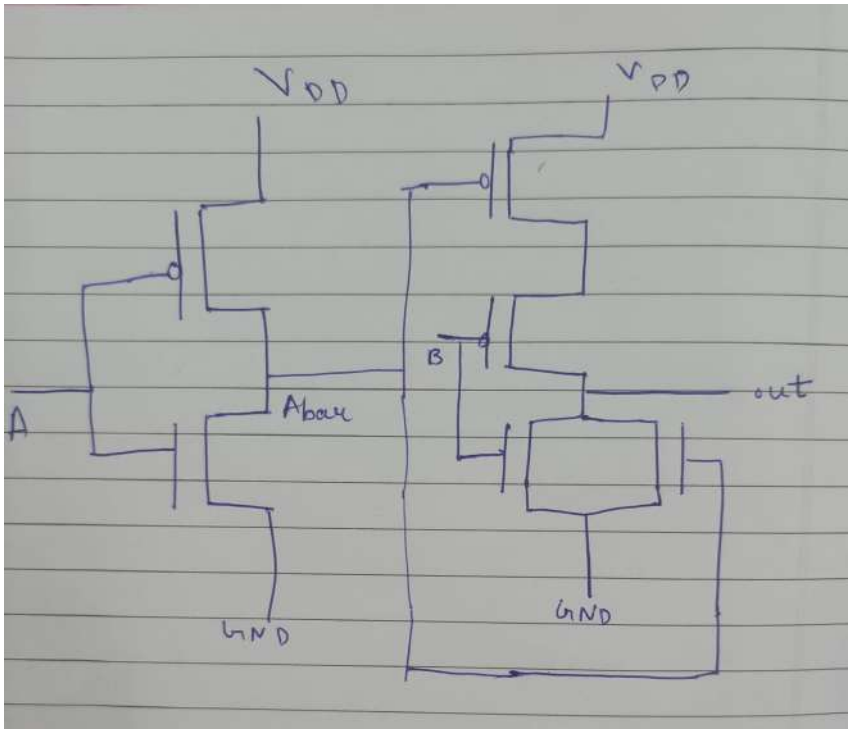


Figure 3.1: Schematic of NOR Gate

3.1.2 NOR Gate Specifications

Device	Width (µm)	Length (µm)
NMOS	0.42	0.31
PMOS	1.55	0.31

Table 3.1: NOR Gate Output Dimensions

3.2 Screenshot of the PEX netlist NOR

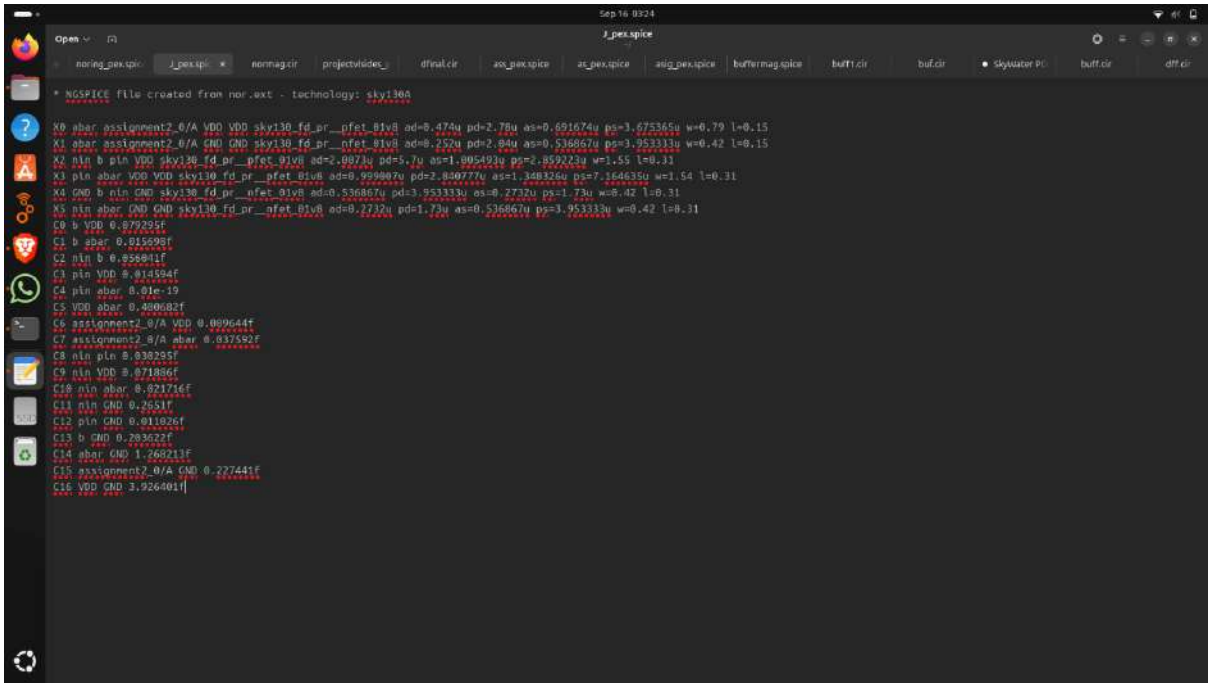


Figure 3.2: Screenshot of the PEX netlist

3.3 Layout Design in Magic

3.3.1 Layout Diagram

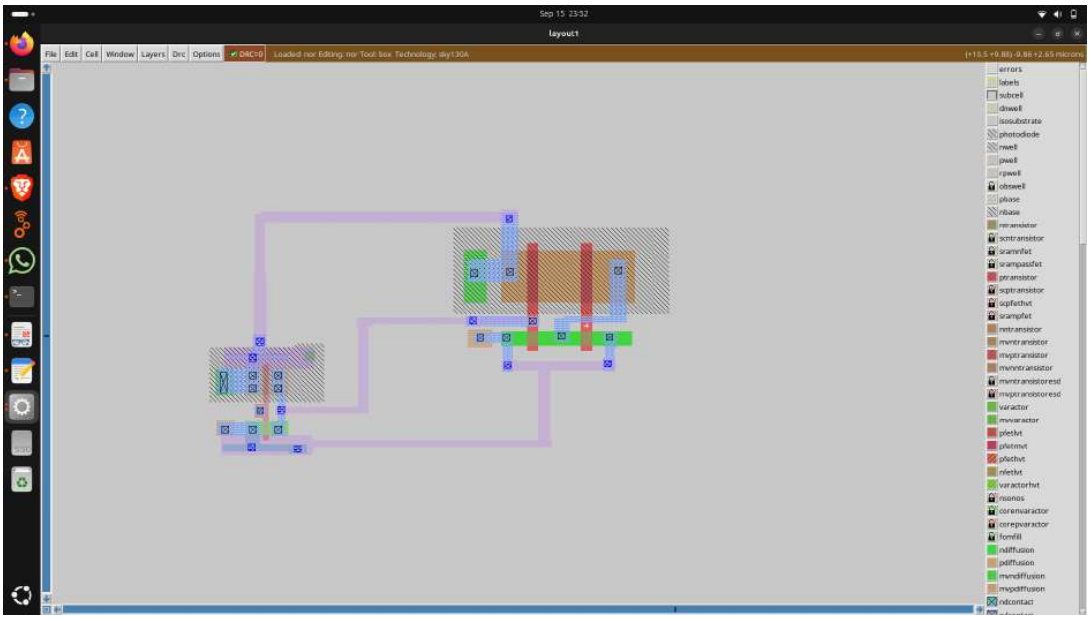


Figure 3.3: Layout of NOR Gate (nor2b)

3.3.2 DRC and LVS Verification

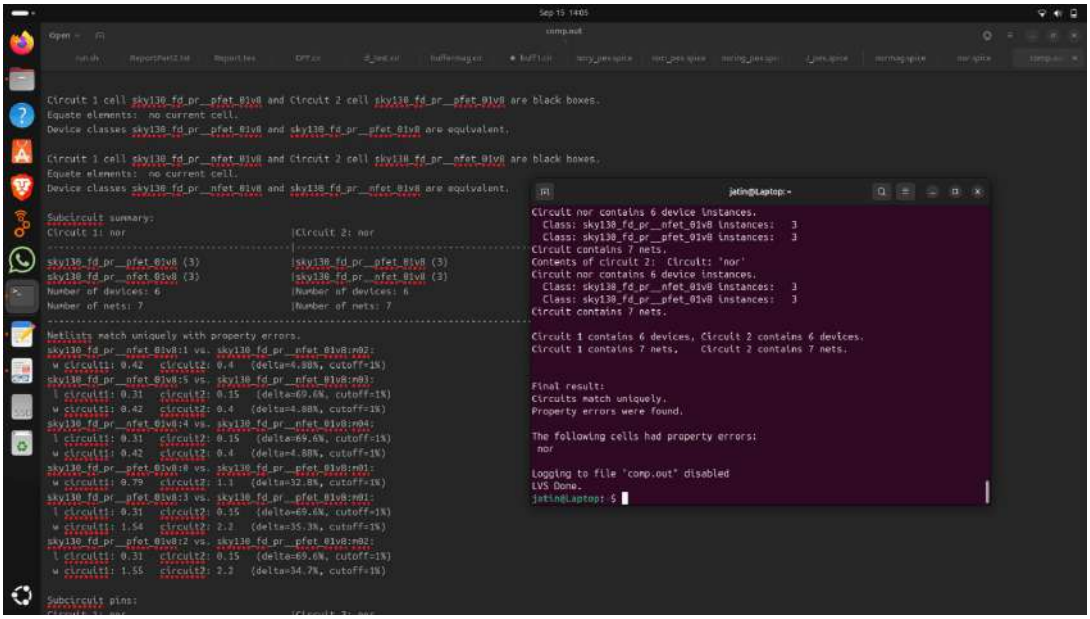


Figure 3.4: LVS Verification for NOR Gate (nor2b)

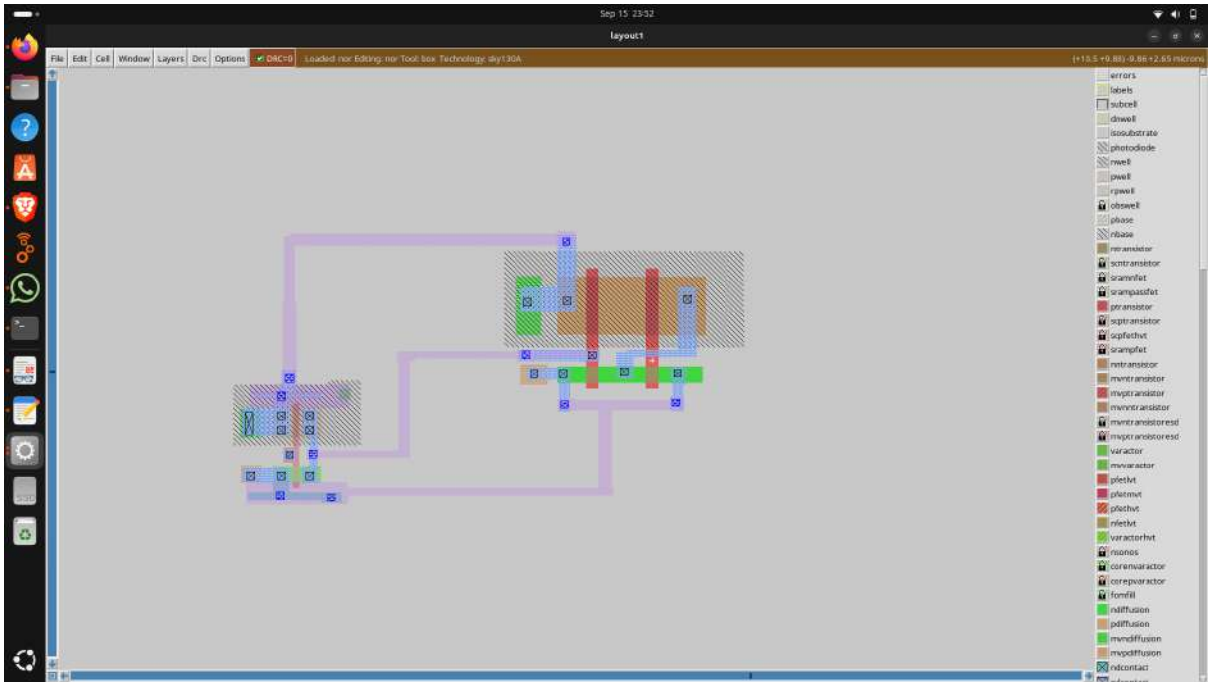


Figure 3.5: DRC Verification for NOR Gate (nor2b)

3.4 Timing, Power, and Capacitance Characterization

3.4.1 Input Pin Capacitances

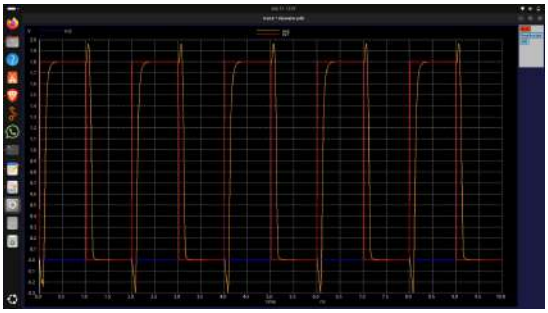
Input Pin	Rise Cap (fF)	Fall Cap (fF)	Average Cap (fF)
A	0.001778	0.0015454	0.0016617
B	0.002336	0.00229	0.002825

Table 3.2: Input Pin Capacitances for NOR Gate (nor2b)

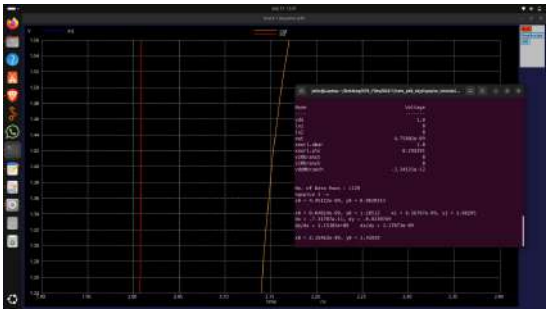
3.4.2 Transition Time Table

Capacitance (fF)	10 ps Slew (ns)	100 ps Slew (ns)	1000 ps Slew (ns)
Output Rise Transitions			
Related Pin A			
0.5 fF	0.04394	0.0477	0.0484
10 fF	0.2322	0.2314	0.2324
100 fF	2.0305	2.0255	2.0247
Related Pin B			
0.5 fF	0.04201	0.04062	0.1058
10 fF	0.3018	0.2209	0.274
100 fF	2.077	1.914	2.016
Output Fall Transitions			
Related Pin A			
0.5 fF	0.04064	0.0459	0.0474
10 fF	0.2172	0.2191	0.2133
100 fF	1.9278	1.9254	1.9151
Related Pin B			
0.5 fF	0.03997	0.03984	0.975
10 fF	0.2966	0.2085	0.257
100 fF	1.87	1.9	1.915

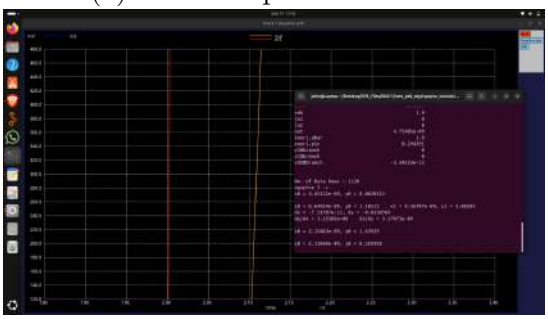
Table 3.3: Transition Time Table for NOR Gate (nor2b)



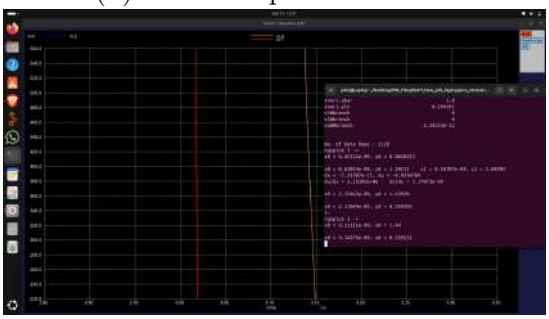
(a) A0.5fF 10psNOR Overall



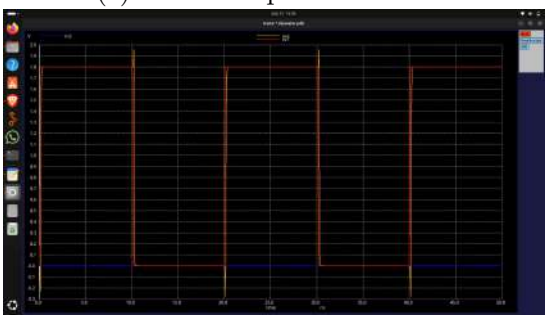
(b) A0.5fF 10psNOR rise 80



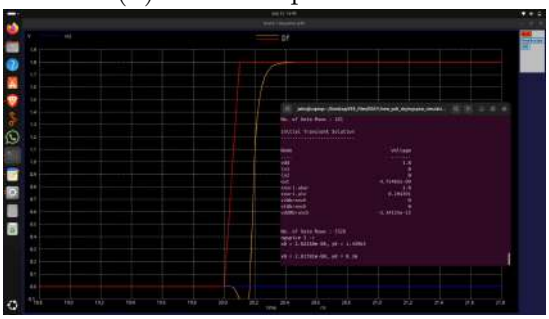
(c) A0.5fF 10psNOR rise 20



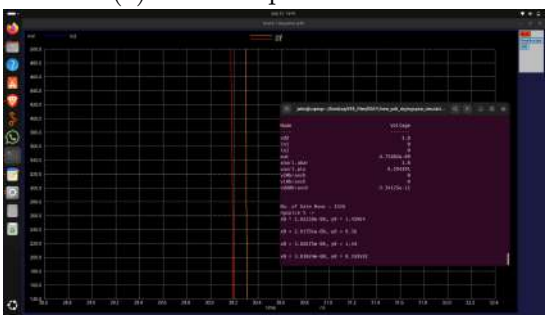
(d) A0.5fF 10psNOR fall



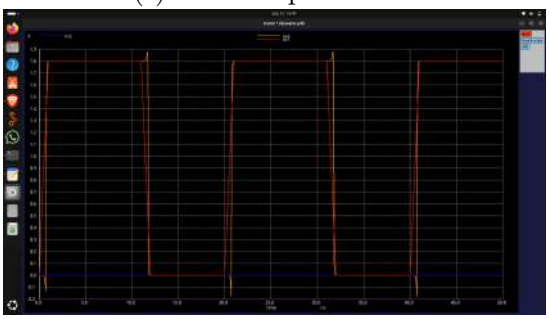
(e) A0.5f100psNor overall



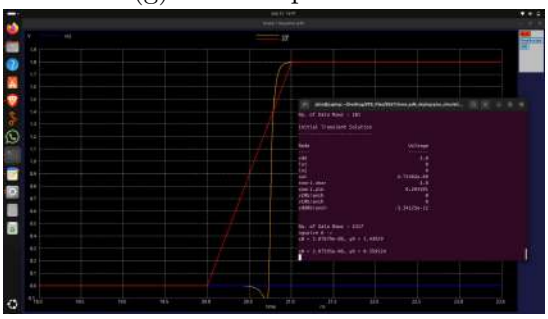
(f) A0.5f100psNor rise



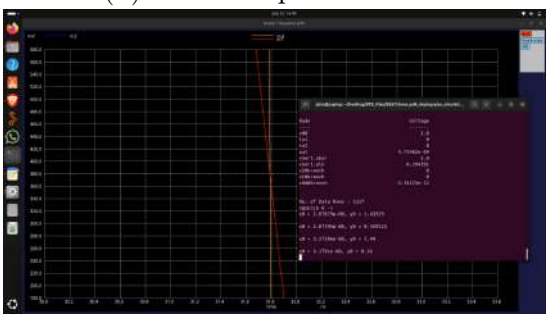
(g) A0.5f100psNor fall



(h) A0.5f1000psNor overall

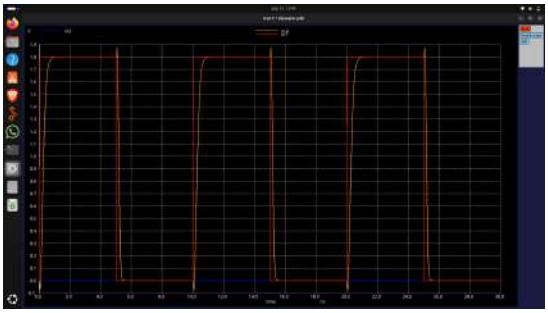


(i) A0.5f1000psNor rise

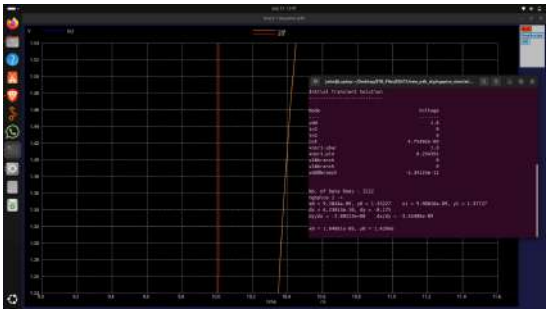


(j) A0.5f1000psNor fall

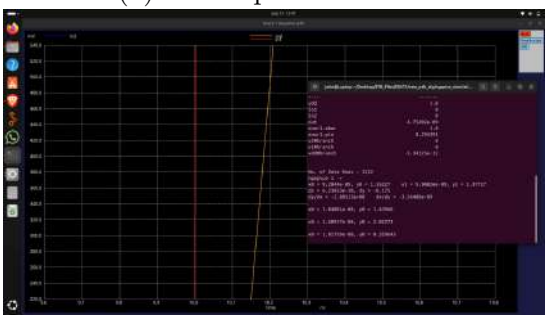
Figure 3.6: Transition Time Simulations for Pin A



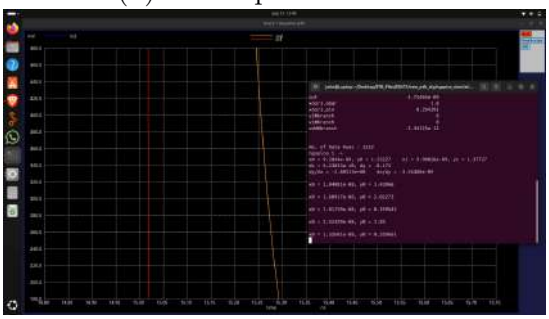
(a) A10f10psNor Overall



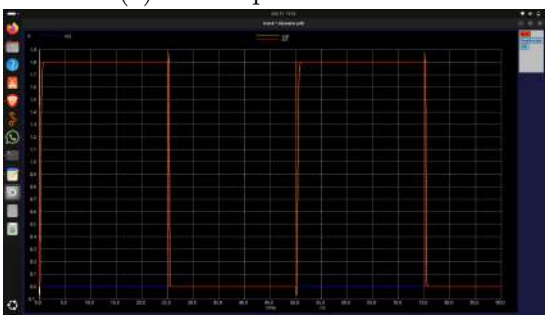
(b) A10f10psNor Rise 80



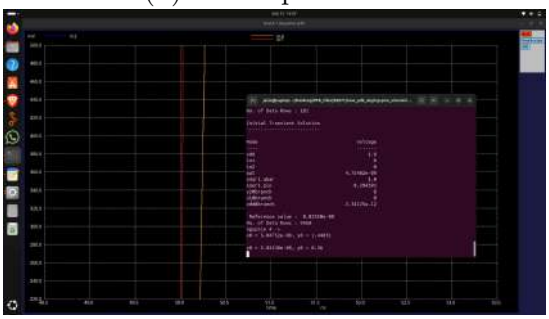
(c) A10f10psNor Rise 20



(d) A10f10psNor fall

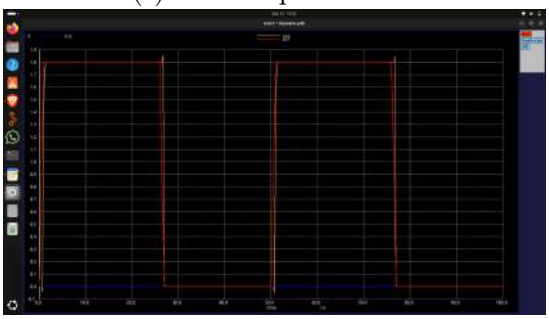


(e) A10f100psNor overall

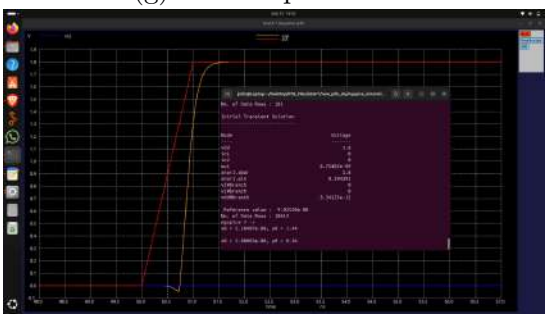


(f) A10f100psNor Rise

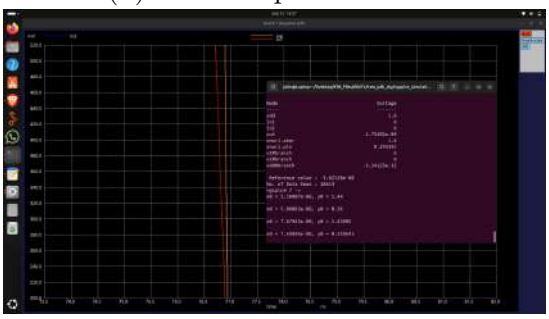
(g) A10f100psNor Fall



(h) A10f1000psNor overall

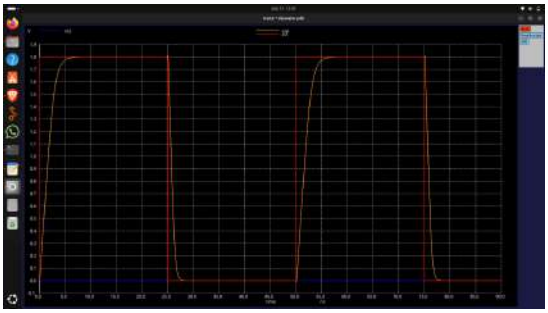


(i) A10f1000psNor rise

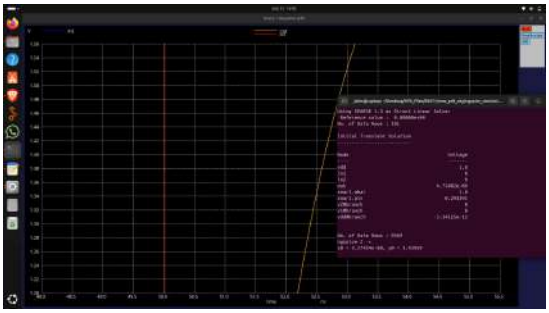


(j) A10f1000psNor fall

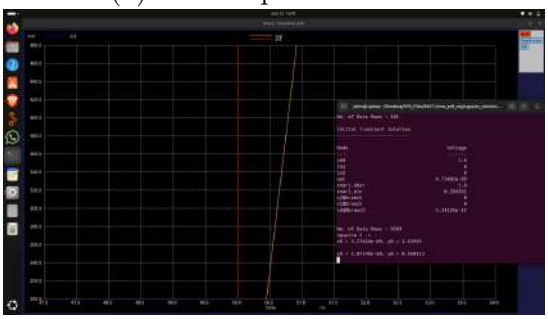
Figure 3.7: Transition Time Simulations for Pin A



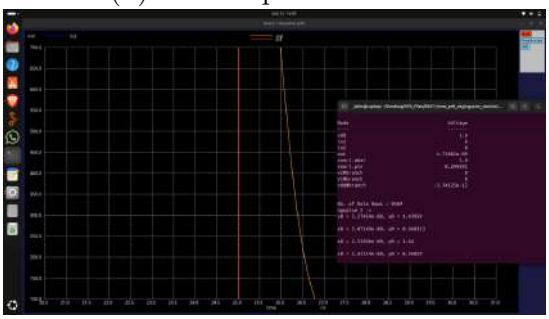
(a) A100f10psNor Overall



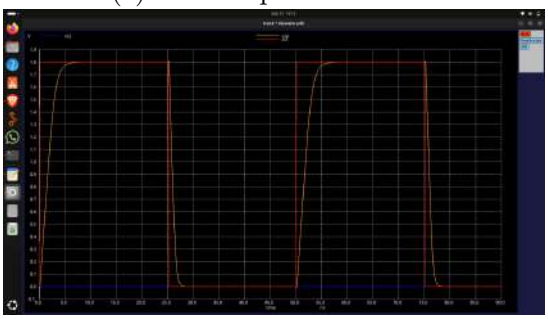
(b) A100f10psNor Rise 80



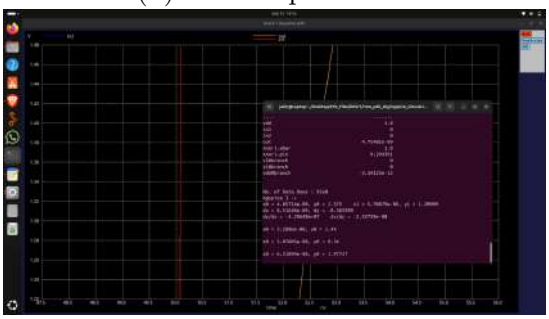
(c) A100f10psNor Rise 20



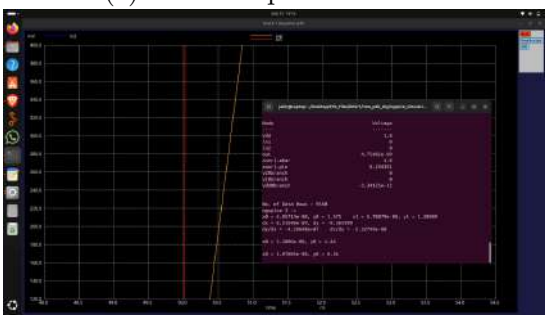
(d) A100f10psNor fall



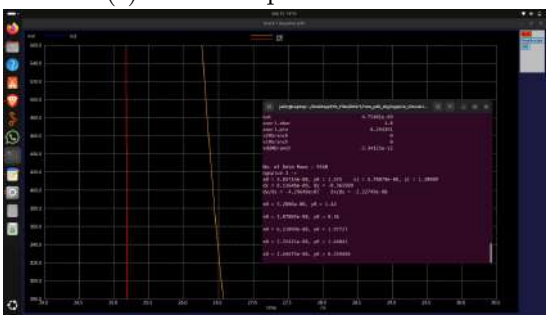
(e) A100f100psNor Overall



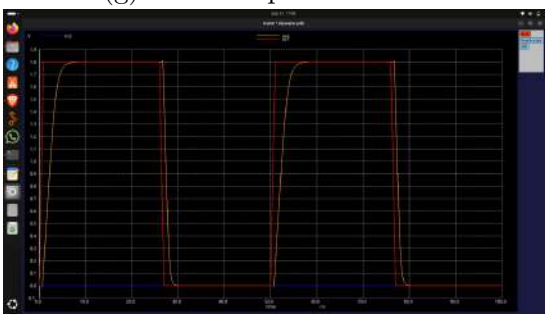
(f) A100f100psNor Rise 80



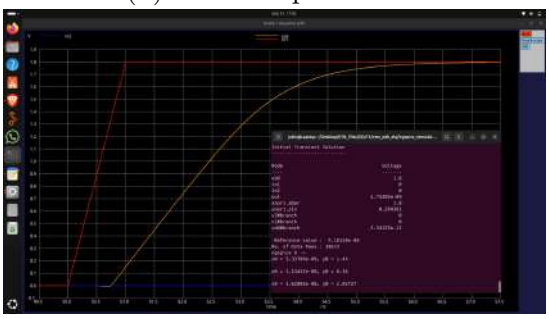
(g) A100f100psNor Rise 20



(h) A100f100psNor Fall

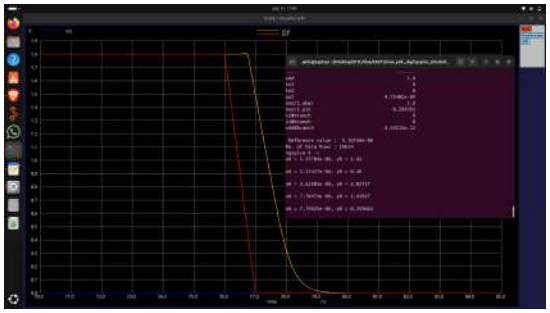


(i) A100f1000psNor overall



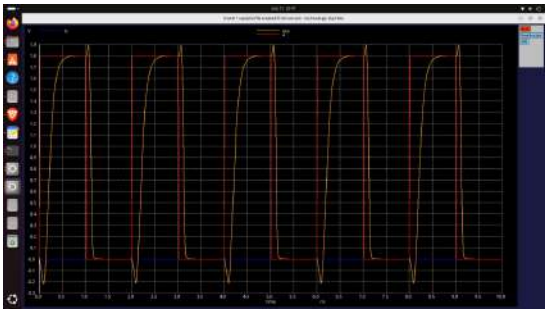
(j) A100f1000psNor rise

Figure 3.8: Transition Time Simulations for Pin A

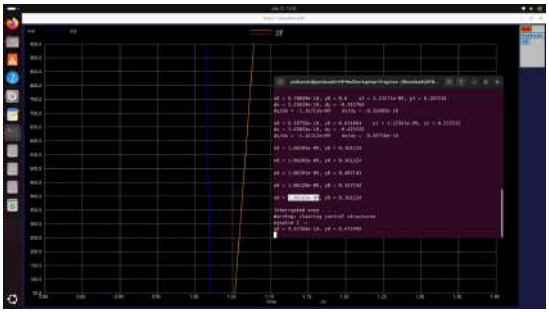


(a) A100f1000psNor fall

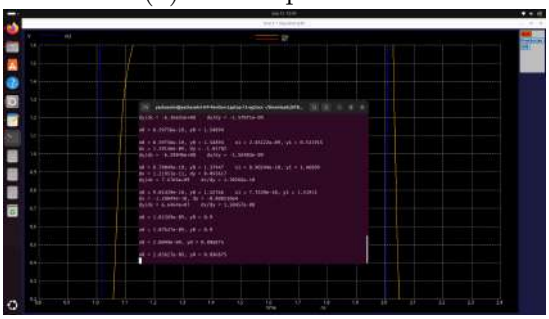
Figure 3.9: Transition Time Simulations for Pin A



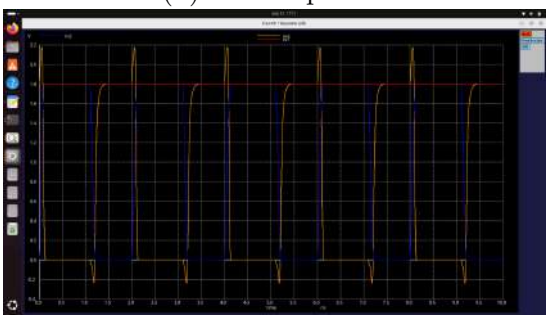
(a) B0.5f10psOverall



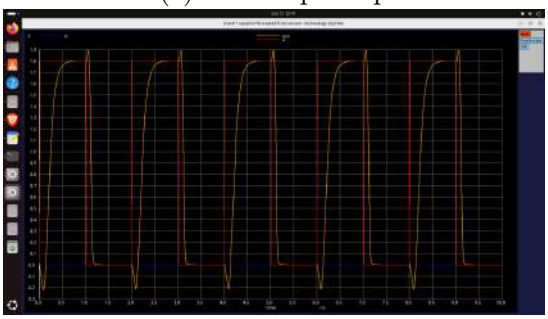
(b) B0.5f10psRise



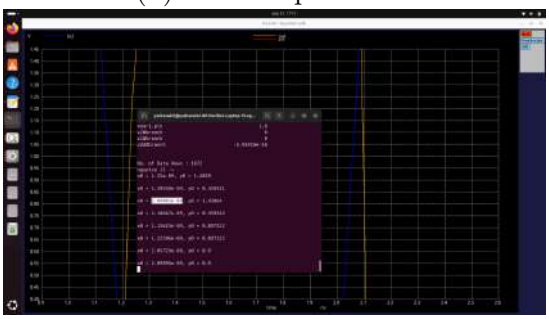
(c) B0.5f10psProp



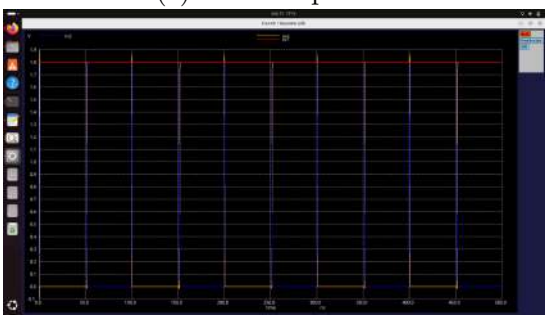
(d) B0.5f100psOverall



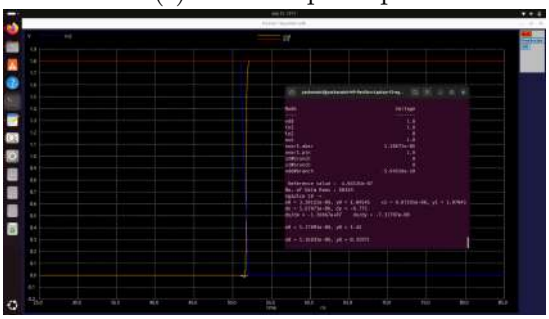
(e) B0.5f100psRise



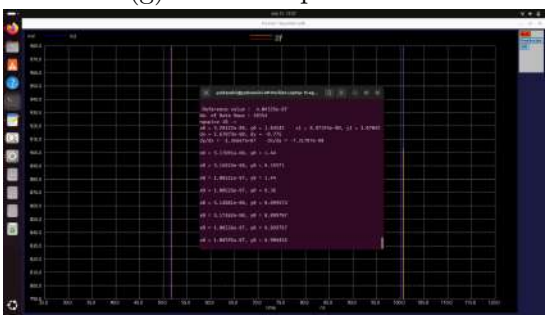
(f) B0.5f100psProp



(g) B0.5f1000psOverall

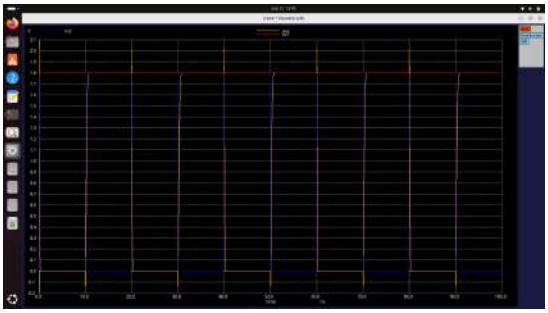


(h) B0.5f1000psRise

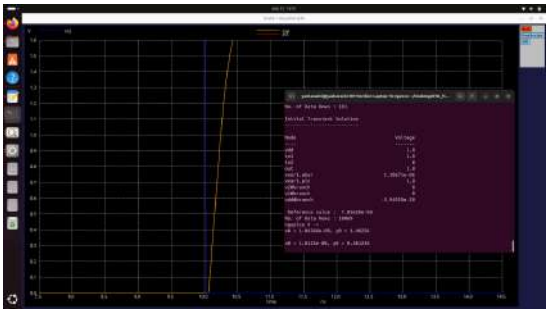


(i) B0.5f1000psProp

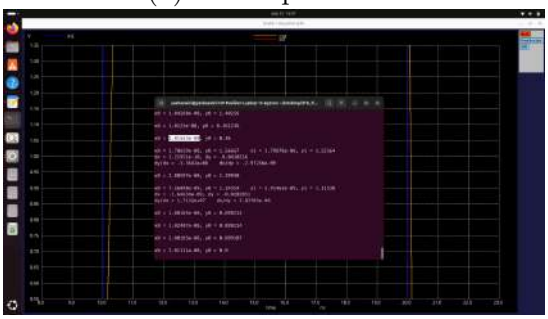
Figure 3.10: Pin B Transition Time Simulations for Capacitance 0.5fF



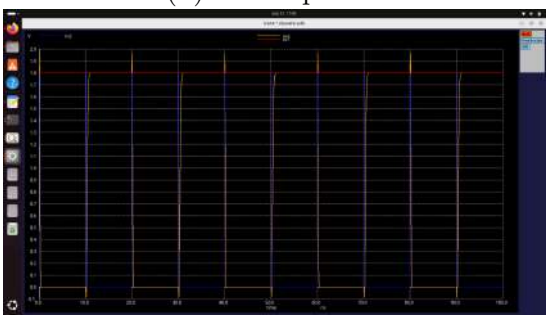
(a) B10f10psOverall



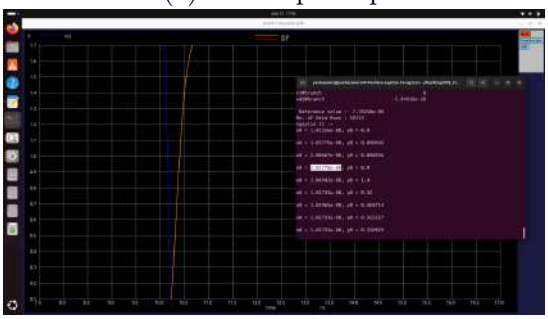
(b) B10f10psRise



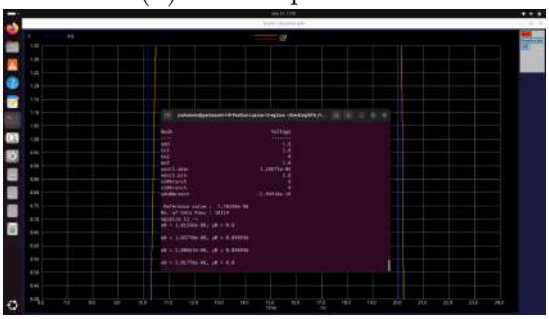
(c) B10f10psProp



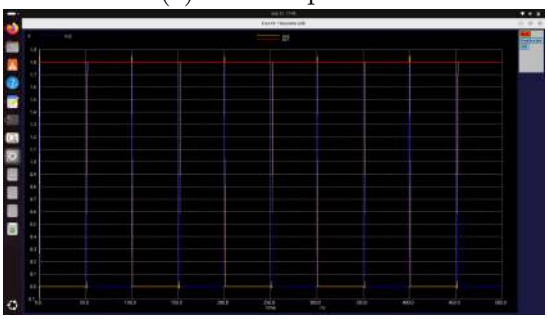
(d) B10f100psOverall



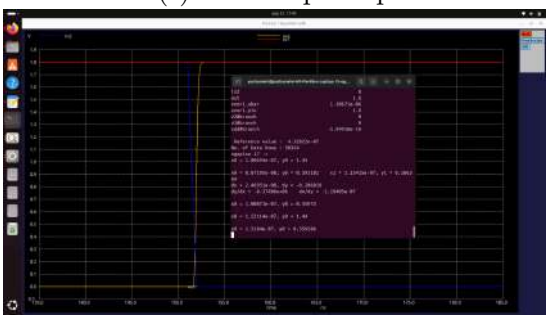
(e) B10f100psRise



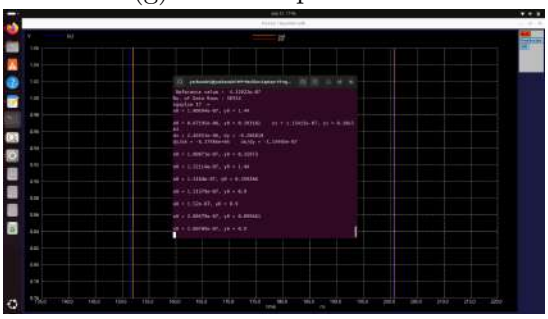
(f) B10f100psProp



(g) B10f1000psOverall

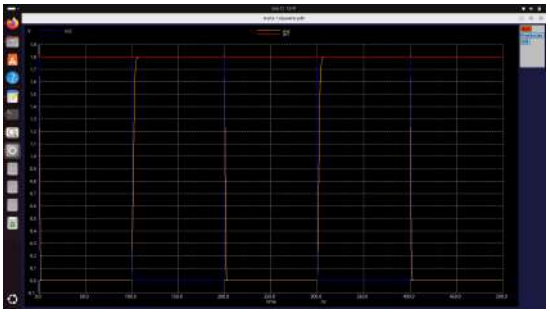


(h) B10f1000psRise

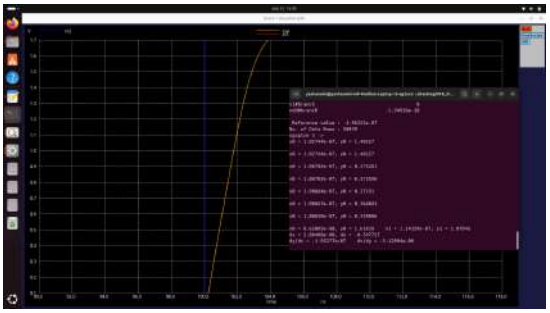


(i) B10f1000psProp

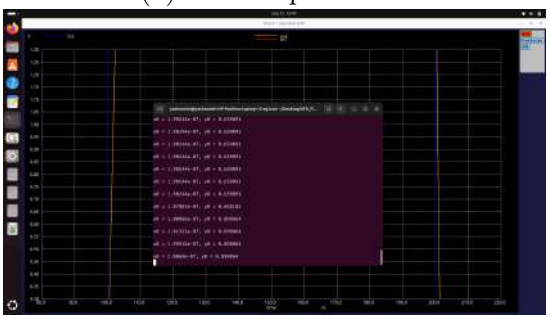
Figure 3.11: Pin B Transition Time Simulations for Capacitance 10fF



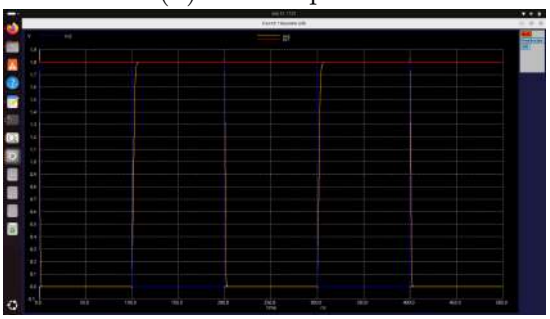
(a) B100f10psOverall



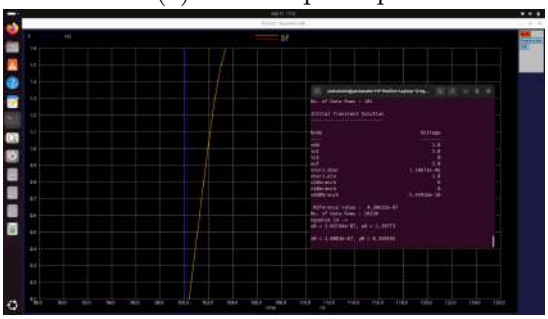
(b) B100f10psRise



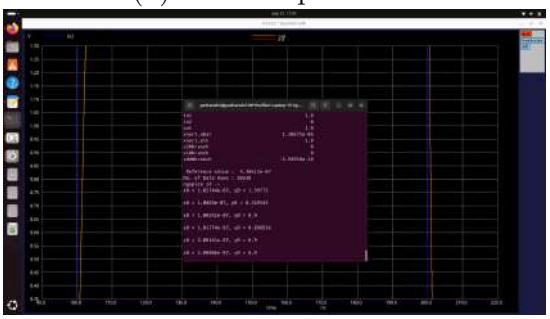
(c) B100f10psProp



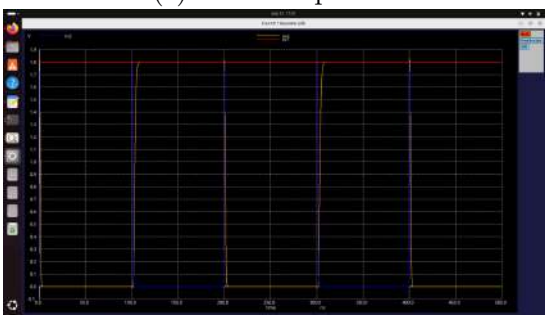
(d) B100f100psOverall



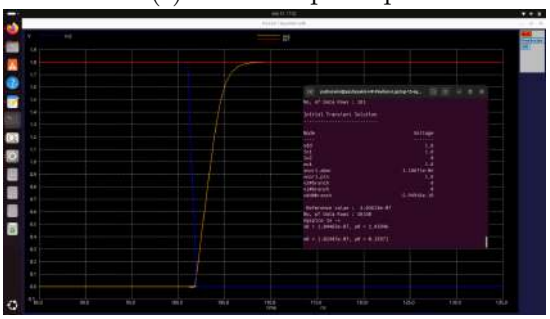
(e) B100f100psRise



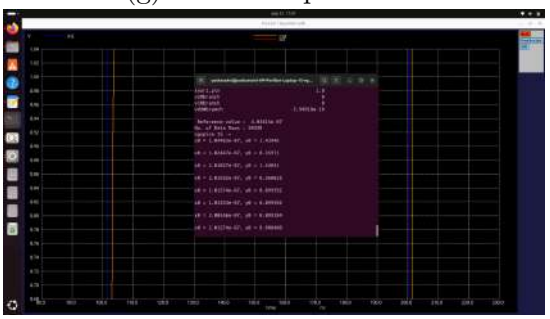
(f) B100f100psProp



(g) B100f1000psOverall



(h) B100f1000psRise



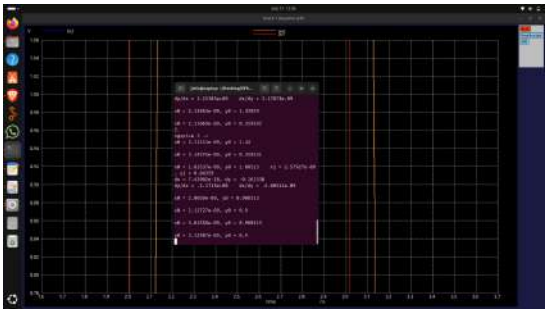
(i) B100f1000psProp

Figure 3.12: Pin B Transition Time Simulations for Capacitance 100fF

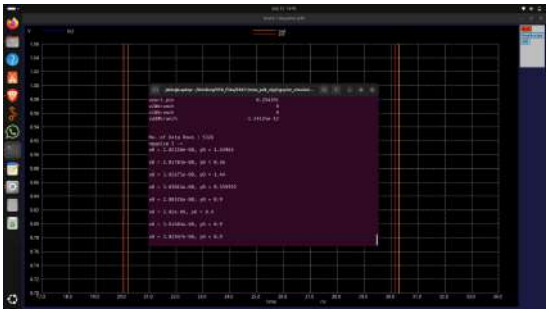
3.4.3 Propagation Delay Time Table

Capacitance (fF)	10 ps Slew (ns)	100 ps Slew (ns)	1000 ps Slew (ns)
Cell Rise Delay			
Related Pin A			
0.5 fF	0.12337	0.1474	0.2475
10 fF	0.2772	0.3556	0.4
100 fF	1.6444	1.7263	1.8025
Related Pin B			
0.5 fF	0.06078	0.06771	0.2381
10 fF	0.2222	0.2222	0.421
100 fF	1.466	1.532	1.759
Cell Fall Delay			
Related Pin A			
0.5 fF	0.11429	0.1263	0.2673
10 fF	0.1881	0.2222	0.353
100 fF	0.8	0.8421	1.0124
Related Pin B			
0.5 fF	0.03137	0.04167	0.059
10 fF	0.0926	0.1111	0.21
100 fF	0.776	0.645	1.018

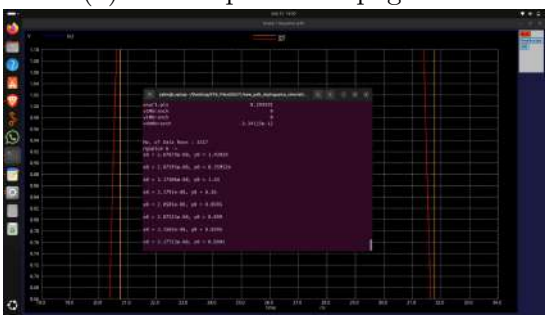
Table 3.4: Propagation Delay Time Table for NOR Gate (nor2b)



(a) A0.5f10psNor Propagation

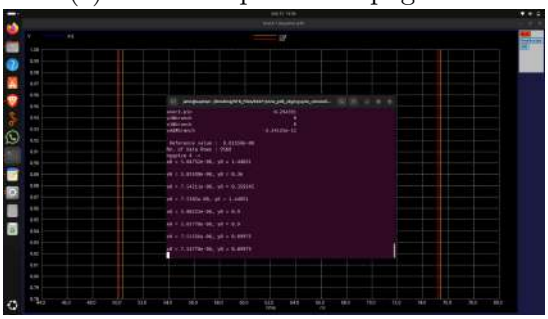


(b) A0.5f100psNor Propagation

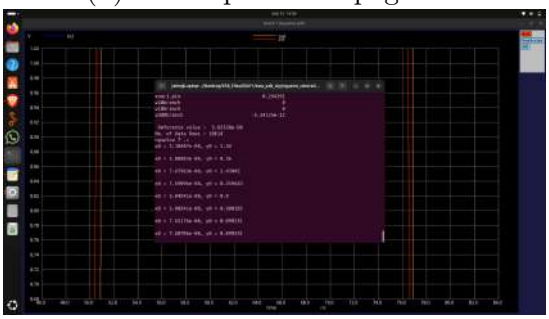


(c) A0.5f1000psNor Propagation

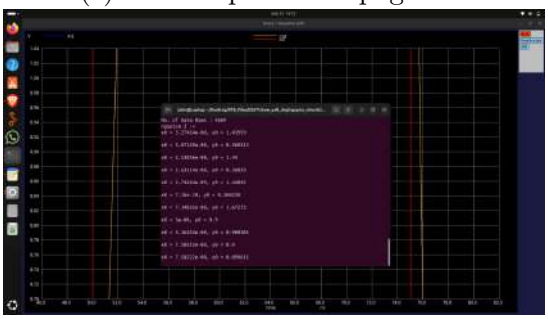
(d) A10f10psNor Propagation



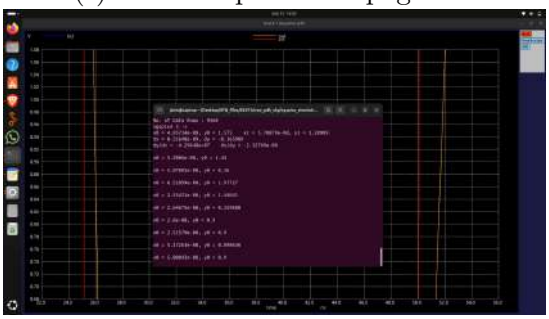
(e) A10f100psNor Propagation



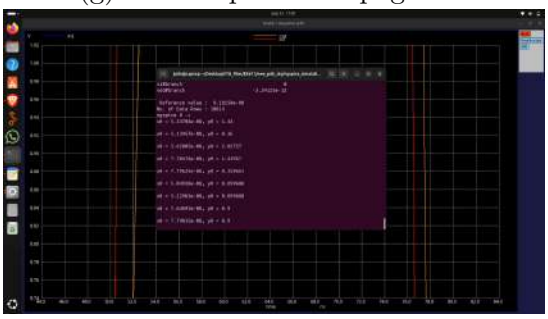
(f) A10f1000psNor Propagation



(g) A100f10psNor Propagation



(h) A100f100psNor Propagation



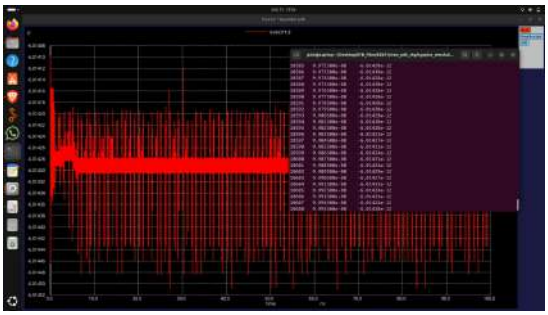
(i) A100f1000psNor Propagation

Figure 3.13: Propagation Delay Simulation NOR Gate

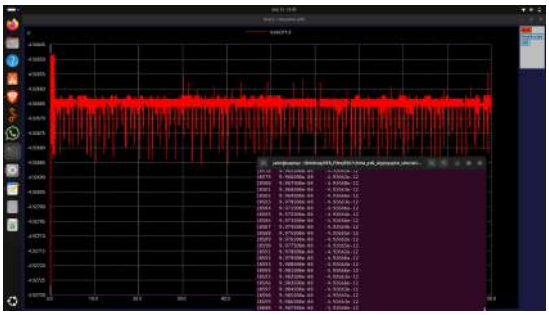
3.4.4 Static Power

Condition (A, B)	Power
00	6 pW
01	4.9266 pW
10	1.07085 nW
11	1.06748 nW

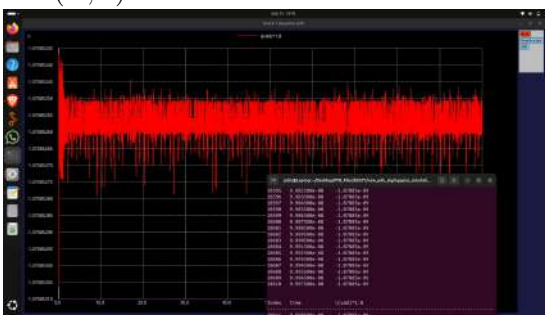
Table 3.5: Static Power for NOR Gate (nor2b)



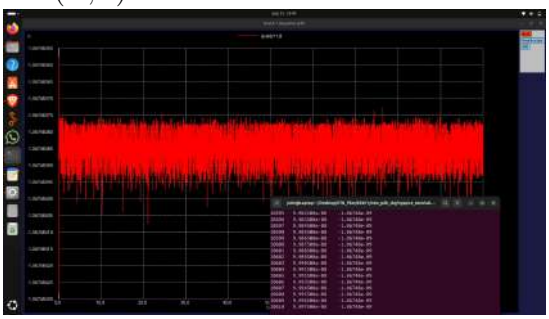
(a) Static Power for NOR Gate Condition(A,B) 00



(b) Static Power for NOR Gate Condition(A,B) 01



(c) Static Power for NOR Gate Condition(A,B) 10



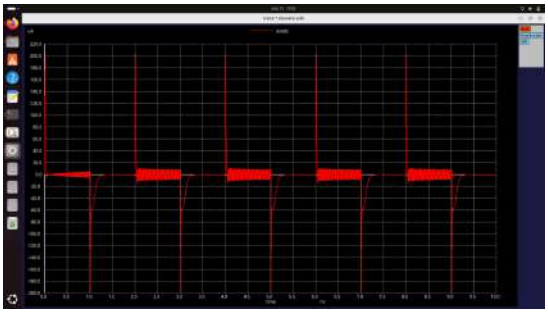
(d) Static Power for NOR Gate Condition(A,B) 11

Figure 3.14: Static Power for NOR Gate Condition(A,B)

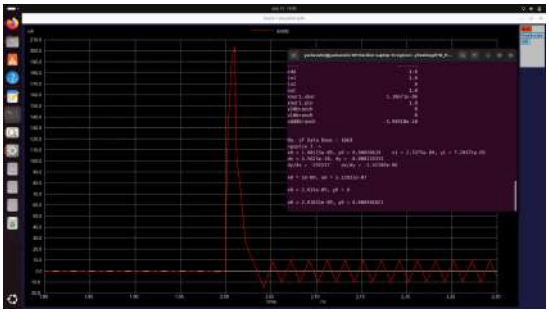
3.4.5 Dynamic Power Table

Capacitance (fF)	10 ps Slew (nW)	100 ps Slew (nW)	1000 ps Slew (nW)
Rise Power			
Related Pin A			
0.5 fF	818	33.156684	1,583
10 fF	356.51	1,721.6	2,936
100 fF	18,220	11,378	11,670
Related Pin B			
0.5 fF	6,366.15	4,653.126	1,516.1
10 fF	594.765	284.94	152.779
100 fF	287.9	83.79466	228.39
Fall Power			
Related Pin A			
0.5 fF	954.7	1,020	812.37
10 fF	1,680.5	882.47	722.7
100 fF	993.983	5,546.5	1,793.346
Related Pin B			
0.5 fF	52.2350775	19,922.4	568.84
10 fF	3,192.1	1,633.82	2,022.57
100 fF	19,120	9,968	9,701

Table 3.6: Dynamic Power Table for NOR Gate (nor2b)

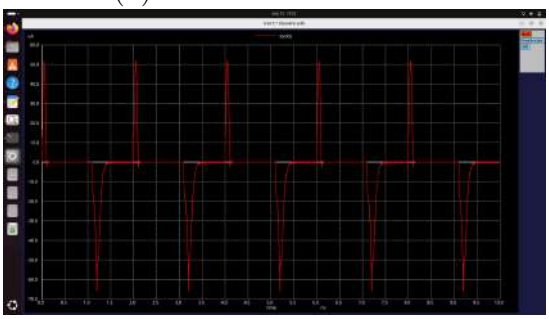


(a) DP0.5f10nsNOR Overall

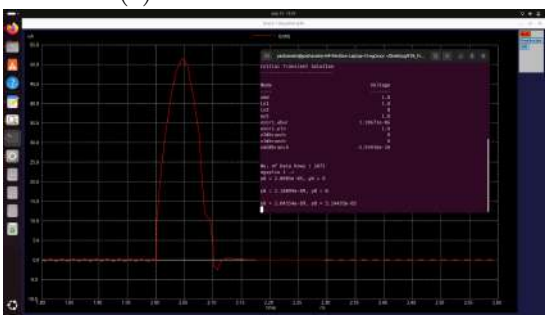


(b) DP0.5f10nsNOR Rise

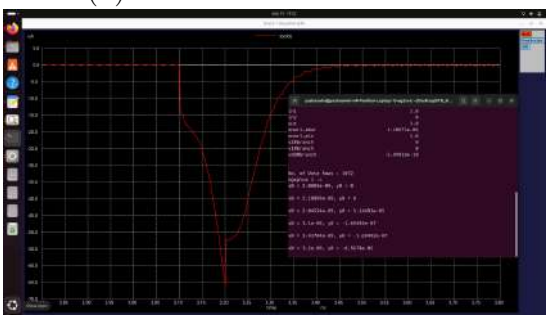
(c) DP0.5f10nsNOR Fall



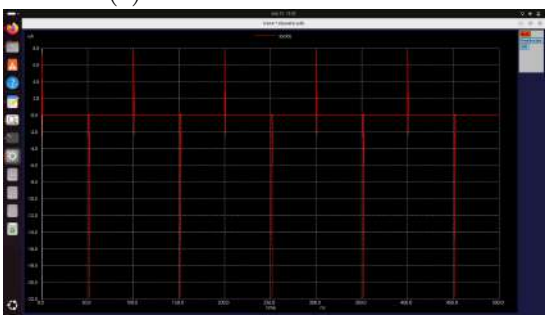
(d) DP0.5f100nsNOR Overall



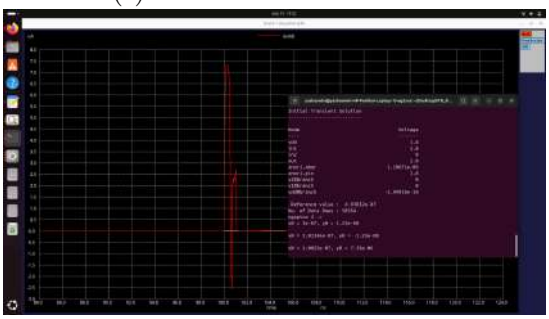
(e) DP0.5f100nsNOR Rise



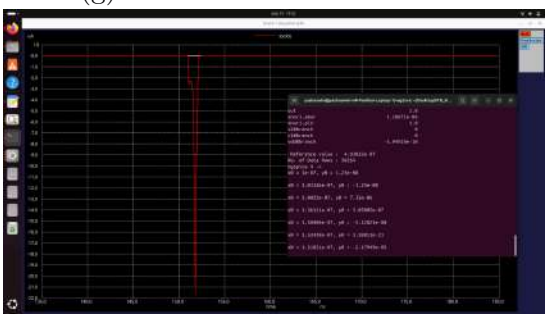
(f) DP0.5f100nsNOR Fall



(g) DP0.5f1000nsNOR Overall

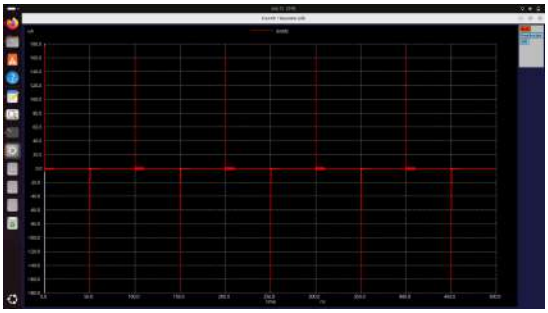


(h) DP0.5f1000nsNOR Rise

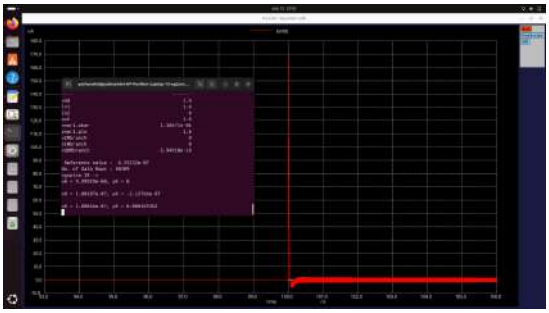


(i) DP0.5f1000nsNOR Fall

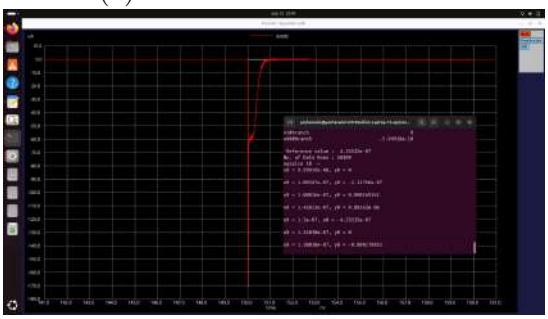
Figure 3.15: Dynamic Power Simulations for 0.5f Capacitance



(a) DP10f10nsNOR Overall

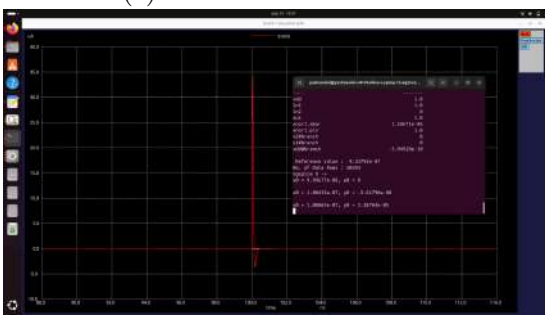


(b) DP10f10nsNOR Rise

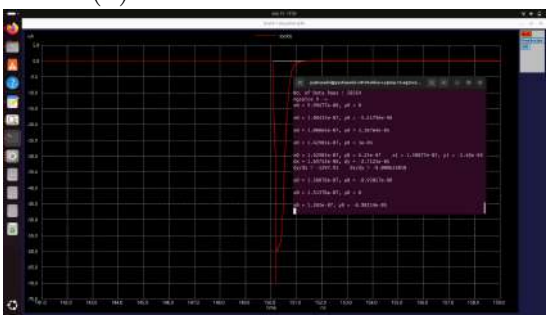


(c) DP10f10nsNOR Fall

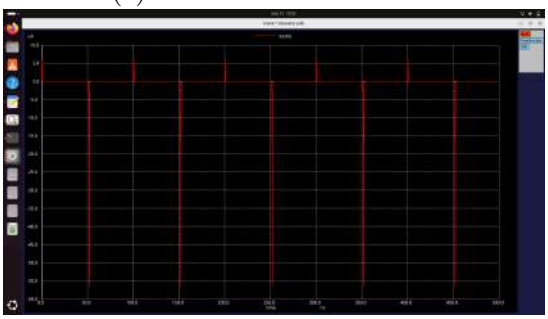
(d) DP10f100nsNOR Overall



(e) DP10f100nsNOR Rise

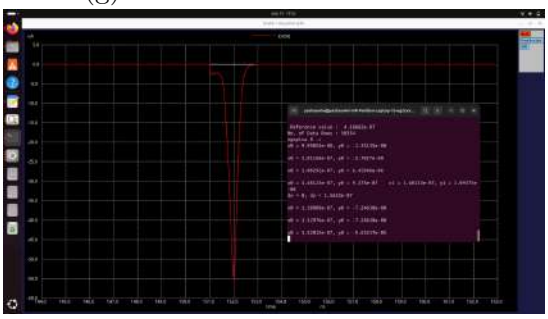


(f) DP10f100nsNOR Fall



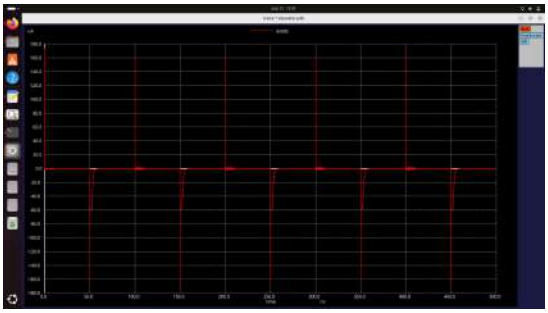
(g) DP10f1000nsNOR Overall

(h) DP10f1000nsNOR Rise

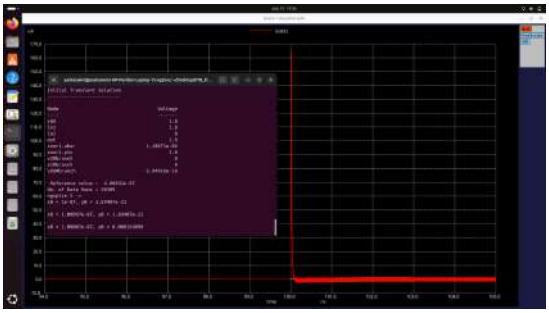


(i) DP10f1000nsNOR Fall

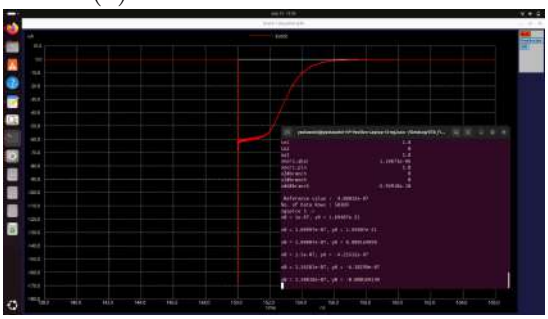
Figure 3.16: Dynamic Power Simulations for 10f Capacitance



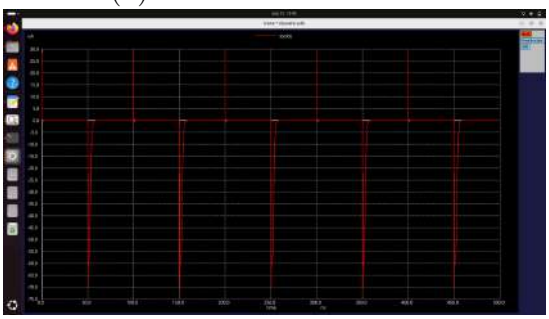
(a) DP100f10nsNOR Overall



(b) DP100f10nsNOR Rise

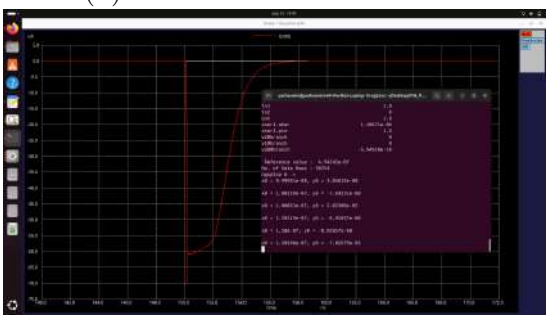


(c) DP100f10nsNOR Fall

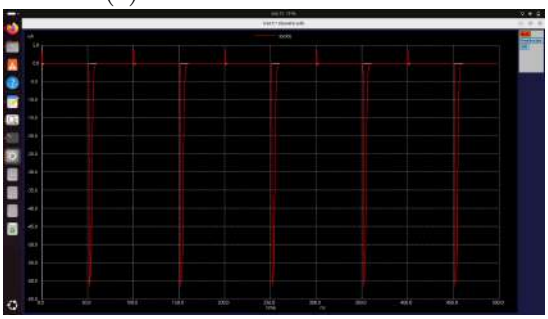


(d) DP100f100nsNOR Overall

(e) DP100f100nsNOR Rise

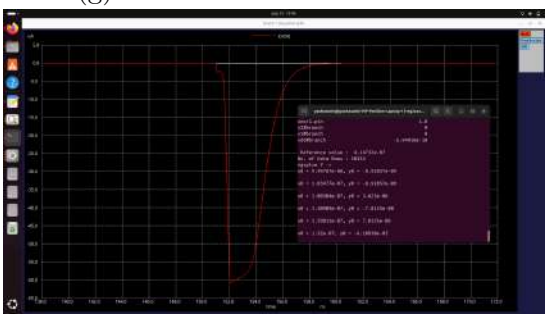


(f) DP100f100nsNOR Fall



(g) DP100f1000nsNOR Overall

(h) DP100f1000nsNOR Rise



(i) DP100f1000nsNOR Fall

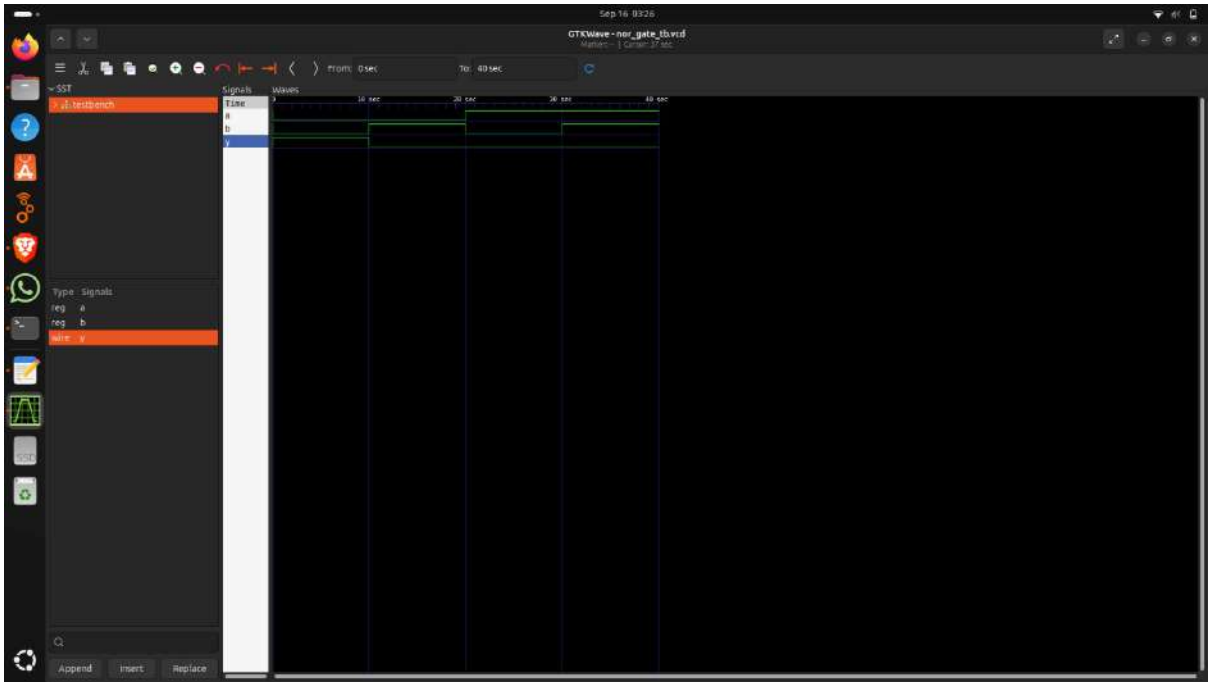
Figure 3.17: Dynamic Power Simulations for 100f Capacitance

3.5 HDL Functional Definition

The following Verilog code implements the NOR gate.

```
module nor_gate (
    input wire a,   // First input
    input wire b,   // Second input
    output wire y   // Output (result of NOR operation)
);

// NOR gate logic
assign y = ~(a |~b);

endmodule

// Testbench for NOR Gate
module testbench;

    reg a, b;       // Inputs for NOR gate
    wire y;         // Output from NOR gate

    // Instantiate the NOR gate
    nor_gate uut (
        .a(a),
        .b(b),
        .y(y)
    );

    // Test stimulus
    initial begin
        $dumpfile("nor_gate_tb.vcd");  // Dump file for waveform
        $dumpvars(0, testbench);

        // Test cases
        a = 0; b = 0; #10;
        a = 0; b = 1; #10;
        a = 1; b = 0; #10;
        a = 1; b = 1; #10;
        $finish;
        end

endmodule
```

3.5.1 VHDL Output for NOR



(a) VHDL Output for NOR

Figure 3.18: VHDL Output for NOR

Chapter 4

Cell 3: Delay Flop (dfxtp)

4.1 Circuit Design in NGSpice

4.1.1 Schematic Diagram

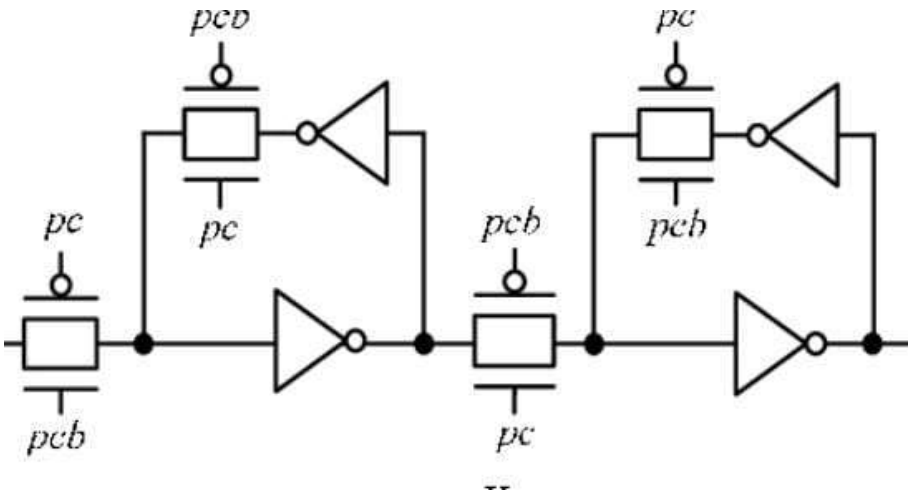


Figure 4.1: Schematic of Delay Flop (dfxtp)

4.1.2 D Flip-Flop Specifications

Device	Width (µm)	Length (µm)
NMOS	0.79	0.15
PMOS	0.42	0.15

Table 4.1: D Flip-Flop Output Dimensions

4.2 Screenshot of the PEX netlist DFF

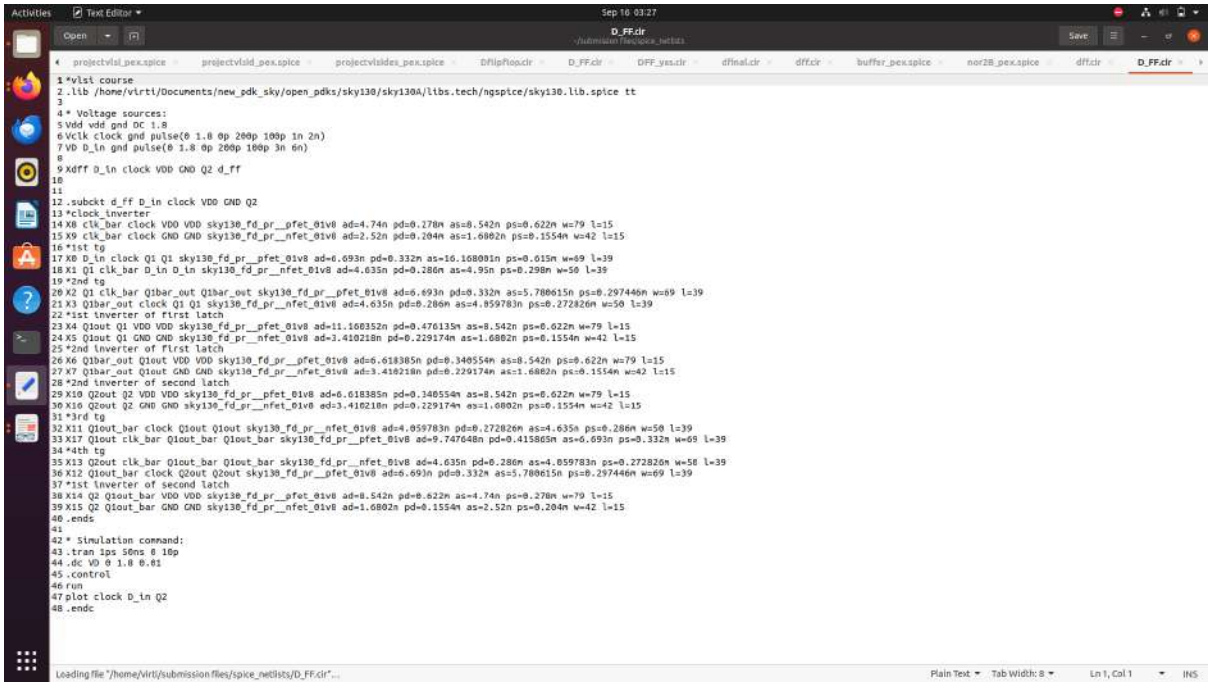


Figure 4.2: Screenshot of the PEX netlist

4.3 Layout Design in Magic

4.3.1 Layout Diagram

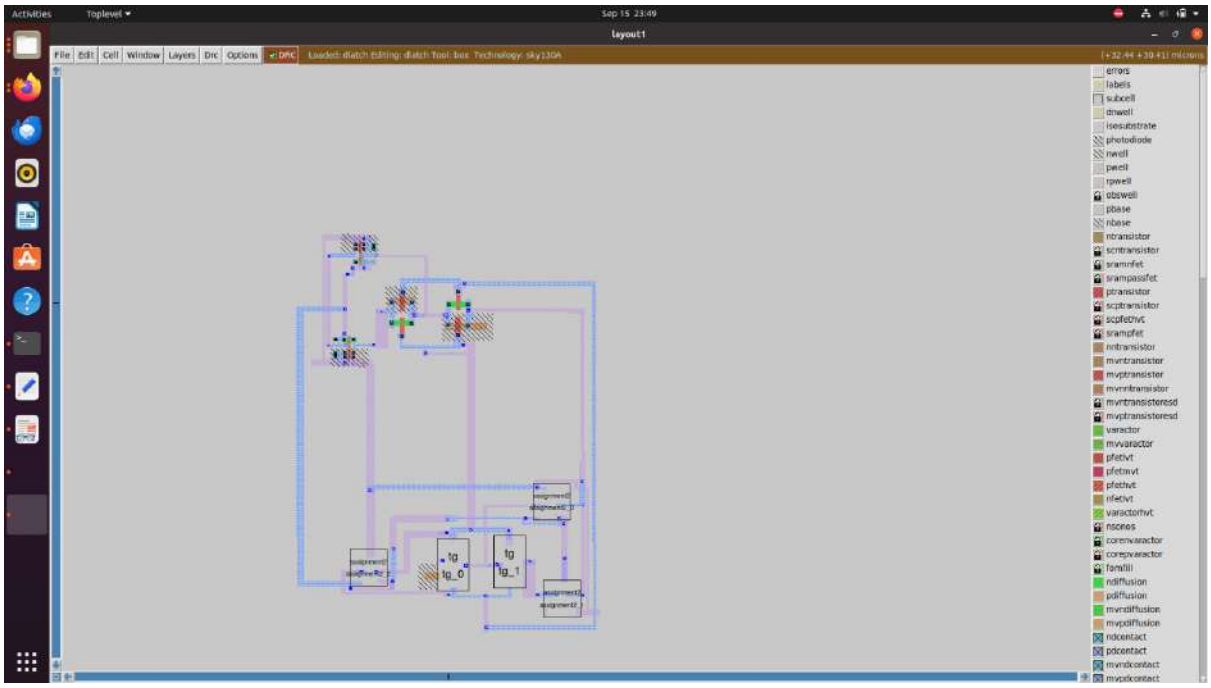


Figure 4.3: Layout of Delay Flop (dfxtp)

4.3.2 DRC and LVS Verification

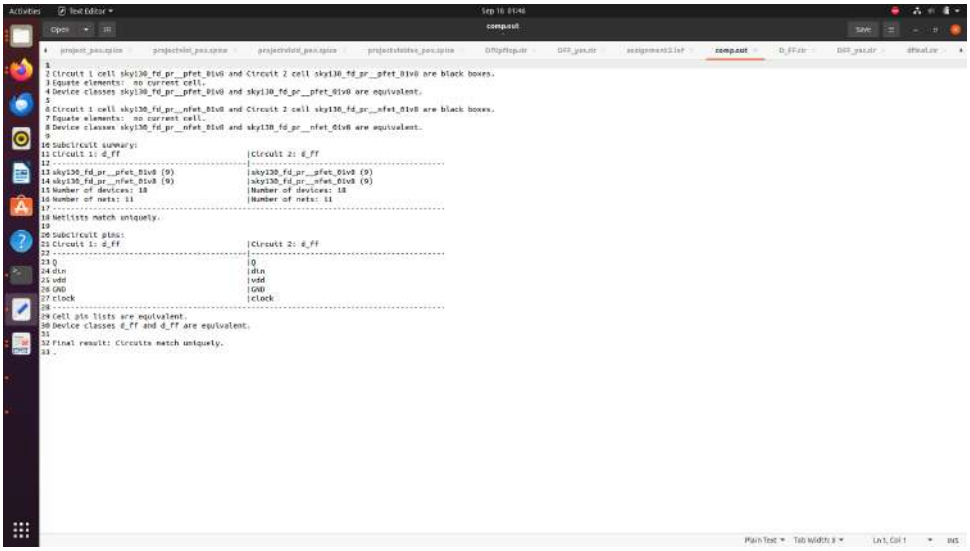


Figure 4.4: LVS Verification for Delay Flop (dfxtp)

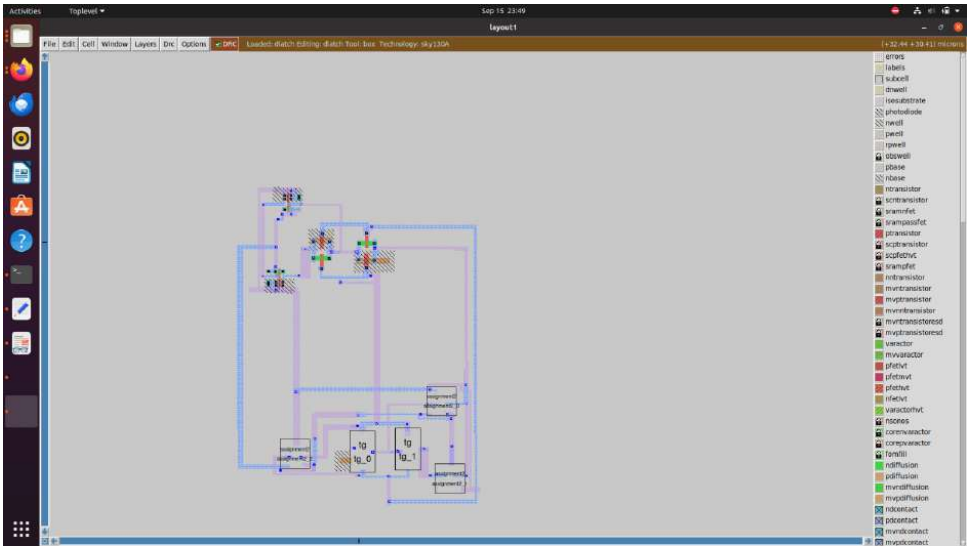


Figure 4.5: DRC Verification for Delay Flop (dfxtp)

4.4 Timing, Power, and Capacitance Characterization

4.4.1 a) Input Pin Capacitances

Input Pins	Rise Cap (fF)	Fall Cap (fF)	Average Cap (fF)
D	0.298	0.1999	0.24895
CLK	0.267	0.1888	0.2275

Table 4.2: Input Pin Capacitances for DFF

4.4.2 b) Set-up Time Table

(i) Rise Constraint (in ns) [Input slew vs CLK slew]

Input Slew	10 ps CLK Slew	1000 ps CLK Slew
10 ps	0.136	0.8
1000 ps	0.44	0.45

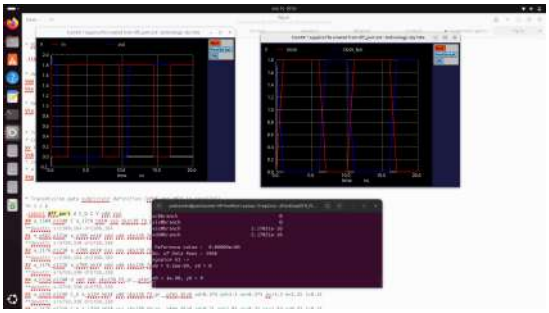
Table 4.3: Set-up Time Rise Constraint for DFF

(ii) Fall Constraint (in ns) [Input slew vs CLK slew]

Input Slew	10 ps CLK Slew	1000 ps CLK Slew
10 ps	0.25	0.9
1000 ps	0.42	0.43

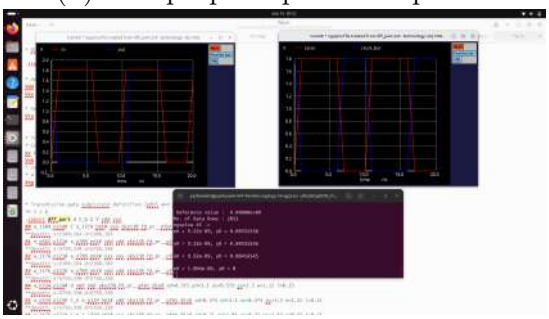
Table 4.4: Set-up Time Fall Constraint for DFF

(a) SetUpInput10psClk10psRise

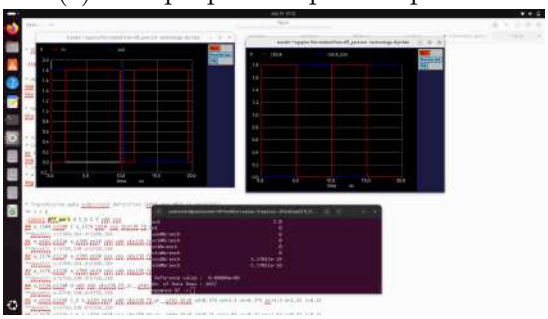


(b) SetUpInput10psClk1000psRise

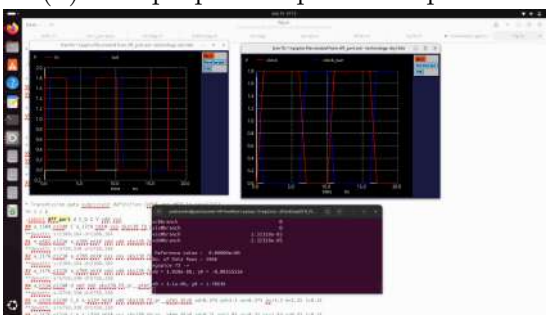
(c) SetUpInput1000psClk10psRise



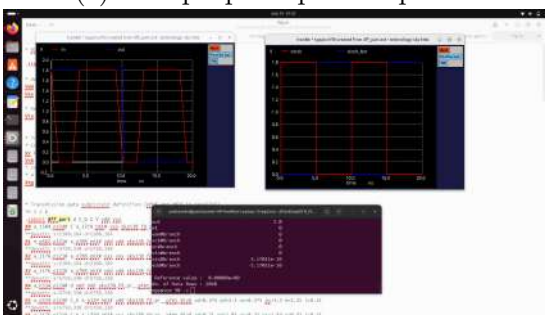
(d) SetUpInput1000psClk1000psRise



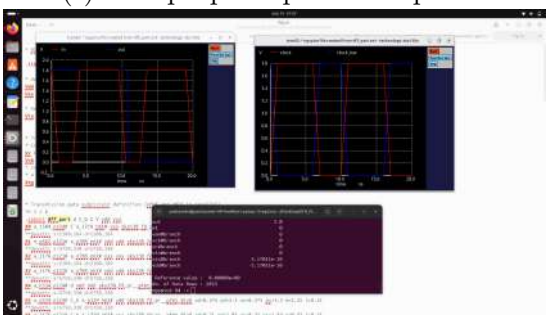
(e) SetUpInput10psClk10psFall



(f) SetUpInput10psClk1000psFall



(g) SetUpInput1000psClk10psFall



(h) SetUpInput1000psClk1000psFall

Figure 4.6: Set-Up Time Table

4.4.3 c) Hold Time Table

(i) Rise Constraint (in ns) [Input slew vs CLK slew]

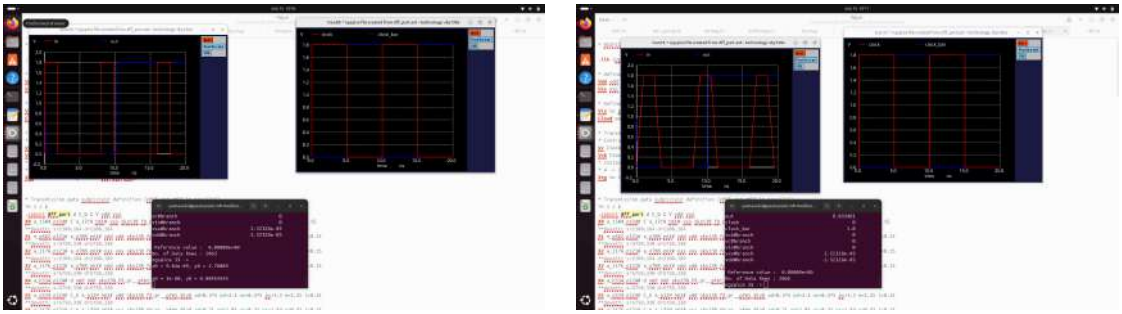
Input Slew	10 ps CLK Slew	1000 ps CLK Slew
10 ps	0.16	0.7
1000 ps	0.53	0.67

Table 4.5: Hold Time Rise Constraint for DFF

(ii) Fall Constraint (in ns) [Input slew vs CLK slew]

Input Slew	10 ps CLK Slew	1000 ps CLK Slew
10 ps	0.33	0.95
1000 ps	0.47	0.52

Table 4.6: Hold Time Fall Constraint for DFF



(a) Hold Constraint (b) Hold Constraint

Figure 4.7: Hold Time Table

(i) Output Rise Transitions (in ns) [Input slew vs output capacitance]

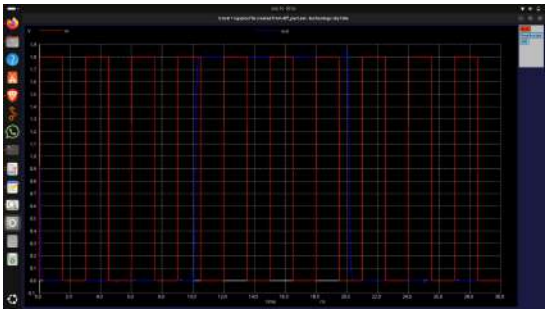
Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	0.1092	0.1144	0.1141
10 fF	0.1703	0.1717	0.1731
100 fF	0.7443	0.7452	0.7437

Table 4.7: Output Rise Transitions for DFF

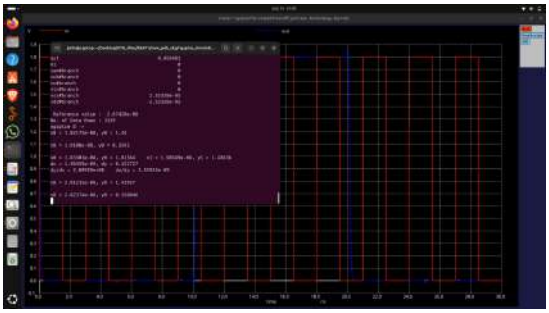
(ii) Output Fall Transitions (in ns) [Input slew vs output capacitance]

Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	0.1139	0.1148	0.1157
10 fF	0.1718	0.1725	0.1739
100 fF	0.7353	0.7349	0.7373

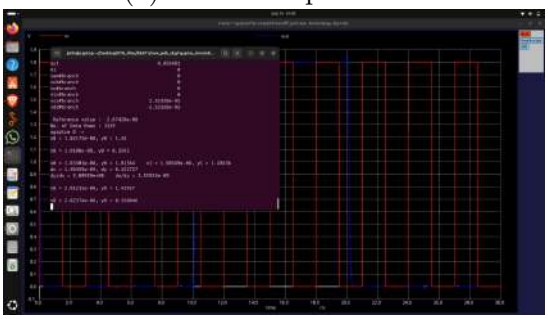
Table 4.8: Output Fall Transitions for DFF



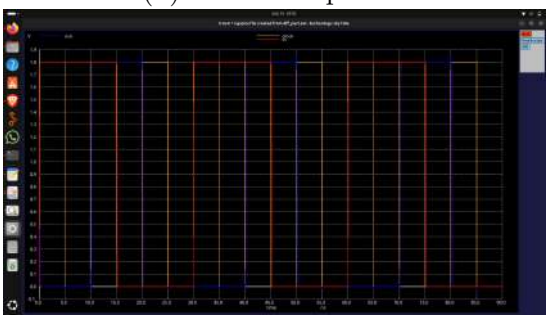
(a) DFF0.5f10psOverall



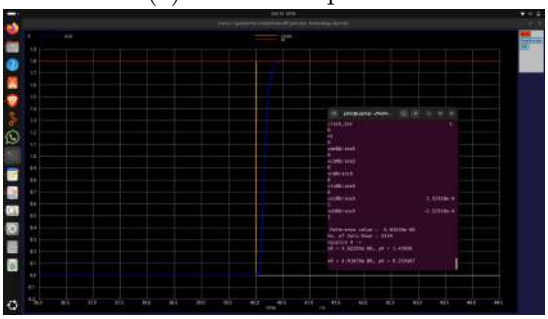
(b) DFF0.5f10psRise



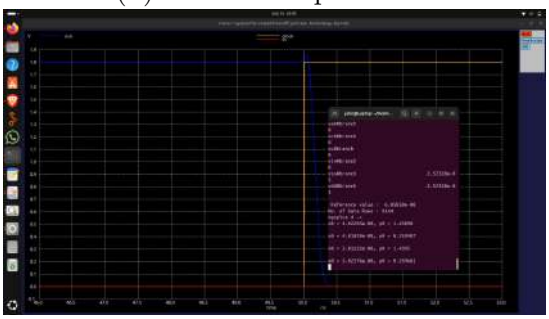
(c) DFF0.5f10psFall



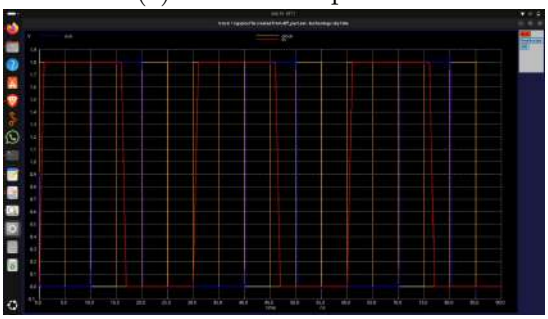
(d) DFF0.5f100psOverall



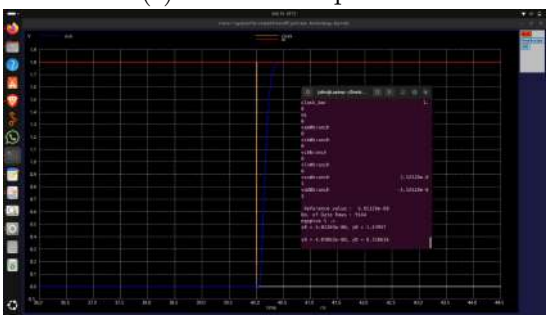
(e) DFF0.5f100psRise



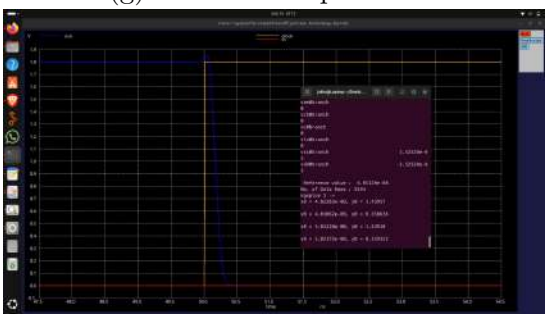
(f) DFF0.5f100psFall



(g) DFF0.5f1000psOverall

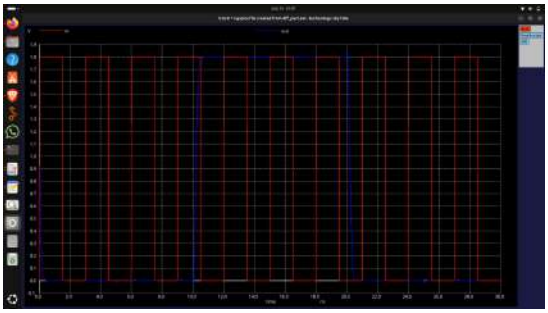


(h) DFF0.5f1000psRise

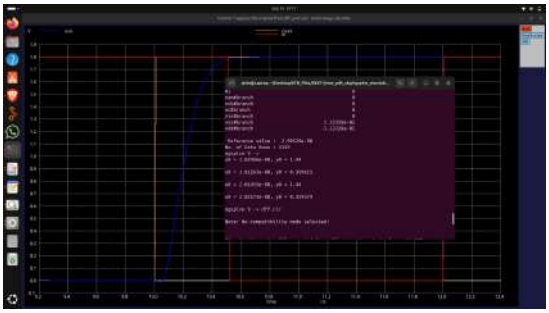


(i) DFF0.5f1000psFall

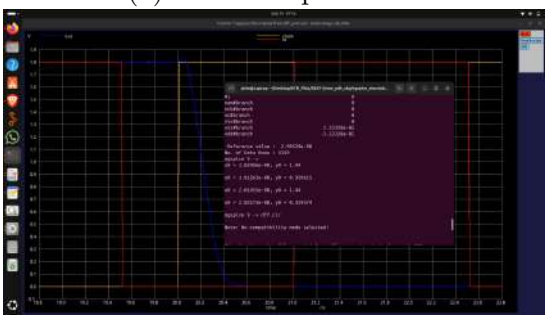
Figure 4.8: Transition Time Simulation for Capacitance 0.5fF



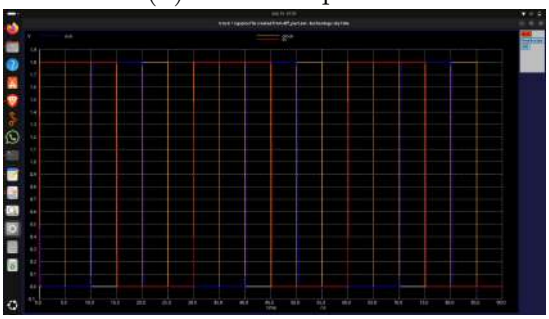
(a) DFF10f10psOverall



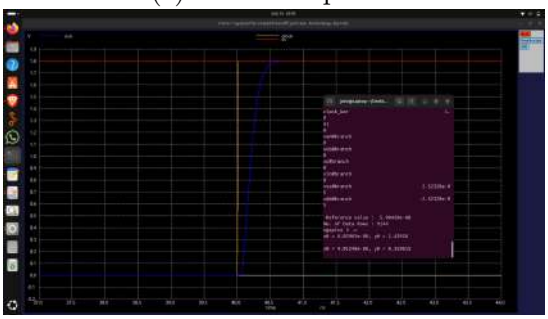
(b) DFF10f10psRise



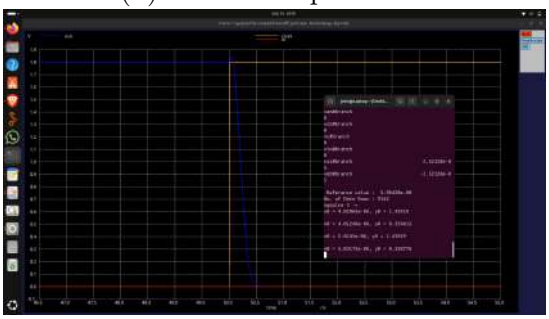
(c) DFF10f10psFall



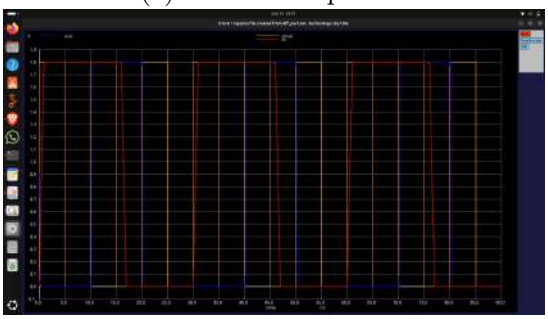
(d) DFF10f100psOverall



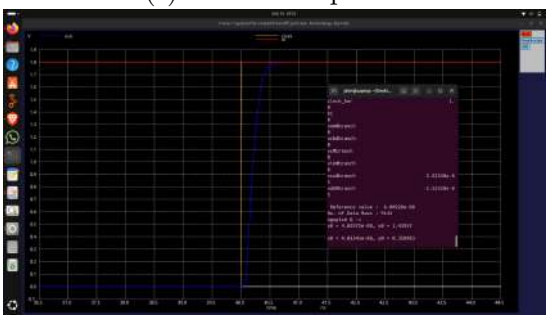
(e) DFF10f100psRise



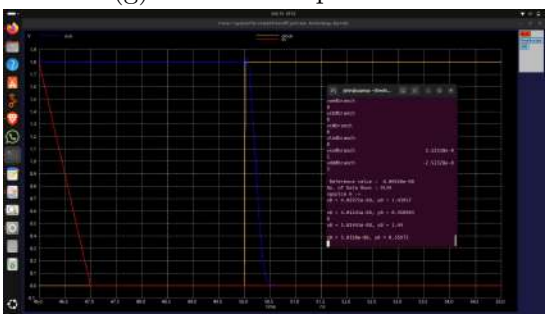
(f) DFF10f100psFall



(g) DFF10f1000psOverall

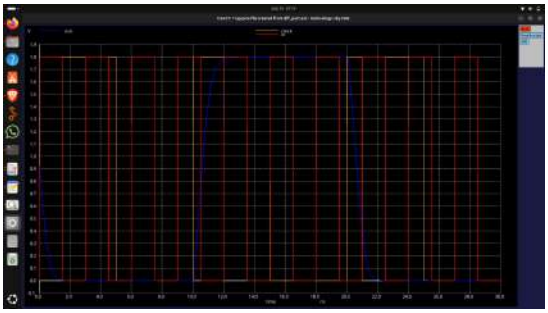


(h) DFF10f1000psRise

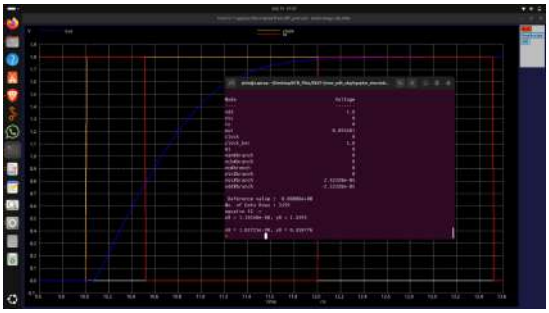


(i) DFF10f1000psFall

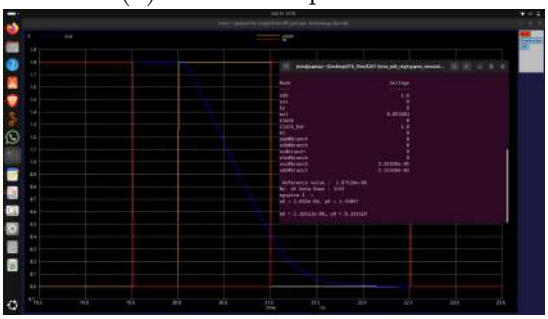
Figure 4.9: Transition Time Simulation for Capacitance 10fF



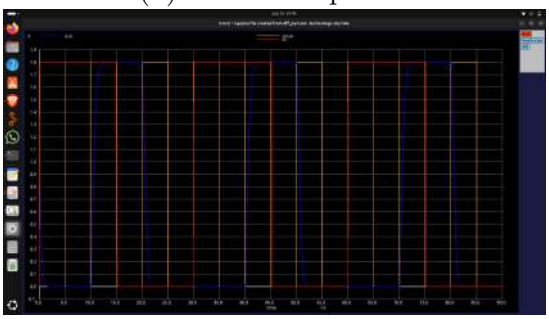
(a) DFF100f10psOverall



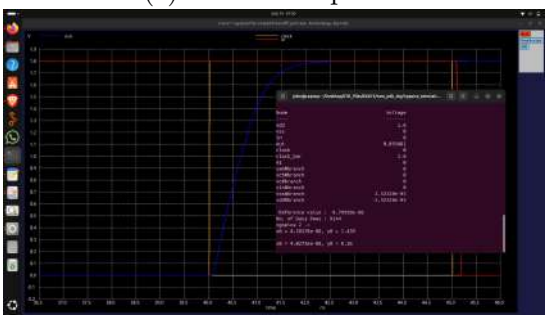
(b) DFF100f10psRise



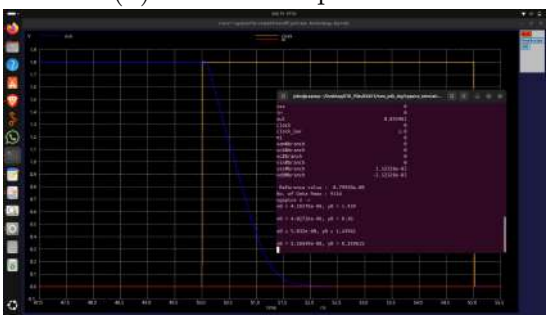
(c) DFF100f10psFall



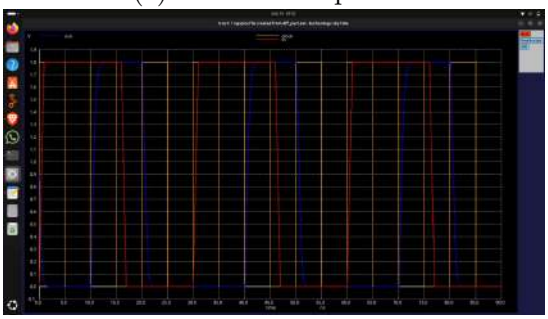
(d) DFF100f100psOverall



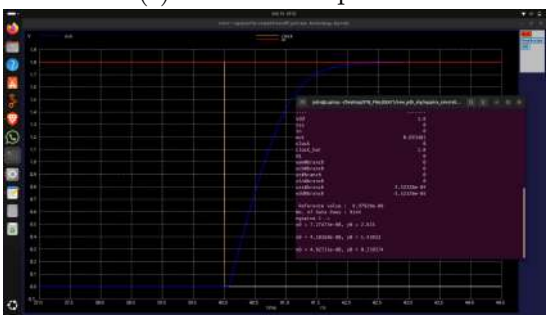
(e) DFF100f100psRise



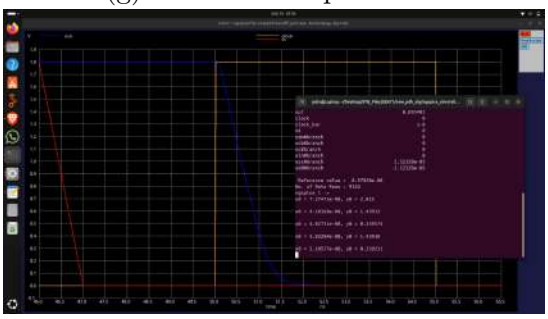
(f) DFF100f100psFall



(g) DFF100f1000psOverall



(h) DFF100f1000psRise



(i) DFF100f1000psFall

Figure 4.10: Transition Time Simulation for Capacitance 100fF

4.4.4 e) CLK-to-Q Delay Time Table

(i) Cell Rise Delay (in ns) [Input slew vs output capacitance]

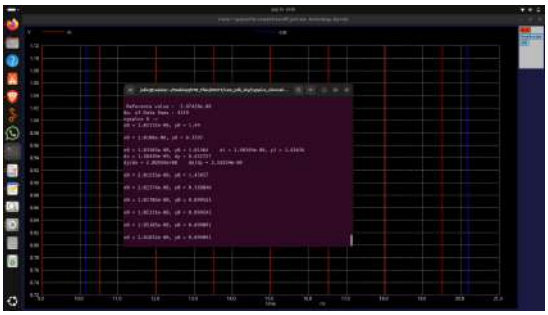
Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	0.3407	0.1765	0.1688
10 fF	0.2177	0.2055	0.2235
100 fF	0.6121	0.6051	0.5968

Table 4.9: Output Rise Delay for DFF

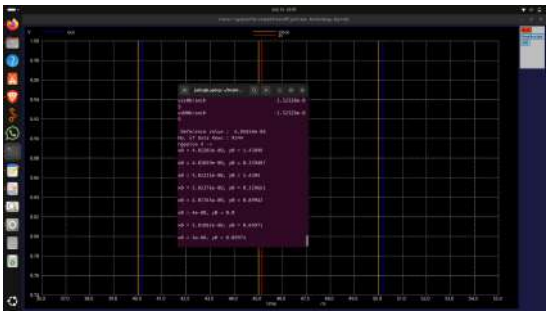
(ii) Cell Fall Delay (in ns) [Input slew vs output capacitance]

Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	0.6667	0.1882	0.1688
10 fF	0.25	0.2603	0.2353
100 fF	0.6897	0.7068	0.6774

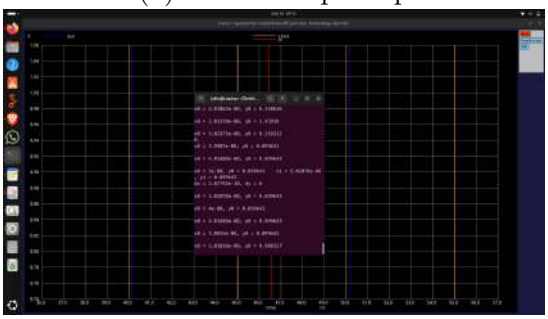
Table 4.10: Output Fall Delay for DFF



(a) DFF0.5f10psProp

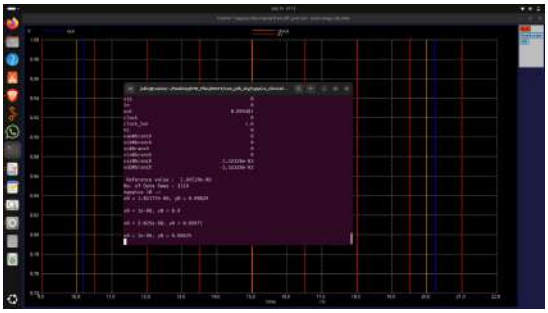


(b) DFF0.5f100psProp

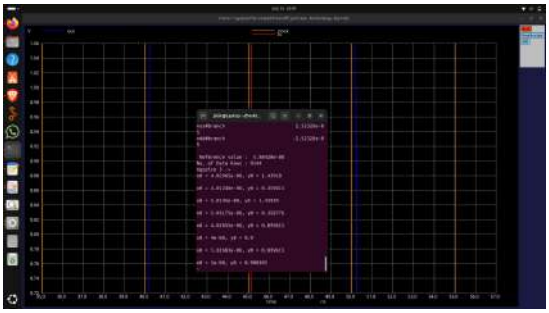


(c) DFF0.5f1000psProp

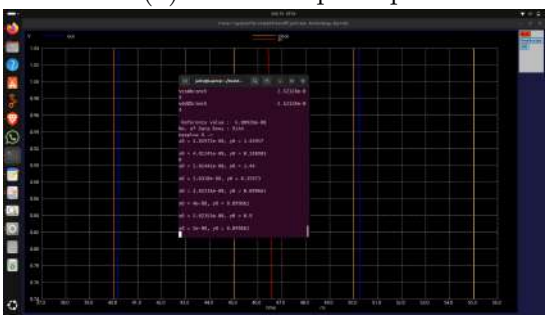
Figure 4.11: Transition Time Propagation for Capacitance 0.5fF



(a) DFF10f10psProp

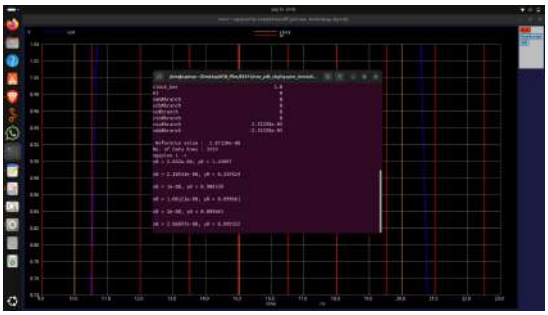


(b) DFF10f100psProp

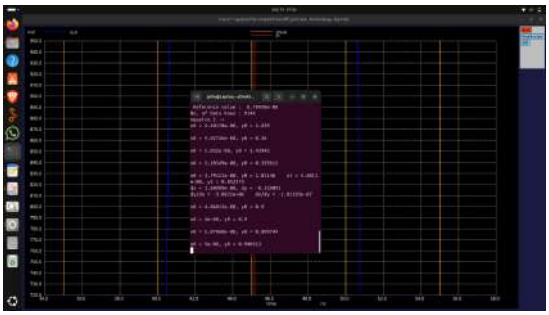


(c) DFF10f1000psProp

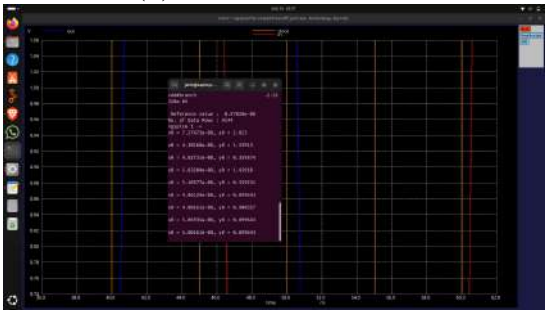
Figure 4.12: Transition Time Propagation for Capacitance 10fF



(a) DFF100f10psProp



(b) DFF100f100psProp



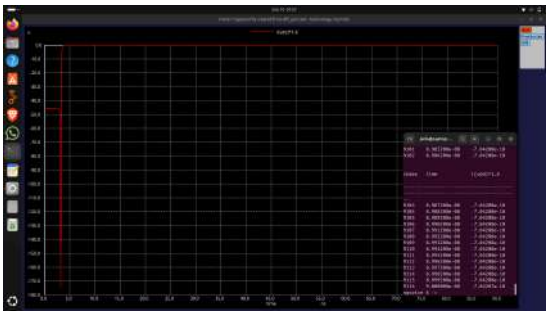
(c) DFF100f1000psProp

Figure 4.13: Transition Time Propagation for Capacitance 100fF

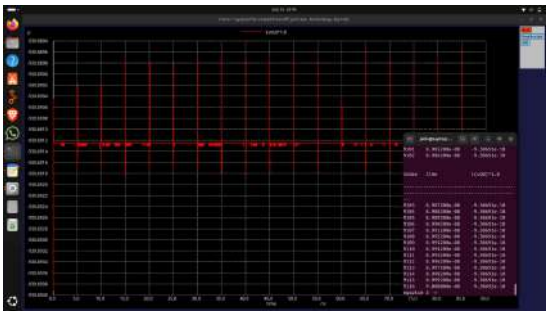
4.4.5 f) Static Power

Condition (CLK, D)	Power (nW)
00	0.704207
01	0.930692
10	0.927231
11	0.930692

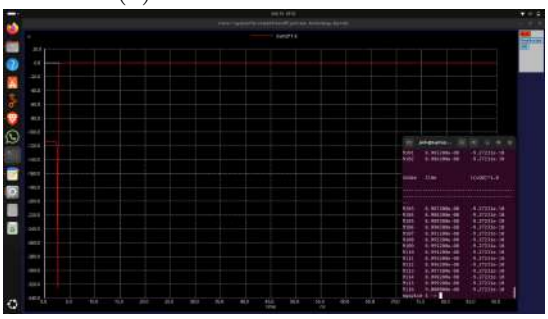
Table 4.11: Static Power for DFF



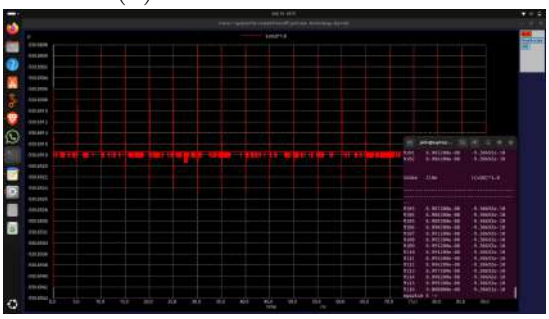
(a) Static Power DFF 00



(b) Static Power DFF 01



(c) Static Power DFF 10



(d) Static Power DFF 11

Figure 4.14: Static Power Simulation for DFF Condition(CLK, D)

4.4.6 g) Dynamic Power Table

(i) Rise Power (in nW) [Input slew vs output capacitance]

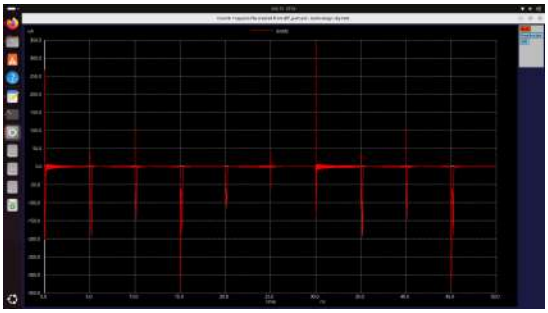
Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	3588.80	3979.99	3833.15
10 fF	7410.00	7569.00	8083.00
100 fF	47852.80	46759.90	47458.00

Table 4.12: Dynamic Rise Power for DFF

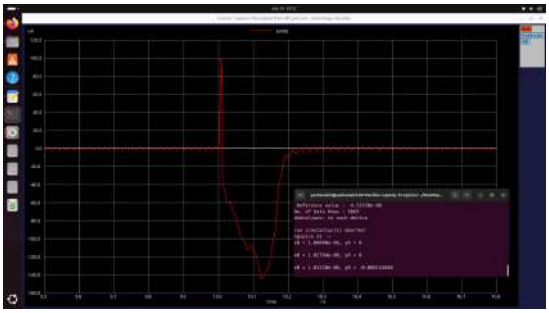
(ii) Fall Power (in nW) [Input slew vs output capacitance]

Capacitance (fF)	10 ps Slew	100 ps Slew	1000 ps Slew
0.5 fF	3787.00	3599.00	3945.00
10 fF	2600.00	2740.00	2702.00
100 fF	10390.00	11523.00	11229.00

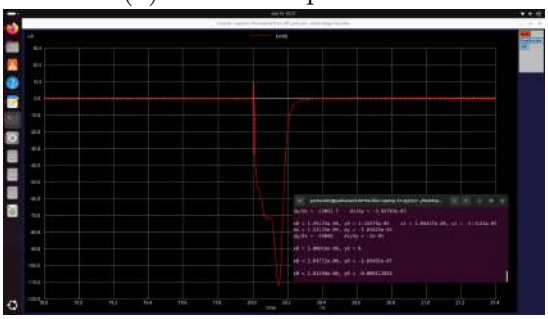
Table 4.13: Dynamic Fall Power for DFF



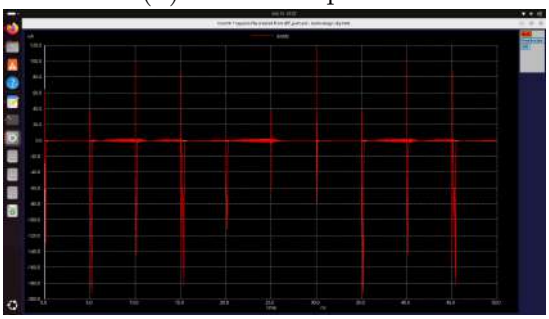
(a) DPP0.5f10psOverall



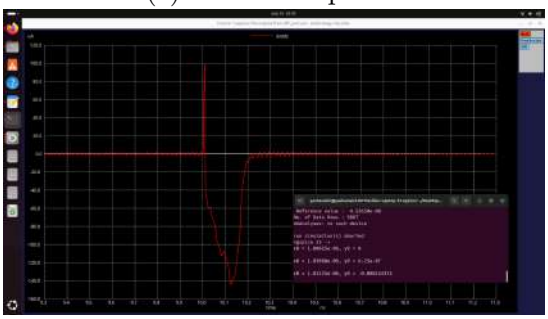
(b) DPP0.5f10psRise



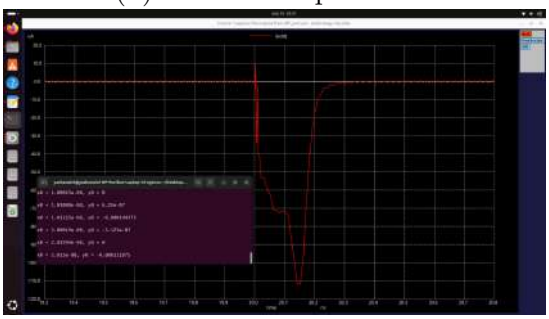
(c) DPP0.5f10psFall



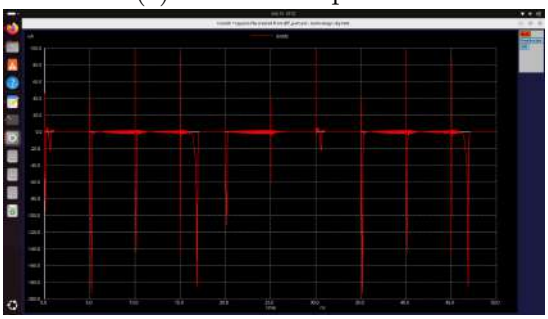
(d) DPP0.5f100psOverall



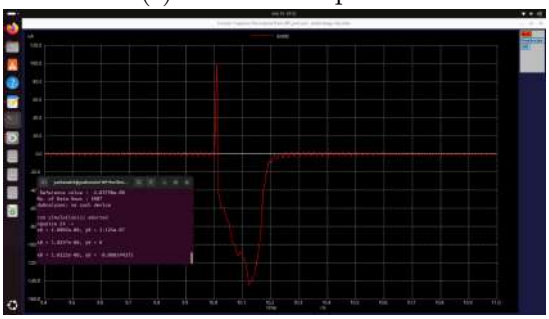
(e) DPP0.5f100psRise



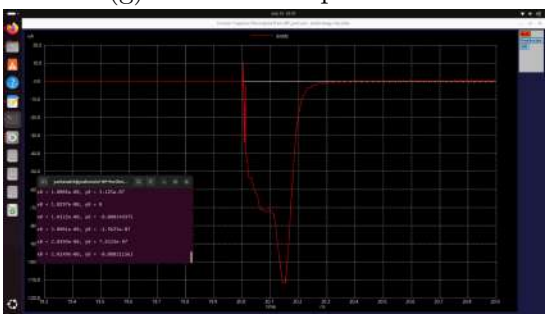
(f) DPP0.5f100psFall



(g) DPP0.5f1000psOverall

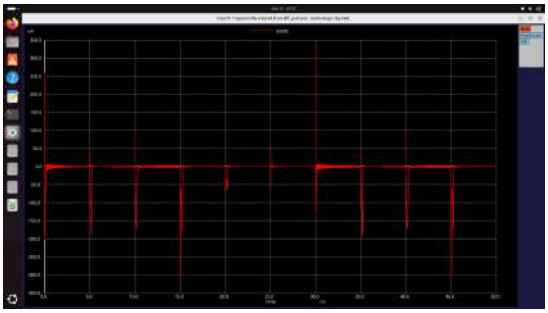


(h) DPP0.5f1000psRise

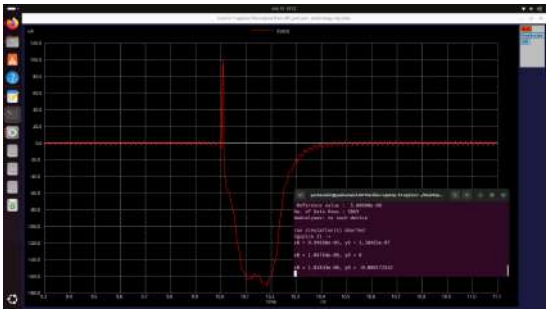


(i) DPP0.5f1000psFall

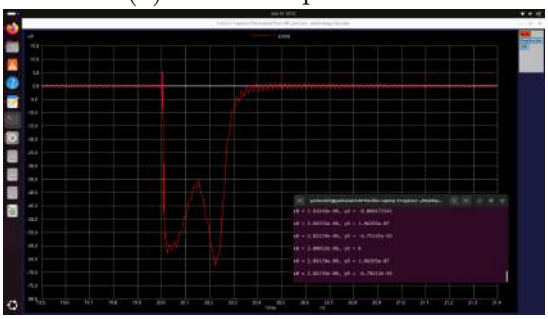
Figure 4.15: Dynamic Power Simulation for Capacitance 0.5fF



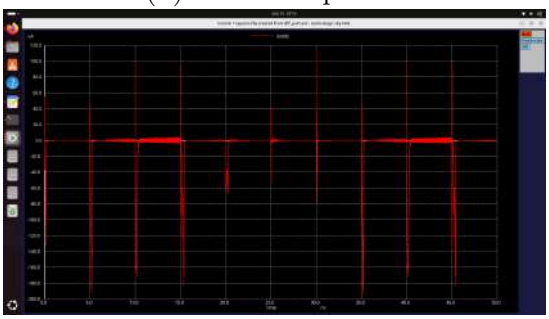
(a) DPP10f10psOverall



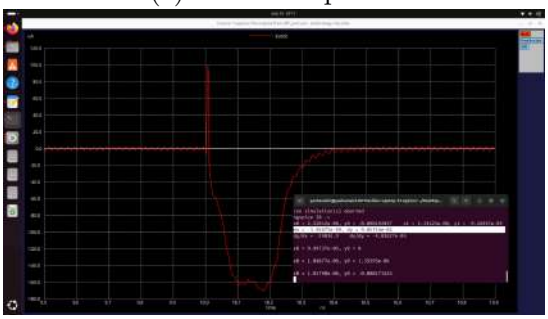
(b) DPP10f10psRise



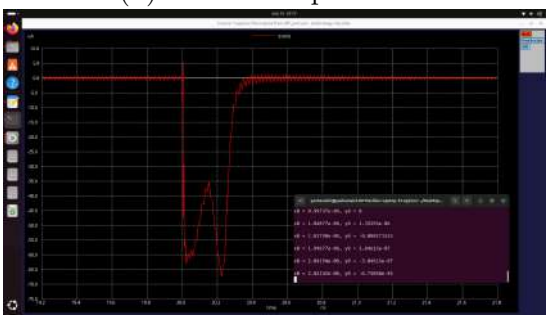
(c) DPP10f10psFall



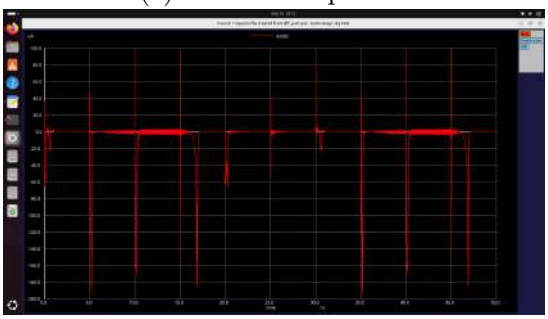
(d) DPP10f100psOverall



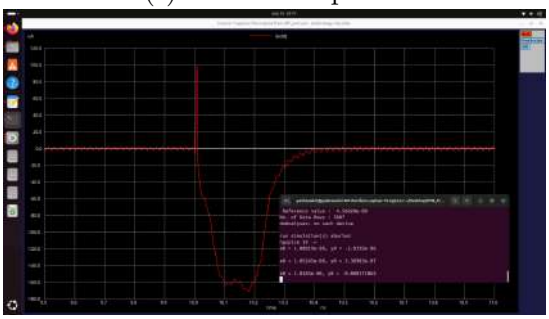
(e) DPP10f100psRise



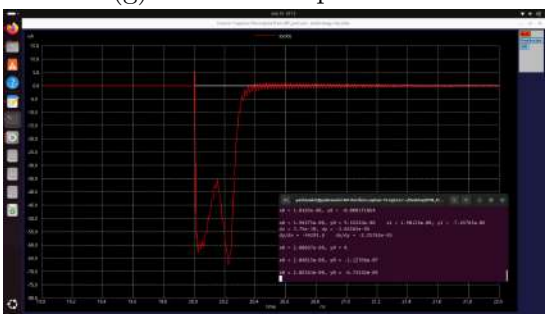
(f) DPP10f100psFall



(g) DPP10f1000psOverall

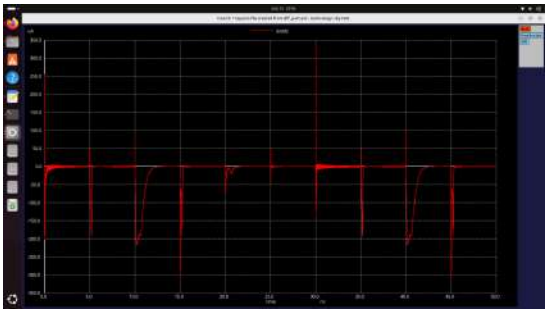


(h) DPP10f1000psRise

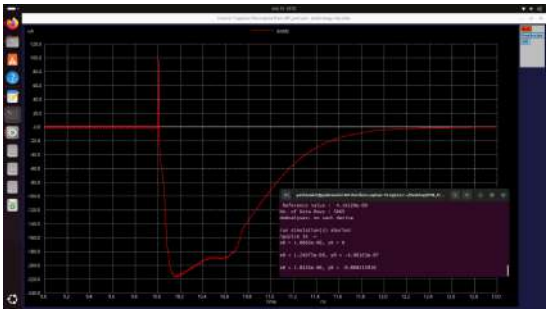


(i) DPP10f1000psFall

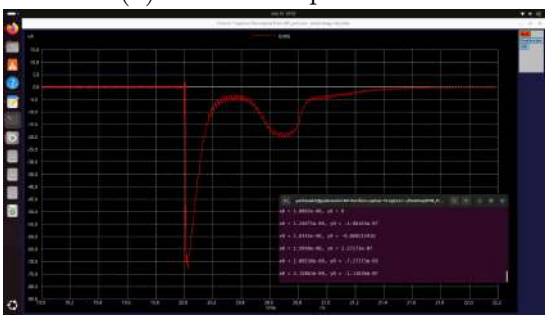
Figure 4.16: Dynamic Power Simulation for Capacitance 10fF



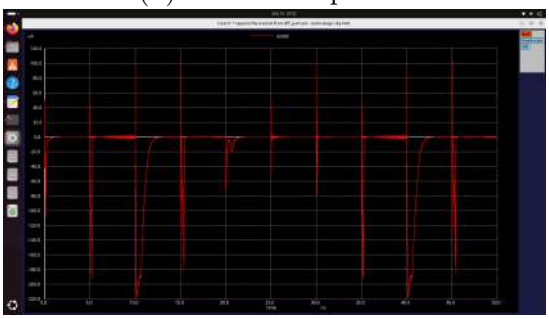
(a) DPP100f10psOverall



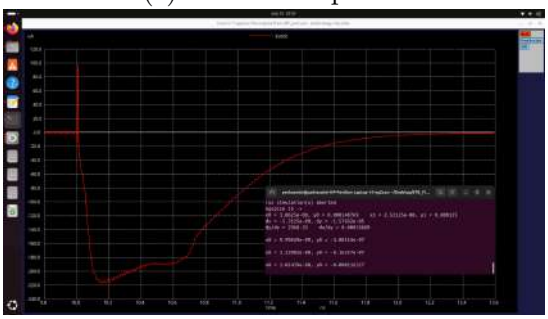
(b) DPP100f10psRise



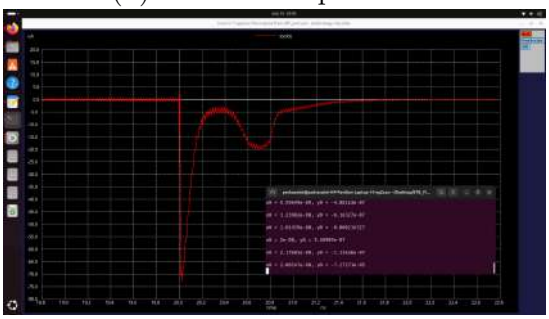
(c) DPP100f10psFall



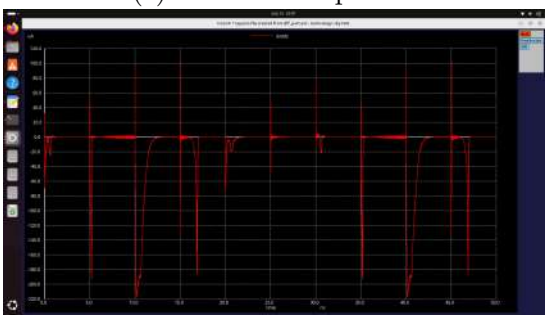
(d) DPP100f100psOverall



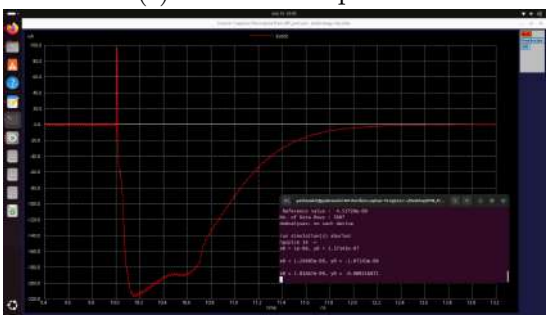
(e) DPP100f100psRise



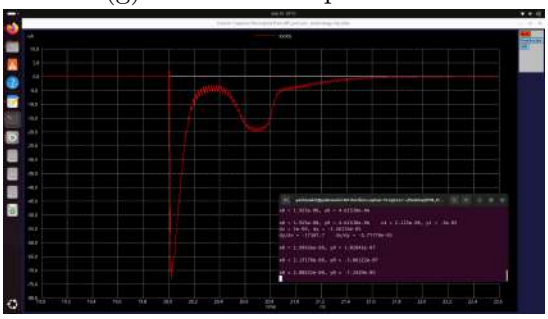
(f) DPP100f100psFall



(g) DPP100f1000psOverall



(h) DPP100f1000psRise



(i) DPP100f1000psFall

Figure 4.17: Dynamic Power Simulation for Capacitance 100fF

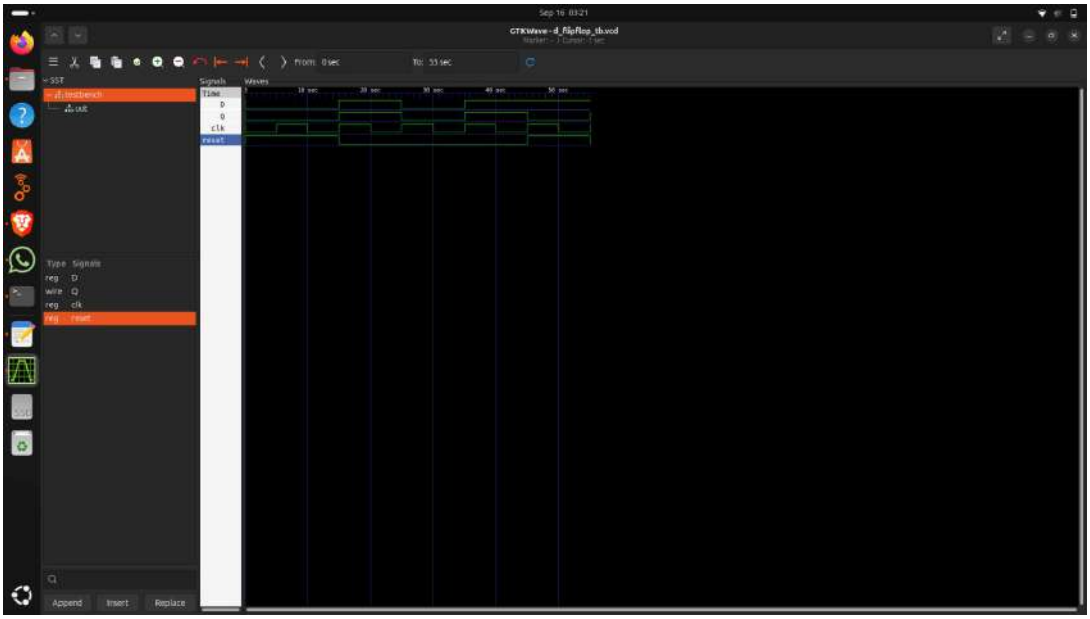
4.5 HDL Functional Definition

The following Verilog code implements the delay flop.

```
module d_flipflop (
    input wire D,       // Data input
    input wire clk,     // Clock input
    input wire reset,   // Reset input (active high)
    output reg Q        // Output
);

// On rising clock edge or reset
always @(posedge clk or posedge reset) begin
    if (reset)
        Q <= 1'b0;  // Set Q to 0 when reset is active
    else
        Q <= D;     // Capture D on the rising clock edge
end

endmodule

// Testbench for D Flip-Flop
module testbench;

    reg D;
    reg clk;
    reg reset;
    wire Q;

    // Instantiate the D Flip-Flop
    d_flipflop uut (
        .D(D),
        .clk(clk),
        .reset(reset),
        .Q(Q)
    );

    // Clock generation
    always begin
        clk = 0; #5;  // 5ns low
        clk = 1; #5;  // 5ns high
    end

    // Test stimulus
    initial begin
        $dumpfile("d_flipflop_tb.vcd");  // Dump file for waveform
        $dumpvars(0, testbench);
```

```
        // Initialize inputs
        D = 0;
        reset = 1;  // Apply reset
        #15;
        reset = 0;  // De-assert reset

        // Test the D Flip-Flop behavior
        D = 1; #10;
        D = 0; #10;
        D = 1; #10;

        // Test reset again
        reset = 1; #10;
        reset = 0;

        $finish;
    end

endmodule
```

4.5.1 VHDL Output for DFF



(a) VHDL Output for DFF

Figure 4.18: VHDL Output for DFF

Chapter 5

Team Contributions

5.1 Samridhi's Responsibilities

- Created the MAG and LEF files for the NOR gate and completed its timing characterization.
- Worked on the power and timing characterization for the buffer, created the buffer's Verilog model, and performed the LVS check to ensure layout accuracy.
- Verified the functionality of the D Flip-Flop (DFF) within the buffer and reviewed the Verilog description for the DFF.

5.2 Yashaswini's Responsibilities

- Designed the MAG file for the buffer, created its LEF file, and completed its timing characterization.
- Performed setup and hold time characterization.
- Managed the LEF creation, power characterization, and provided the netlist and Verilog model for the D Flip-Flop (DFF).
- Measured the input capacitance of the DFF for accurate performance.

5.3 Jatin's Responsibilities

- Created the LEF file for the buffer, performed timing characterization, and handled power characterization.
- Conducted the power and timing characterization for NOR Gate B.
- Provided the buffer netlist and compiled the required library documentation of combinational circuits.

5.4 Virti's Responsibilities

- Developed the MAG file for the D latch and D Flip-Flop (DFF) and the Transmission gate MAG file.
- Generated the LEF files and handled both the timing and power characterization for the NOR gate.
- Provided the netlist for the NOR gate, contributed to report writing, and managed the library documentation of the DFF.

Chapter 6

Conclusion

This project involved the successful design and characterization of three standard cells: the **Buffer (buf)**, **Delay Flop (dfxtp)**, and **2-input NOR with an inverted input (nor2b)**. Each of these cells was thoroughly verified through NGSpice simulations, with the corresponding layouts created and validated using Magic. Comprehensive timing, power, and input capacitance characterizations were conducted, ensuring accurate performance metrics. Additionally, all cells passed **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** validation, confirming both their manufacturability and functional correctness.