For Sequential cells, the following characterizations have to be performed and filled.

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 0.298 | 0.1999 | 0.24895 |
| CLK | 0.267 | 0.188 | 0.2275 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.136 | 0.8 |
| **1000 ps** | 0.44 | 0.45 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.25 | 0.9 |
| **1000 ps** | 0.42 | 0.43 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.16 | 0.7 |
| **1000 ps** | 0.53 | 0.67 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.33 | 0.95 |
| **1000 ps** | 0.47 | 0.52 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):** (please strictly consider 20% and 80% of VDD for transition time)

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.1092 | 0.1144 | 0.1144 |
| **10 fF** | 0.1703 | 0.1717 | 0.1731 |
| **100 fF** | 0.7443 | 0.7452 | 0.7437 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.1139 | 0.1148 | 0.1157 |
| **10 fF** | 0.1718 | 0.1725 | 0.1738 |
| **100 fF** | 0.7353 | 0.7349 | 0.7373 |

1. **CLK-to-Q Delay Time Table**: (delay between clock transition and data transition. Use 50% of CLK to 50% of output to simulate propagation delay).

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.3407 | 0.1765 | 0.1688 |
| **10 fF** | 0.2177 | 0.2055 | 0.2235 |
| **100 fF** | 0.6121 | 0.6051 | 0.5968 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.6667 | 0.1882 | 0.1688 |
| **10 fF** | 0.25 | 0.2603 | 0.2353 |
| **100 fF** | 0.6897 | 0.7068 | 0.6774 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 0.704207 |
| 01 | 0.930692 |
| 10 | 0.927231 |
| 11 | 0.930692 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 3588 | 3979 | 3833 |
| **10 fF** | 7410 | 7569 | 8083 |
| **100 fF** | 4785 | 4675 | 4745 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 3787 | 3599 | 3945 |
| **10 fF** | 2600 | 2740 | 2702 |
| **100 fF** | 10390 | 11523 | 11229 |