Hardware Modeling Using Verilog

Assignment- Week 1

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following VLSI design styles only allows layouts of functional blocks with fixed height?

a. Standard cell.
b. Full custom.
c. FPGA.
d. None of these.

Correct Answer: a

Detailed Solution:

In standard cell, the technology library contains optimized layouts of functional modules, each with fixed height.

Thus option (a) is the correct answer.

QUESTION 2:

Which of the following statement(s) is/are false?

a. FPGA based design is slower than standard cell based design.
b. Standard cell based design is faster than full custom design.
c. FPGA based design is faster than full custom design.
d. None of these.

Correct Answer: b, c

Detailed Solution:

In decreasing order of speed, we can order the design styles as full custom, semi custom (or standard cell), gate array, FPGA.

Hence, the statements (b) and (c) are false.

QUESTION 3:

Which of the following design descriptions represent a netlist?

a. A set of gates and their interconnections.
b. Interconnection of register transfer level components.
c. The truth table representation of a function.
d. All of these.

Correct Answer: a, b

Detailed Solution:

A netlist refers to a set of building blocks and their interconnection. Both (a) and (b) satisfy these criterial

Thus options (a) and (b) are correct.

QUESTION 4:

Which of the following is carried out before the others in a typical VLSI design flow?

a. Logic design.
b. Data path design.
c. Physical design.
d. Layout design.

Correct Answer: b

Detailed Solution:

Among the steps mentioned, data path design is carried out first, followed by logic design, and then physical design, and then layout design.

Thus correct option is (b).

QUESTION 5:

What are the basic building blocks in a switch level description of s VLSI design?

a. Gates
b. RTL level modules
c. Transistors
d. Relay switches

HINT: (If options a, b and c are all correct, select option d as the answer.)

Correct Answer: c

Detailed Solution:

Switch level description is a netlist of transistors and the way they are interconnected.

Thus correct option is (c).

QUESTION 6:

Which of the following is used to specify a design in Verilog?

a. A Verilog module.
b. A Verilog test bench.
c. A Verilog design bench.
d. None of these.

Correct Answer: a

Detailed Solution:

A Verilog module is used to describe the specification of a design, whereas a test bench is used to specify the input stimulus and output behavior during simulation. There is nothing called “design bench”.

Thus options (a) is true.

QUESTION 7:

The process of converting a function specification to a netlist of gates/modules is called:

a. Evolution
b. Simulation
c. Synthesis
d. Emulation

Correct Answer: c

Detailed Solution:

Converting a design specification into the corresponding implementation is called synthesis.

The correct option is (c).

QUESTION 8:

For FPGA design style, what is the full form of CLB?

a. Combinational logic block.
b. Constant logic bit.
c. Cumulative logic bias.
d. Combinational latch block.

Correct Answer: a

Detailed Solution:

The full form of CLB is combinational logic block.

Thus option (c) is correct.

QUESTION 9:

The truth table description of a function represents a behavioral description.

a. True
b. False

Correct Answer: a

Detailed Solution:

The truth table specifies the input-output behavior of a function, without specifying its implementation. It represents a behavioral description.

The correct option is (a).

QUESTION 10:

How many distinct functions of 3 variables are possible?

a. 8
b. 256
c. 9
d. None of these

Correct Answer: b

Detailed Solution:

The number of distinct functions of n variables is given by 2^(2^n).

Thus option (b) is correct.

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 2

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 X 1 = 10**

QUESTION 1:

A Verilog module can describe a hardware component at which level of abstraction?

a. Behavioral level

b. Netlist of gates

c. Netlist of other Verilog modules

d. All of these

Correct Answer: d

Detailed Solution:

A Verilog module can represent a hardware component at any level of design abstraction (e.g. behavioral, logical, hierarchical, etc.). For hierarchical design, the component sub modules are instantiated within another module as many times as required.
Thus option (d) is correct.

QUESTION 2:

Given the Verilog code, which of the following statement(s) is/are true?

```
module fun (f, a, b, c );
   input a, b, c ;
   output f;
   wire f, t1, t2;
   assign t1 = a ^ b ;
   assign t2 = b ^ c;
   assign f = t1 ^ t2 ;
endmodule
```

a. It represents behavioral description of the Boolean function f = a xor c.

b. It represents behavioral description of the Boolean function f = a and b.

c. It represents behavioral description of the Boolean function f = a or b.
d. None of these.

Correct Answer: a

Detailed Solution:

The assign statement in Verilog can be used to specify functional assignments at the behavioral level.

Here f = (a ^ b) ^ (b ^ c) = a ^ c, since b ^ b = 0 .
Thus option (a) is correct.

QUESTION 3:

Which of the following statement(s) is/are true for the "assign" statement?

a. A register type variable can be assigned a value.
b. A net type variable can be assigned a value.
c. No value can be assigned.
d. None of these.

Correct Answer: b

Detailed Solution:

In assign statement a net type variable can appear at both sides of equal to (=) operator whereas a register type variable can only appear at the RHS.

The correct option is (b).

QUESTION 4:

Given the Verilog code segment:

```
input a, b, c, d;
output f;
wire f1, f2;
assign f1 = a & c;
assign f2 = ~(f1 | b);
```

What will be the values of f1 and f2 if a = 0, b = 1, and c = 1?

a. f1 = 0, f2 = 0
b. f1 = 0, f2 = 1
c. f1 = 1, f2 = 0
d. f1 = 1, f2 = 1

Correct Answer: a

Detailed Solution:
Here, f1 = a & c = 0 & 1 = 0
f2 = ~(f1 | b) = ~(0 | 1) = 0

The correct option is (a).

QUESTION 5:

Which of the following statement(s) is/are true regarding the Verilog module shown below?

```
modulefun3 (f, a, b, clk);
      input [7:0] a, b;
      input clk;
      output f;
      integer f;
      always @(negedge clk)
      begin
            f = a + b;
      end
endmodule
```

a. The size of f will be inferred as 8 bits
b. The size of f cannot be inferred
c. The size of f will be inferred as 9 bits
d. None of these

Correct Answer: c

Detailed Solution:
The default size of integer data type is 32-bit and during synthesis, CAD tool can perform a data flow analysis to reduce the size. The sum of two 8-bit numbers produces an output of 9 - bits.

Thus option (c) is true.

QUESTION 6:

Consider the Verilog code presented below:

```
reg [0:3] data1;
reg [0:3] data2;
reg [0:3] res;
res = data1 ^ data2;
```

What will be the value of "res" after simulating the code with the initialization1 data1 = 4'b0011 and data2 = 4'b0110?

a. 4'b0111.
b. 4'b0011.
c. 4'b0101.
d. None of these.

Correct Answer: c

Detailed Solution:

The exclusive-or of 0011 and 0110 is 0101. Thus option (c) is correct.

QUESTION 7:

Consider the Verilog code for declaring a multi-dimensional array:

```
reg [10:0] data[0:7];
```

Which of the following assignment statement(s) is/are correct?

a. data[0] = 8'b11111111;
b. data[0] = 11'b0;
c. data[0] = 1'b1;
d. All of these.

Correct Answer: d

Detailed Solution:
The declaration defines 8 11-bit registers and the result of all these assignments will be:

Assignment	data[0]
data[0] =8'b11111111	00011111111
data[0] = 11'b0	00000000000
data[0] = 1'b1	00000000001

All the three assignments are correct.
Thus option (d) is correct.

QUESTION 8:

Which of the following statement(s) is/are true about defining constant in Verilog?

a. The statement `parameter H = 25;` defines a constant of size 4 -bit.
b. The statement `parameter H = 36;` defines a constant of size 32 -bit.
c. The statement `parameter H = 4'b1011;` defines a constant of size 4-bit.
d. None of these.

Correct Answer: b, c

Detailed Solution:
Defining constants in Verilog, if the size of the value is not explicitly mentioned, will be 32 -bits.
Thus options (b) and (c) are true.

QUESTION 9:

Which of the following logic expressions is correct? Assume that variable 'b' is a 1-bit wire and 'z' and 'x' denote high impedance state and unknown logic state respectively.

a. b & x = x
b. b | x = x
c. b ^ x = x
d. All of the above

Correct Answer: c

Detailed Solution:

Option (a) and (b) are not correct since 0 & x = 0 and 1 | x = 1. For logic values 0, 1, and z of variable b, the XOR operation b ^ x produces the result x.

Thus, option (c) is the correct answer.

QUESTION 10:

Consider the following Verilog code:

```
b = {2'b01, {2{2'b00}}, 2'b10};
```

The value assigned to b will be _____ (in decimal). Assume that b is an 8-bit reg type variable.

Correct Answer: 66

Detailed Solution:

2'b01 is 01

{2{2'b00}}, here repeat 00 twice, which is 0000

2'b10 is 10

Concatenating them, we get binary 01000010

Binary 01000010 is decimal 66.

Thus, the correct value is 66.

**********END*******

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Hardware Modeling Using Verilog

Assignment- Week 3

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 12 **Total mark: 12 X 1 = 12**

QUESTION 1:

Which of the following statements is/are true for the "assign" statement in Verilog?

a. It implements continuous assignment of the expression specified on the right - hand side to a "net" type variable specified on the left-hand side.
b. It implements continuous assignment of the expression specified on the right - hand side to a "reg" type variable specified on the left-hand side.
c. It can be used to assign values to a "reg" type variable in synchronism with a clock.
d. None of these.

Correct Answer: a

Detailed Solution:

For the "assign" statement, the left-hand side can only be a "net" type variable, and cannot be a "reg" type variable. It models a continuous assignment, where the right-hand side can be any expression consisting of "net" and "reg" type variables. It cannot be used to assign values in synchronism with a clock.

Thus, the correct answer is (a).

QUESTION 2:

Which of the following are true for the following code segment?

```
input [3 :0] a;
input [3:0] b;
input sel;
output [3:0] f;
assign f = sel? a : b;
```

a. One 4-to-1 multiplexer will be generated.
b. Four 2-to-1 multiplexers will be generated.
c. One 4-to-1 and one 2-to-1 multiplexer will be generated.

d. None of these.

Correct Answer: b

Detailed Solution:

The conditional statement "?" will generate a 2-to-1 multiplexer, with "sel" as the select input. The variables "a", "b", and "f" are all 4-bit vectors; hence, four 2-to-1 multiplexers will be generated.

The correct answer is (b).

QUESTION 3:

Which of the following constructs will be generating a demultiplexer, where "a," "b," and "c" are variables?

a. assign a = b[c];
b. assign b[c] = a;
c. assign a = b[c] & ~b[~c];
d. assign a = b & ~c

Correct Answer: b

Detailed Solution:

A demultiplexer will be generated if the L HS of an assignment is an array reference with a variable as index (as in option b).

The correct option is (b).

QUESTION 4:

What does the following code segment implement?

```
q1 = ~ (q2 | y);
assign q2 = ~ (x | q1);
```

a. A 1-bit flip-flop with clocked input.
b. A 2-bit right-shift register.
c. Two NOR gates connected in cascade.
d. A 2-bit comparator.
e. None of these.

Correct Answer: e

Detailed Solution:

The first NOR will have "y" and "q2" as inputs and give "q1" as output. The second NOR will have "x" and "q1" as inputs and give "q2" as output. This corresponds to a pair of cross-coupled NOR gates are used to build a one-bit latch.

The correct answer is (e).

QUESTION 5:

Which of the following is/are true for the "initial" procedural block in Verilog test benches?

a. It specifies a procedural block that is executed repeatedly.
b. It specifies a procedural block that can be used for synthesis.
c. It specifies a procedural block that is executed only once.
d. None of these.

Correct Answer: c

Detailed Solution:

The "initial" block is used only in test benches, and cannot be used to write a module for synthesis. It is executed only once during simulation, and is typically used to apply input stimulus to the module under test.

The correct option is (c).

QUESTION 6:

What will be the time period of the repetitive signal "stim" generated by the following code segment?

```
initial stim = 1'b0;
always #7 stim = ~stim;
```

a. 0
b. 7
c. 14
d. None of these.

Correct Answer: c

Detailed Solution:

The "initial" block initializes the "stim" signal to 0 at time 0. The "always" block toggles "stim" with a delay of 7 time units. Clearly, the period of the clock is 2 x 7 = 14 time units.
Hence, the correct option is (c).

QUESTION 7:

Which of the following event expressions can be used to specify a procedural block that will execute whenever there is a change in the state of the signal "clk"?

a. always @(posedge clk)
b. always @(negedge clk)
c. always @(clk=0 or clk=1)
d. always @(clk)
e. None of these.

Correct Answer: d

Detailed Solution:

Options (a) and (b) specify edge-triggered execution with respect to the signal "clk". Option (c) is not valid. Option (d) specifies the event expression that is true whenever "clk" changes state. Thus, option (d) is correct.

QUESTION 8:

Which of the following is true for the following module?

```
module guess (a, b);
  input [1:0] b;
  output reg a;
  always @(b)
    begin
      if (b == 2'b00) a = 1'b1;
      else if (b == 2'b11) a = 1'b1;
  else a = 1'b0;
    end
endmodule
```

a. A combinational circuit implementing an XOR function will be generated.
b. A combinational circuit implementing an AND function will be generated.
c. A latch will be generated for the output “a.”
d. None of these.

Correct Answer: a

Detailed Solution:

Assignment to variable “a” is specified for all values of the input “b,” and hence a combinational circuit will be generated. “a” is assigned 0 if “b” is neither 00 nor 11. Hence, it implements the XNOR function.

QUESTION 9:

In which of the following case(s), the synthesis tool will infer a sequential circuit from the description of an always block?

a. Every branch of a conditional statement defines all the outputs.
b. Every branch of a case statement defines all outputs.
c. Some branches of a case statement do not have defined outputs.
d. Some branches of conditional statements do not have defined outputs.
e. None of these.

Correct Answer: c, d

Detailed Solution:

The synthesis tool will generate a sequential circuit (latch or register) when the outputs are not defined for every branch of a conditional or case statement.
The correct options are (c) and (d).

QUESTION 10:

Consider the following code segment:

```
reg [0:7] a, b, c, d;
     initial begin
     #4 a = 10; b = 8; c = 2; d = 15;
     #4 a = 4; b = a; c = b; d = c;
end
```

What will be the values of variables a, b, c, and d after a time interval of 10 units?

a. a = 10, b = 8, c = 2 and d = 15.
b. a = 4, b = 8, c = 2 and d = 15.
c. a = 4, b = 4, c = 4 and d = 4.
d. None of these.

Correct Answer: c

Detailed Solution:

Since the initial block uses blocking assignments, the values of variables after a time interval of 4 units will be a = 10, b = 8, c = 2, and d = 15, and after a time interval of 8 units, all variables will be updated to the value 4. The values will not change any further till time 10.
Thus, option (c) is correct.

QUESTION 11:

Given the following Verilog code:

```
reg clk;
     integer y;
     initial clk = 1'b0;
     always #5 clk = ~clk;
     initial
          begin
               y = 2435;
               while (y >= 45) #5 y = y >>1;
          end
```

The while loop will be iterated _____ number of time.

Correct Answer: 6

Detailed Solution:

The while loop executes as long as y >= 45. On each iteration, y is halved using right shift. Starting from 2435, it takes 6 right shifts to drop below 45.

QUESTION 12:

Given the following Verilog code:

```
integer x, y;
reg clk;
always #5 clk = ~clk;
initial
     begin
          #5 clk = 1'b0; x = 0;
          #3 y = 12;
     end
initial
     begin
          #5 y =7;
          Repeat (y)
               #5 x = x + y;
     end
```

The final value of **x** will be _____.

Correct Answer: 49

Detailed Solution:

The variable y is updated to 7 before entering the repeat loop. The loop runs 7 times, adding 7 to x each time. Therefore, x = 0 + 7×7 = 49.

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 4

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

For the statement "A = B + C" inside a procedural block, which of the following alternatives are valid?

a. A is a reg type variable, B & C are wire type variables.
b. A & B are reg type variables, C is a wire type variable.
c. A is a wire type variable, B & C are reg type variables.
d. A, B and C are all wire type variables.

Correct Answer: a, b

Detailed Solution:

In a procedural assignment statement, only register type variables can be used in the left hand side. A wire type variable cannot be assigned a value within a procedural block.

Hence, the correct options are (a) and (b).

QUESTION 2:

For the following code segment, the final value of variable "c" will be _____.

```
integer  a, b, c;
initial
  begin
    a = 20; b = 2; c = 15;
    a = b * c;
    b = a - 12;
    c = a + b;
  end
```

HINT: (Please provide numeric answer, e.g. 37, do not type thirty seven**.)**

Correct Answer: 48

Detailed Solution:

In blocking assignments, statements are executed one after the other.

First assignment: a = 2 * 15 = 30

Second assignment: b = 30 – 12 = 18

Third assignment: c = 30 + 18 = 48

Thus, final value of variable "c" will be 48.

QUESTION 3:

For the following code segment, the final value of variable "c" will be _____.

```
integer  a, b, c;
initial
  begin
    a = 20; b = 2; c = 15;
  end
initial
  begin
    a <= #5  b * c;
    b <= #5  a - 12;
    c <= #5  a + b;
  end
```

HINT: (Please provide numeric answer, e.g. 53, do not type fifty three**.)**

Correct Answer: 22

Detailed Solution:

In non-blocking statements inside a procedural block, all right hand side expressions are evaluated in parallel, and are assigned to the left hand side variables all together.

First assignment: a = 2 + 15 = 30

Second assignment: b = 20 – 12 = 18

Third assignment: c = 20 + 2 = 22

Thus, final value of variable "c" will be 22.

QUESTION 4:

What will the following code segment do?

```
always @(posedge clock)
  begin
    x = z;
    y = z;
    z = x;
  end
```

a. Shift the values stored in the three variables.
b. All the variables will get the value previously stored in “x”
c. All the variables will get the value previously stored in “y”.
d. All the variables will get the value previously stored in “z”.

Correct Answer: d

Detailed Solution:

Because the assignments are blocking, first, the value of “z” will be assigned to “x”, and then “z” will be assigned to “y”, and then the new value of “x” will be assigned to “z”. Thus all the three variables will get the previous value stored in “z”.

Hence, the correct option is (d).

QUESTION 5:

If the 5-bit variable “data” declared as “`reg [4:0] data`” is initialized to 5’b01101, what will be its value after execution of the following code segment?

```
always @(posedge clock)
  begin
     data[4:0] <= data[4:0] >> 2;
  end
```

a. 5’b00110
b. 5’b00011
c. 5’b10100
d. None of these.

Correct Answer: b

Detailed Solution:

The RHS of the assignment will be data[4:0] >> 2 = 00011

Thus, the correct option is (b).

QUESTION 6:

What will the following code segment generate on synthesis?

```
always @(posedge clock)
  begin
    y = x;
    z = y;
  end
```

a. Two D flip-flops all fed with the data “x”.
b. A 2-bit shift register.
c. A 2-bit parallel-in parallel-out register.
d. None of these.

Correct Answer: a

Detailed Solution:

Since blocking assignment statements are executed sequentially one after another, the value of “x” will be first assigned to “y”, and then to “z”. Thus, the same input will feed both the D flip-flops in the synthesized circuit.

The correct option is (a).

QUESTION 7:

What will the following code segment generate on synthesis?

```
always @(posedge clock)
  begin
    y <= x;
    z <= y;
    w <= z;
  end
```

a. A 3-bit parallel-in parallel-out register.
b. Three D flip-flops all fed with the same input “z”.
c. A 3-bit shift register.
d. None of these.

Correct Answer: c

Detailed Solution:

Since we use non-blocking assignments, the values on the RHS are assigned to the variables on the LHS at the same time in synchronism with the clock. This will generate a 3-bit shift register.

Thus, the correct option is (c).

QUESTION 8:

What function does the following Verilog module realize in the final output “f”?

```
module mystery (f, a, b, c);
  input a, b, c;
  output f;
  wire t;
  xor G1 (t, a, b);
  xor G2 (f, t, c);
endmodule
```

a. The carry function of a full adder with inputs “a”, “b”, “c”.
b. The sum function of a full adder with inputs “a”, “b”, “c”.
c. 3-variable majority function with inputs “a”, “b”, “c”.
d. None of these.

Correct Answer: b

Detailed Solution:

This Verilog module will generate a 3-input xor function, which is basically the sum output of a full adder with inputs “a”, “b” and “c”.

Thus, the correct option is (b).

QUESTION 9:

Which of the following is/are true for “generate” blocks in Verilog?

a. Multiple copies of code blocks are generated dynamically before simulation or synthesis.
b. Can be used to instantiate multiple copies of some module.
c. Cannot be used along with a variable of type “genvar”.
d. None of these.

Correct Answer: a, b

Detailed Solution:

Both (a) and (b) are true for “generate” blocks; also they must be used along with some variable of type “genvar”.

Hence, the correct options are (a) and (b).

QUESTION 10:

Which of the following is/are ***not true*** for user defined primitives in Verilog?

a. Can be used to specify a combinational circuit with any number of outputs.
b. Can be used to specify a combinational circuit with a single output.
c. Can be used to specify a finite state machine with one or two state variables.
d. Can be used to specify a finite state machine with only one state variable.

Correct Answer: a, c

Detailed Solution:

We can specify a combinational circuit with only one output using user defined primitives.

Also, we can specify a FSM with only one state variable.

Hence, the correct options are (a) and (c).

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 5

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

A Verilog test bench is used for:

a. Synthesis of a Verilog module.
b. Formal verification of a Verilog module.
c. Simulation of a Verilog module.
d. None of these.

Correct Answer: c

Detailed Solution:

In Verilog, we use test bench to specify the stimulus and expected response, which are used for simulating a Verilog module.

The correct option is (c).

QUESTION 2:

Given the following Verilog code segment for simulating primitive **OR** gate operation:

```
module or_gate;
      reg a, b;
      wire f;
      or ggg (f, a, b);
      initial begin
            $dumpfile ("gate_response.vcd");
            $dumpvars (0, or_gate);
            $monitor ("f = %b", f);
            #5 a = 0; b = 0;
            #5 a = 0; b = 1;
            #5 a = 1; b = 0;
            #5 a = 1; b = 1;
      end
endmodule
```

The value of the variable f will be printed _____ number of times.

Correct Answer: 3

Detailed Solution:

The $monitor statement will print every time the value of the variable f is modified.

Initially when the $monitor statement is encountered at time 0 unit, the value of f is printed as unknown logic state, x. After time 5 unit simulating the or operation with logic value 00 for the inputs {a, b} when the output logic state of variable f is changed from x to 0, $monitor prints the value of f. Finally, at time 10 unit when for the input logic value 01 the state of variable f is changed from 0 to 1, f is printed.

Thus the state of variable f is printed 3 times during simulation.

QUESTION 3:

Assume that the `or` gate operation is defined in the following way:

```
module or (out, x, y);
      input x, y;
      output out;
      assign out = x | y;
endmodule
```

Simulating the above module using the test bench defined in **Q.2**, which of the following set of variables will be dumped in "`gate_response.vcd`" file.

a. `{x, y, out}`
b. `{a, b, f}`
c. `{x, y, out, a, b, f}`
d. `{f}`

Correct Answer: c

Detailed Solution:

In the test bench, since the parameters `or_gate` module and level 0 are passed to the "`$dumpvars`" directive, all the variables of `or_gate` module as well as the variables from the instantiated `or` module, i.e. `{a, b, f, x, y, out}` will be dumped.

The correct option is (c).

QUESTION 4:

Which of the following statement(s) is/are true for the "initial" block in a test bench?

a. It is executed only once.
b. It is executed repeatedly.
c. It is executed repeatedly until the end of simulation time is reached.
d. None of these.

Correct Answer: a

Detailed Solution:

The "initial" block in a Verilog test bench is executed only once.

The correct option is (a).

QUESTION 5:

Consider the following Verilog code:

```
and   #6    G1 (t1,A,B);
or    #18   G2 (t2,C,~B,D);
nor   #11   G3 (t3,E,F);
nand  #5    G4 (Y,t1,t2,t3);
```

If all the inputs A, B, C, D, E and F are fed with some logic value at the same time, after a delay of _____ time unit the correct logic value at the output port Y of nand gate will be observed.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 23

Detailed Solution:

Since the delay of OR gate is maximum (18 time unit), the input for the NAND gate will be stable after 18 time unit and the output of NAND gate will be observed after a delay of 5 time unit. Thus after feeding the input, an interval of 23 time unit will require to obtain the output of NAND gate.

QUESTION 6:

Which of the following(s) is/are the features of combinational circuits?

a. Output of the circuit depends on the present inputs and present state.
b. Output of the circuit depends only on the present inputs.
c. At any instance of time the circuit must be in one of the finite states.
d. None of these.

Correct Answer: b

Detailed Solution:

In a combinational circuit, the output depends only on the applied inputs. There are no flip-flops in the circuit, and hence there is no concept of states.

The correct option is (b).

QUESTION 7:

Which of the following statement(s) is/are true about Verilog test benches?

a. A test bench may contain more than one initial blocks.
b. A test bench may contain both initial and always blocks.
c. Input and output ports of the DUT require explicit connections to the test bench module.
d. All of these.

HINT: (If options a, b and c are all true, select option d as the answer.)

Correct Answer: d

Detailed Solution:

More than one "initial" procedural block can be defined in a testbench to provide input stimuli for a DUT. In testbench "always" block is mainly used for clock pulse generation. All input/output ports of the designed module must be connected explicitly to the testbench which is responsible for generating the input logic values including clock pulses during simulation. Thus statements (a), (b), and (c) are true.

The correct option is (d).

QUESTION 8:

Which of the following is/are true about the following verilog directive

```
`timescale 10ns / 10ps
```

a. The synthesis tool interprets 10 nanoseconds as unit of delay.
b. The directive is only considered during simulation and ignores during actual synthesis.
c. The simulator interprets 10 nanoseconds as unit of delay with a resolution of 10 picoseconds.
d. All of these.

Correct Answer: b, c

Detailed Solution:

The timescale directive is only considered during simulation, it is ignored by synthesis tool. Thus option (a) is false and option (b) is true. The simulator interprets 10ns as unit of delay with precision 10ps. Thus option (c) is true and option (d) is false.

QUESTION 9:

What will be the time period of the clock (**clk**) generated by the following code segment?

```
module test_dut;
reg clk
initial
      #2 clk = 1'b0;
always
      #4 clk = ~clk;
endmodule
```

a. 6 time units
b. 2 time units
c. 8 time units
d. None of these.

Correct Answer: c

Detailed Solution:

Thus the "clk" variable will be toggled after 4 time units, giving a time period of 4 + 4 = 8 time units.

The correct option is (c).

QUESTION 10:

Which of the following statements is/are true?

a. For both Mealy and Moore machines the present state and present input determines the next state.
b. In Mealy machine the output is associated with present state.
c. In More machine the output is associated with present state and present input.
d. Both Mealy and Moore machines are used to realize sequential circuit.

Correct Answer: a, d

Detailed Solution:

The next state is determined as a function of present state and present input for both Mealy and Moore machines. Thus option (a) is true. The output of Mealy machine is associated with present input and present state whereas output of Moore machine depends only on present state. Thus options (b) and (c) are false. Both state machines are used for realizing sequential circuit. Thus option (d) is also true.

The correct options are (a) and (d).

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 6

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 x 1 = 10**

QUESTION 1:

Which of the following statement(s) is/are true?

a. The data path contains only combinational circuit elements.
b. The data path may contain both combinational and sequential circuit elements.
c. The control path implements a finite-state machine.
d. The control path must contain only combinational circuit elements.

Correct Answer: b, c

Detailed Solution:

Both sequential and combinational circuit elements like registers and multiplexers can be found in a typical data path. All decision-making signals are part of the control path, which is typically implemented as a finite-state machine.

Thus options (b) and (c) are correct.

QUESTION 2:

Which of the following is/are true for a finite-state machine?

a. The output can depend on the applied (present) inputs as well as the present state.
b. The output depends only on the applied inputs.
c. The next state must only depend on the applied (present) inputs.
d. None of these.

Correct Answer: a

Detailed Solution:

A FSM consists of memory elements that define the state of the system. In general, both the primary outputs as well as the next state depends on the applied (present) inputs and also the present state of the system.

Thus option (a) is correct.

QUESTION 3:

Which of the following design convention(s) is/are typically used in Verilog during modeling data path and control path?

a. The state changes are carried out inside an “always” block triggered by clock.
b. The state changes are modeled using “assign” statements.
c. The control signals are generated in an “always” block using blocking assignments.
d. The control signals are generated in an “always” block using non-blocking assignments.

Correct Answer: a, c

Detailed Solution:

In designing data and control path, managing state changes are carried out using non-blocking statements in a clock triggered always block, and generation of control signals using blocking assignment statements inside separate always block(s) triggered by state variable.

Thus options (a) and (c) are correct.

QUESTION 4:

Which of the following statement(s) is/are ***false*** about the design for GCD computation module as discussed in lecture 26?

a. The control path of the design is realized as a Mealy machine.
b. The control path realizing a FSM takes as input the status signals that are generated by the data path.
c. The final result of GCD computation will be available in both A and B registers.
d. None of these.

Correct Answer: d

Detailed Solution:

Control signals for the design as discussed in Lecture 26 are generated based on current state as well as present inputs (Mealy machine), e.g. for present state S2 and input eq = 1 the control output signal "done" is set to 1 and next state to S5. Since the computation stops when the value of both registers A and B are equal, any of these register value can be used as the final result.

Thus option (d) is correct.

QUESTION 5:

Assume the clock pulse is generated in the following way:

```
reg clk = 0;
always #5 clk = ~clk;
```

Simulating the GCD computation modules discussed in lecture 26 with inputs

```
#3 start = 1'b1;
#10 data_in = 35;
#8 data_in = 20;
```

the outcome 5 will be observed after _____ (in decimal) clock periods.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 7

Detailed Solution:

The state transition is carried out at the positive clock edge and each positive clock edge will appear at an interval of 10 time units. The following table shows the GCD computation and state change with the time as the clock pulse appears:

Time	State	A	B
0	X	X	X
5	S0	X	X
15	S1	35	X
25	S2	35	20
35	S4	15	20
45	S3	15	5

55	S4	10	5
65	S4	5	5

Thus $\frac{65}{clock\ cycle\ time} = \frac{65}{10} = 6.5$ or 7 complete clock cycles will be required.

QUESTION 6:

Assume that registers M and Q of the sequential Booth's multiplier (discussed in lecture 27) are initialized with the values 136 and 118. Simulating the multiplier, _____ (in decimal) subtraction operations will be performed.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 2

Detailed Solution:

The multiplier $Q = 118 = 01110110$ with $Q_{-1} = 0$ have 2 "10" bit patterns. Thus 2 subtraction operations will be carried out.

QUESTION 7:

Assume that registers M and Q of the sequential Booth's multiplier (discussed in lecture 27) are initialized with the values 215 and 170. Simulating the multiplier, _____ (in decimal) subtraction operations will be performed.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 4

Detailed Solution:

The multiplier $Q = 170 = 10101010$ with $Q_{-1} = 0$ have 4 "10" bit patterns. Thus 4 subtraction operations will be carried out.

QUESTION 8:

For the 32-bit Booth's multiplier discussed in lecture 27, the number of latches/flip-flops required to realize the A, M and Q registers will be _____.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 96

Detailed Solution:

The memory requirement details are given below:

Component	Size
Register A	32-bit
Register M	32-bit
Register Q	32-bit

Thus 96 latches/flip-flops will be required to satisfy the memory requirements.

QUESTION 9:

Which of the following Verilog statement(s) are synthesizable?

a. The primitive logic gates “and”, “or”, “not”.
b. “if” statement.
c. Delay specified on primitive gates using “#”.
d. All of these.

HINT: (If options a, b and c are all false, select option d as the answer.)

Correct Answer: a, b

Detailed Solution:

The primitive logic gates and conditional constructs like “if” are synthesizable. However, delays specified along with primitive logic gates cannot be synthesized.

Thus options (a) and (b) are correct.

QUESTION 10:

Which of the following statements is true about the Verilog module as shown?

```
module guess (f, x, y, z);
      input x, y, z;
      output reg f;
      always @(x)
            if (x) f = y;
            else f = z;
endmodule
```

a. A MUX will be inferred on synthesis.
b. A flip-flop will be inferred for variable “f” on synthesis.
c. A latch will be inferred for variable “f” on synthesis.
d. None of these.

HINT: (If options a, b and c are all false, select option d as the answer.)

Correct Answer: c

Detailed Solution:

Since the event expression contains only x, a latch will be inferred for the “f” variable.

Thus option (c) is correct.

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 7

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 8 **Total mark: 8 x 1.25 = 10**

QUESTION 1:

Which of the following statement(s) defines a memory of size 64 X 16 bit?

a. `reg [15:0] mem [63:0];`
b. `reg [63:0] mem [15:0];`
c. `reg [0:15] mem [0:63];`
d. All of these.

HINT: (If options a, b and c are all correct, select option d as the answer.)

Correct Answer: a, c

Detailed Solution:

The declaration of type `reg [0:n-1] mem [0:m-1];` defines a m x n memory, i.e. a memory consisting of m number of n-bit words. Instead of [0:n-1], we can also write [n-1:0].

Thus options (a) and (c) are correct.

QUESTION 2:

Part of a Verilog module realizing a 512 X 8 bit memory is defined in the following way:

```
module memory (d_out, clk, read, write, address,...);
      input clk, read, write;
      input [A:0] address;
      ...
      output reg [B:0] d_out;
      reg [C:0] mem [D:0];
      ...
      always @ (negedge clk)
            if (read) d_out = mem[address];
      ...
endmodule
```

What will be the values of (A, B, C, D)? Assume 1K = 1024.

a. (9, 7, 7, 512);
b. (8, 7, 7, 511);
c. (8, 8, 8, 9);
d. None of these.

Correct Answer: b

Detailed Solution:

The memory of size 512 X 8 has $2^9 = 512$ words with word size 8 bit and accessing each word requires 9-bit address lines and 8-bit data lines.

Thus option (b) is correct.

QUESTION 3:

The maximum speedup that can be obtained by using an m-stage pipeline is upper bounded by:

a. m – 1
b. 2^m
c. m
d. None of these.

Correct Answer: c

Detailed Solution:

The speedup of a pipeline can at most approach m.

Thus options (c) is correct.

QUESTION 4:

What does the declaration "`reg mem[16:0][15:0]`" indicate?

a. A 2-dimensional array with 17 rows and 16 columns, where every element is a single bit.
b. An array of 16 elements, each containing 17 bits.
c. An array of 17 words, each word consisting of 16 bits.
d. None of these.

Correct Answer: a

Detailed Solution:

Here there is no size specifier after "reg", which indicates that each data element is 1-bit in size. The two dimensions after "mem" indicates that it is a 2-dimensional array of single-bit numbers

The correct option is (a).

QUESTION 5:

Assume that a computational task requires 100 ns in a non-pipelined processor for execution. 200 such tasks are assigned to a 4-stage pipelined processor with uniform stage delay of 30 ns each. Ignoring the pipeline latch delay, the speedup observed is _____ (in decimal).

HINT: (Provide numeric constant value as answer, e.g. 90.5.)

Correct Answer: 3.2 to 3.3

Detailed Solution:

Number of tasks is 200.

The time taken by non-pipelined processor is $= 200 \times 100$**ns = 20,000 ns**

Number of pipeline stages is 4

The time taken by pipelined processor is $= (200 + 3) \times 30$**ns = 6090 ns**

Thus speedup = 20,000 / 6,090 = 3.284

QUESTION 6:

A 5-stage pipelined processing unit has stage delays 150ns, 130ns, 120ns, 140ns, and 75ns. The latch delay in each stage of computation is 20ns. The total time to process 100 tasks will be _____ microseconds.

HINT: (Provide numeric constant value as answer, e.g. 90.)

Correct Answer: 17.6 to 17.7

Detailed Solution:

The maximum stage delay is = 150ns.

Latch delay is $= 20$**ns**

Pipeline clock period = 150 + 20 = 170 ns

Total time taken = (100 + 4) x 170 ns = 17,680 ns = 17.68 microseconds.

QUESTION 7:

The maximum frequency with which a pipeline can operate is determined by:

a) The fastest stage in the pipeline

b) The slowest stage in the pipeline

c) The average stage delay in the pipeline

d) Cannot say

Correct Answer: b

Detailed Solution:

The maximum frequency with which a pipeline can operate is determined by the slowest stage.

The correct option is (b).

QUESTION 8:

Which function is realized by the following Verilog module?

```
module guess(f, a, b, c);
      input a, b, c;
      output f;
      wire t1, t2;
      supply1 vdd;
      supply0 gnd;

      pmos p1(t1, vdd, a);
      pmos p2(f, t1, b);
      pmos p3(f, vdd, c);
      nmos n1(f, t2, a);
      nmos n2(f, t2, b);
      nmos n3(t2, gnd, c);
endmodule
```

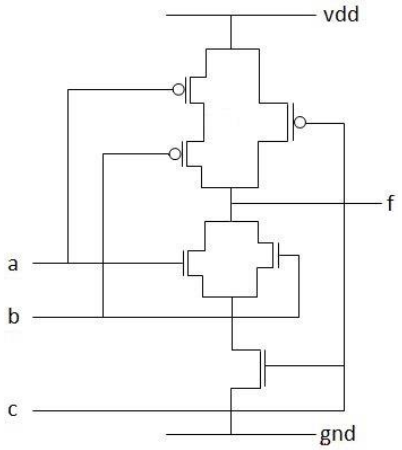
a. $f = ab + c$
b. A 3-input NAND function.
c. A 3-input NOR function.
d. None of these

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

Correct Answer: d

Detailed Solution:

The transistor network for the Verilog module is shown below:



Here the function is $f = \left((a + b)c\right)'$

$$= (a' + c')(b' + c')$$

Thus option (d) is the correct answer.

**********END*******

Hardware Modeling Using Verilog

Assignment- Week 8

TYPE OF QUESTION: MCQ/MSQ/SA

Number of questions: 10 **Total mark: 10 X 1 = 10**

QUESTION 1:

The number of general-purpose registers available in MIPS32 processor is:

a) 16
b) 32
c) 33
d) 64

Correct Answer: b

Detailed Solution:
MIPS32 has 32 general-purpose registers, R0 to R31.The correct option is (b).

QUESTION 2:

Given the MIPS32 code segment:

```
ADDI  R1, R0, 25
SUBI  R2, R1, -5
ADD   R3, R1, R2
```

The value at R3 after executing the above code segment will be _____.

a. 40

b. 50

c. 56

d. None of these.

Correct Answer: d

Detailed Solution:
The registers will be updated with values by the instruction sequence as follows:
$R1 = R0 + 25 = 0 + 25 = 25$
$R2 = R1 - (-5) = 25 + 5 = 30$
$R3 = R1 + R2 = 25 + 30 = 55$.
Thus, value of R3 after executing the code will be 55. The correct option is (d).

QUESTION 3:

For register values **R2=55** and **R6=42**, after execution of "**SLT R12, R2, R6**", the contents of **R12** will be _____.

HINT: (Please provide a numeric answer, e.g. 53, do not type fifty-three.)

Correct Answer: 0

Detailed Solution:

The SLT instruction will set the value of register R12 to 1 if R2 < R6, and will set it to 0 otherwise. In this example, since R2 > R6, R12 will become 0.

QUESTION 4:

What will be the hexadecimal machine code for the MIPS instruction "**AND R8, R3, R5**"?

a. $(08622000)_{16}$

b. $(08e22000)_{16}$

c. $(08624000)_{16}$

d. None of these

Correct Answer: d

Detailed Solution:

Opcode	Rs	rt	rd	Shamt	funct
AND	R3	R5	R8	00000	000000
000010	00011	00101	01000	00000	000000

$(0000\ 1000\ 0110\ 0101\ 0100\ 0000\ 0000\ 0000)_2 = (08654000)_{16}$. Thus, option (d) is correct.

QUESTION 5:

Given the following Verilog code segment:

```
reg clk1, clk2;
fun1 f1(f, a, b);
initial begin
     clk1 =0; clk2 = 0;
```

```
        repeat(4) begin
            #5 clk1 = 1; #5 clk1 = 0;
            #5 clk2 = 1; #5 clk2 = 0;
        end
    end
```

What is the duty cycle of clocks (clk1, clk2)? Duty cycle of a clock is defined as the fraction of a period of clock during which the clock is in active state.

a. (5,10)

b. (15, 5)

c. (0.25, 0.25)

d. (10, 5)

Correct Answer: c

Detailed Solution:

For clk1, HIGH duration = 5 time units, LOW duration = 20 time units.
Thus, duty cycle of clk1 is = **5**/2**0** =**0**.25

For clk2, HIGH duration = 5 time units, LOW duration = 20 time units.
Thus, duty cycle of clk1 is = **5**/2**0** =**0**.25

The correct answer is (c).

QUESTION 6:

The decimal number -11 is represented in 4-bit binary 2's complement notation. It is a sign extended to 16 bits. The sign-extended value in hexadecimal will be

a. FFFB
b. FFFC
c. FFEA
d. None of the above

HINT: (If options a, b and c are incorrect, select option d as the answer.)

Correct Answer: d

Detailed Solution:

Decimal -11 in 16-bit 2's complement:
11 in binary = 0000 0000 0000 1011.
Invert = 1111 1111 1111 0100.
Add 1 = 1111 1111 1111 0101.

So 16-bit representation of -11 = 1111 1111 1111 0101 = FFF5 (hex). So the correct answer is (d).

QUESTION 7:

Which of the following statement(s) is/are true about usage of the **HALTED** signal in the Verilog implementation of the processor as discussed in the lectures?

a. To halt the processor by sending a signal from an external device.
b. To indicate that the instructions after the HLT instruction should not make any changes.
c. To indicate that the processor has started its execution.
d. None of these.

HINT: (If options a, b, and c are incorrect, select option d as the answer.)

Correct Answer: b

Detailed Solution:

The **HALTED** signal in Verilog processors is typically used to indicate that the processor should stop further execution, and no subsequent instructions should alter the state of the processor after the **HLT** instruction. The correct answer is (b).

QUESTION 8:

Which of the following statement(s) is/are true about the usage of the variable TAKEN-BRANCH in the Verilog implementation of the processor as discussed in the lecture?

a. To stop all the instructions following the branch instruction from entering the pipeline.
b. To prevent instructions inside pipeline from making any changes after the branch decision is made.
c. To indicate that the processor has successfully jumped to the location specified in the branch instruction.
d. None of these.

HINT: (If options a, b and c are all incorrect, select option d as the answer.)

Correct Answer: b

Detailed Solution:

Before the branch decision is made, the processor has not yet determined which path to follow. Instructions fetched before this decision may or may not be the correct ones to execute. The TAKEN-BRANCH signal ensures that these instructions do not change the processor state until the branch outcome is known, maintaining correct program execution.
The correct option is (b).

QUESTION 9:

Given the following Verilog code segment:

```
reg clk1, clk2;
initial begin
    clk1 =0; clk2 = 0;
    forever begin
         #20 clk1 = 1; #5 clk1 =0;
         #15 clk2 = 1; #5 clk2 = 0;
    end
end
```

What is the duty cycle of the clocks (clk1, clk2)? The duty cycle of a clock is defined as the fraction of the time period the clock is in an active state.

a. (0.50, 0.50)
b. (0.25, 0.25)
c. (0.20, 0.25)
d. (0.11, 0.11)

Correct Answer: d

Detailed Solution:

For clk1, HIGH duration = 5 time units, LOW duration = 45 time units.
Thus, duty cycle of clk1 is = **5**/45 =**0**.11

For clk2, HIGH duration = 5 time units, LOW duration = 45 time units.
Thus, duty cycle of clk1 is = **5**/45 =**0**.11

The correct answer is (d).

QUESTION 10:

Consider the following MIPS 32 code segment:

```
        ADDI   R1,R0,5
        ADDI   R2,R0,3
        ADDI   R3,R0,4
Loop:   MUL    R3,R3,R1
        SUBI   R2,R2,1
        SLTI   R4,R2,2
        BNEQZ  R4,Loop
```

After executing the above code the value at register R3 will be _____ (in decimal).

Correct Answer: 100

Detailed Solution:

Iteration	R1	R2	R3	R3 = R3x R1	R2 = R2 - 1	R4 = (R2<2)? 1: 0	Loop?
0	5	3	4	-	-	-	-
1	5	3	4	20	2	0	Yes
2	5	2	20	100	1	1	No

Final value of R3 is 100.

*********END*******