Siddhartha R. Nair

+1 415 933 1361 |srnair@ucsd.edu | LinkedIn: Siddhartha Nair

EXPERIENCE

Intel Corporation — *SoC Logic Design Engineer Intern* **June 2023 – December 2023**

- Developed a multi-script consolidation program using **Python, Bash, Perl** to streamline the validation testing of the project SOC, reducing setup time over 90%
- Ran customizable regressions on several chip designs and models, and then populate and share data through outlook in html, text, and xlsx using **Python**
- Utilized **Microsoft Azure** to automate 100+ regressions into Power Bi reports, cutting down the generation time from hours to near seconds
- Formatted these reports into the network sharepoint, allowing data-driven decision-making from management
- Developed 4+ **SystemVerilog** projects, each with tailored modules and testbenches, simulated them through VCS, conducted waveform analysis through Verdi
- Configured 200+ IP repositories to their appropriate format by analyzing the structure of RTL files and simulating through VCS

Loadstar Sensors — *Software Engineer, Hardware Technician Intern* **June 2022 – September 2022**

- Developed **Python** cross-platform programs using serial communication to display and analyze multi-channel data from 20+ inputs
- Compatible with all Loadstar products, including both capacitive and resistive variations devices of different units (force/pressure/temperature/displacement/voltage)
- Capable of reading and plotting continuous data of up to 1k Hz, displaying results in fully customizable layout
- Facilitated the CEO and Head of Marketing in executing their responsibilities
- Corrected 3 bugs in current company developed software programs, enhancing stability for end users
- Organized, assembled, and calibrated orders with state-of-the-art Instron machines for shipment
- Awarded as the most valuable intern directly from the CEO

Loadstar Sensors — *Technical Associate* **November 2019 – September 2021**

- Assembled and flashed 100+ Raspberry Pi touch display computers with custom operating system configurations, including company logo boot-up and program integration
- Expedited the generation of invoices and order preparation for streamlined shipping processes
- Diagnosed and resolved hardware and software malfunctions in 5+ laptop and desktop computers

EDUCATION

University of California San Diego — *B.S. Computer Engineering* **September 2021 – June 2025**

Relevant Coursework: OOP (CSE11), Data Structures/Algorithms (CSE12, CSE 21, 101) , Discrete Math (CSE 20), Linear Algebra (MATH 18), Mechanics/Electromagnetism/Thermodynamics (PHYS 2A, 2B, 2C), Analog Design/Systems (ECE 35, 45, 101), Systems Programming/Assembly (CSE 30), Digital Design (CSE 140, 140L)

PROJECTS

CSE 140L - Digital Design Laboratory (SystemVerilog) **Winter 2024**

Robertson Multiplier: 4-bit binary multiplier using shift-and-add algorithm. Modules for full adders, shift registers, control logic.

Alarm Clock: Digital alarm clock with settable date, time, alarm using finite state machines. Modules for clock generation, time increment, time setting, alarm comparison, display control.

Traffic Light Controller: Traffic light control system for 4-way intersection with protected left turns, adaptive timing. Modules for state control, traffic detection, light output encoding.

LFSR Encryptor/Decryptor: Message encryption using linear feedback shift register. Modules for state machine controller, dual-port data memory, data path encryption.

For each project, developed comprehensive testbenches and utilized ModelSim software for simulation and waveform analysis. Performed synthesis and compilation using Intel Quartus Prime to analyze RTL diagrams.

TECHNICAL SKILLS

Software Tools: ModelSim, Intel Quartus, VCS, Verdi, Github, Git, Visual Studio Code

Languages: Python, Java, C, C++, Verilog/SystemVerilog, MATLAB, Assembly

Tools: Microsoft Azure, Power BI, Sharepoint, Excel, WSL, Unix

Algorithms/Data Structures: Graphs, Trees, Arrays, Stacks, Queues, Hashing, Sorting, Dynamic Programming, Recursion