Siddhartha R. Nair

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EXPERIENCE

Intel Corporation — *SoC Logic Design Engineer Intern* **June 2023 – December 2023**

- Developed a multi-script consolidation program using **Python, Bash, Perl** to streamline the validation testing of the project SOC, reducing setup time over 90%
- Ran customizable regressions on several chip designs and models, and then populate and share data through outlook in html, text, and xlsx using **Python**
- Utilized **Microsoft Azure** to automate 100+ regressions into Power BI reports, immensely cutting generation time
- Formatted these reports into the network SharePoint, allowing data-driven decision-making from management
- Developed 4+ **SystemVerilog** projects, simulated through VCS, visualized through Verdi
- Configured 200+ IP repositories by analyzing the structure of RTL files and simulating through VCS

Loadstar Sensors — *Software Engineer, Hardware Technician Intern* **June 2022 – September 2022**

- Developed **Python** cross-platform programs using serial communication to display and analyze multi-channel data from 20+ inputs, compatible with capacitive and resistive devices of different units
- Capable of reading and plotting continuous data of up to 1k Hz, displaying results in fully customizable layout
- Corrected 3 bugs in company developed software programs
- Facilitated the CEO and Head of Marketing in executing their responsibilities
- Assembled, and calibrated orders with state-of-the-art Instron machine
- Awarded as the most valuable intern directly from the CEO

Loadstar Sensors — *Technical Associate* **November 2019 – September 2021**

- Assembled and flashed 100+ Raspberry Pi touch display computers with custom operating system configurations
- Expedited the generation of invoices and order preparation for streamlined shipping processes

EDUCATION

University of California San Diego — *B.S. Computer Engineering* (Expected) **Spring 2025**

Relevant Coursework:

CSE 140 - Components and Design Techniques for Digital Systems **Winter 2024**

Digital logic design, Boolean logic, finite state machines, combinational and sequential logic, timing and canonical analysis

CSE 140L - Digital Design Laboratory (SystemVerilog, ModelSim, Quartus Prime) **Winter 2024**

Combinational logic, CAD FSM synthesis. Projects: Robertson Multiplier, digital alarm clock, traffic light controller, LFSR encryptor/decryptor

ECE 111 - Advanced Digital Design Project (SystemVerilog, ModelSim, Quartus Prime) **Spring 2024**

Advanced digital systems, hazard elimination, CAD sync/async FSM synthesis, synchronization, pipelining, resource and timing analysis. Projects: barrel shifter, booth multiplier, sync/async FIFO, **SHA-256** based Bitcoin mining model

PROJECTS

FPGA Digital Design Projects* (SystemVerilog, ModelSim, Vivado) **Spring 2024**

Implemented basic digital circuits (Full Adder, MUX, Counter) on FPGA and utilized switches, buttons, and LEDs for interaction

FPGA-Based RISC-V Processor Implementation* (SystemVerilog, Vivado) **Spring 2024**

-RISC-V processor RTL model with modular design of components (Control Unit, ALU, Memory, Register, Program Counter)
-LED indicators for real-time interaction and on-board reset functionality
-Supports all modern RISC-V register, immediate, load, and store instructions

*Functionality verified using testbenches. Debounce signal processing and clock synchronization required. Designed, simulated, synthesized, and implemented using AMD Vivado. Bitstreams programmed onto Digilent Basys 3 FPGA Board

NavigateUCSD (Javascript, React) **Spring 2024**

Designed front/backend application utilizing Microsoft Azure Map API to animate user-defined, point-to-point paths across a college campus based on an interactive schedule input

TECHNICAL SKILLS

Languages: SystemVerilog, Verilog, C++, C, Assembly, Python, Java, JavaScript, React, MATLAB
Software Tools: ModelSim, Intel Quartus, Vivado, VCS, Verdi, Github, Git, Visual Studio Code
Cloud/Data Tools: Microsoft Azure, Power BI, Sharepoint, Excel, WSL, Unix, Vercel
Data Structures: Graphs, Trees, Arrays, Linked Lists, Stacks, Queues, Heaps, Hash Tables, Tries, Disjoint Sets
Algorithms: Sorting, Dynamic Programming, Recursion, Graph Algorithms, Backtracking, Greedy, Divide and Conquer