INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

EE-Midsem

Monday Apr. 24, 2023	**MS-101 Makerspace**	Marks: 40
Time: 15:15-16:00	Spring Semester 2022-23	(To be re-scaled)

Roll Number: _____ **Name:** _____

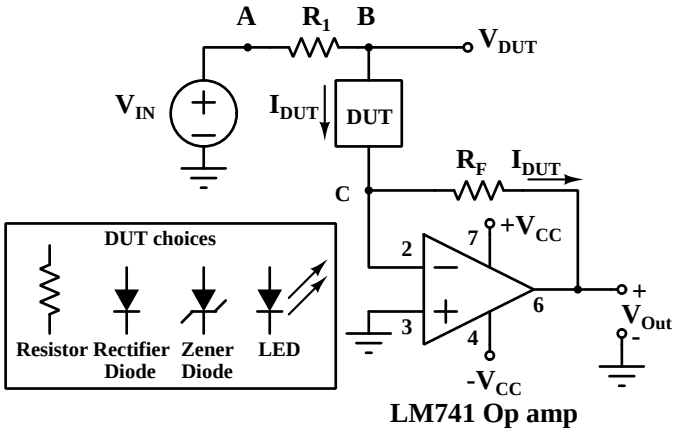
Division: _____ **Batch:** _____ **Signature:** _____

Answer the following in the space provided with the questions.

Q–1 Circuit diagram of the op amp I to V converter used in Expt. 3 is shown below.

The device under test (DUT) is connected between terminals B and C.
Assume that the op amp is ideal.
$+V_{cc} = +12$ V, $-V_{cc} = -12$ V; $R_1 = 1$ kΩ, $R_F = 2$ kΩ.

Also assume that the maximum and minimum V_{Out} levels are $+V_{cc}$ and $-V_{cc}$ respectively.
Calculation steps must be shown with your answer.
No marks will be awarded without proper steps.



a) A 1 kΩ resistor is connected as the DUT.

If $V_{IN} = +4$ V, what will be the values of V_{DUT} and V_{Out}? Answer:	**Steps:** $R_1 = R = 1$ kΩ (connected between 4 V and virtual ground). So $V_{DUT} = 2$ V. (Pot. division bet. R_1 and R. $I_{DUT} = V_{DUT}/R = 2$ V/1000Ω = 2 mA. $V_{out} = -2$ mA$*R_F = -2$ mA * 2 k = -4 V $V_{DUT} = \underline{2.0}$ V, $V_{Out} = \underline{-4.0}$ V 0.5 mark penalty for wrong sign

– **[2]**

b) a Zener diode is connected as the DUT with its anode at terminal B and cathode at terminal C. The Zener voltage is 3.2 V, and the Zener I-V characteristic is linear in the Zener region with a slope of 200 Ω.

If V_{IN} = -8 V, what will be the values of V_{DUT} and I_{DUT}? Answer:	**Steps:** For applied voltage > Zerner voltage, $I_{DUT} = -(8-3.2)/(1000+200) = -4.8/1200 = -4.0$ mA. $V_{DUT} = -(200 * \lvert I_{DUT} \rvert + 3.2) = -(0.8+3.2) = -4.0$ V. $\boxed{V_{DUT} = \underline{\text{-4.0V}}}$, $\boxed{I_{DUT} = \underline{\text{-4.0mA}}}$ 0.5 mark penalty for wrong sign

– [**2**]

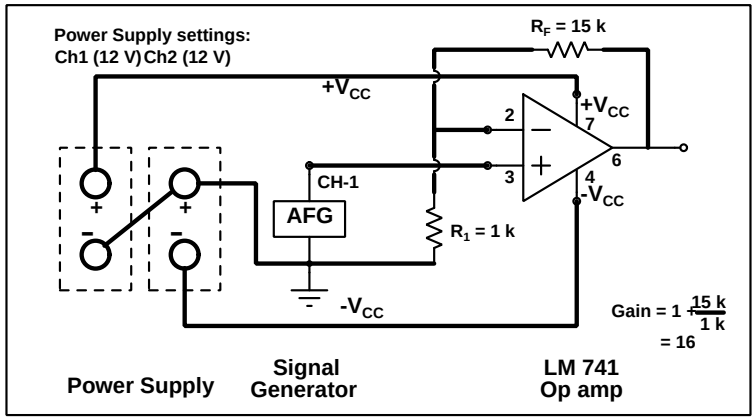
c) an LED is connected as the DUT with its anode at terminal B and cathode at terminal C. The LED cut-in voltage is 2.5 V (below this voltage the LED draws negligible current).

If V_{IN} = +2 V, what will be the values of V_{DUT} and V_{Out}? Answer:	**Steps:** No current through the LED since the voltage is less than cut in voltage. So Op amp output is 0 V, and there is no drop across the current limiter resistor R_1. 0.5 mark penalty for wrong sign $\boxed{V_{DUT} = \underline{2.0\text{ V}}}$, $\boxed{V_{Out} = \underline{0.0\text{ V}}}$

– [**2**]

– [**Q1: 2+2+2=6 marks**]

Q–2 Three blocks with their terminals, *viz.* Power supply, AFG and LM 741 op amp are shown below.



Show the wiring between these three blocks so as to obtain a **non-inverting** amplifier with a voltage gain of **16**. (Add the connections to the diagram above).
Connect also the required resistors out of the following resistor values:
1 kΩ, 10 kΩ, 15 kΩ, 16 kΩ, 17 kΩ, 160 kΩ and 170 kΩ.
Assume that both Ch1 and Ch2 of Power supply are set at 12 V. You must use the Power supply Ch1 as $+V_{CC}$ and Ch2 as $-V_{CC}$. – [**Q2: 5 marks**]

Marking Key for Q2:

Ch1 +	to Opamp $+V_{CC}$	0.5
Ch1 -	to Ch2 + and Ground	0.5+0.5 = 1.0
Ch2 -	to Opamp $-V_{CC}$	0.5
AFG top	to Opamp non-inv (3)	0.5
Opamp out(6)	to Inv input (2) through R_F	0.5
Opamp Inv (2)	to Ground through R_1	0.5
Opamp config	for non inverting amp	0.5
Choics of R	R_F and R_1 values	1.0

Q–3 A digital circuit receives a natural number in the range $0 \leq n \leq 15$ represented by 4 bits ABCD (with A as the most significant bit). We want to design the logic for outputting a 'Select' signal when n is any one of 0, 1, 2, 8, 9 or 10.

a)

Fill entries in the truth table shown on the right for 'Select' as a function of A, B, C and D. **Be very careful with these entries. Errors in this part will lead to wrong results in the remaining parts!**

Answer:

A	B	C	D	Select
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

0.5 mark penalty for every wrong entry

– [**2**]

b)

Express 'select' in canonical form as a sum of products.

Answer:

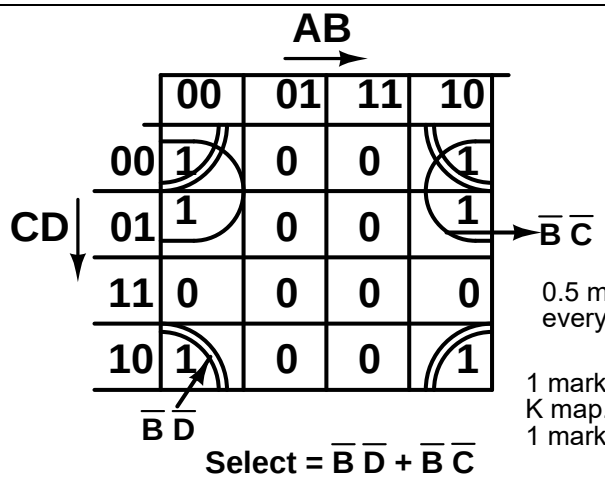
$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D}$

0.5 mark penalty for every wrong entry

– [**2**]

c)

Fill entries in the Karnaugh map shown on the right for 'Select' as a function of A, B, C and D.



0.5 mark penalty for every wrong entry

1 mark for correct K map.
1 mark for correct circlings

Show the maximal groupings of '1's in the Karnaugh map above and derive the **minimal** logic expression for **'select** in terms of A,B,C,D and their complements.

Select $= \overline{B} \cdot (\overline{C} + \overline{D})$

2 marks for the correct minimized expression.

(if only one term is correct, then 1 mark)

– [4]

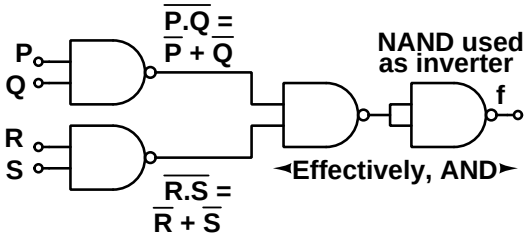
– Q3: 2+2+4 = 8 marks

Q–4

We need to generate the function:
$f = (\overline{P} + \overline{Q}) \cdot (\overline{R} + \overline{S})$ from input signals P, Q, R and S. (Their complements are not provided as inputs).

IC 7400 provides 4 2-input NAND gates in a single package. Implement the function f using a single 7400 package (*i.e.* Using 4 or fewer 2-input NAND gates).

Logic Diagram:

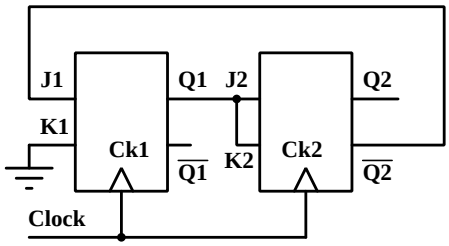


Partial marks only if the first two gates (P, Q, R, S) are correctly connected.
Correct P, Q, R, S connection: 2 marks
Correct connections of the third NAND gate: 2 marks

– Q4: 5 marks

Q–5

Consider the circuit on the right using two positive edge triggered JK flipflops. You are given that at t=0, Q1 = Q2 = 0.



Four positive clock edges arrive after this initial state. What will be values of Q1 and Q2 after the arrival of each of the clock edges?

	Q1	Q2
At t=0	0	0
After Clock1	1	0
After Clock2	1	1
After Clock3	1	0
After Clock4	1	1

No marks if 'After Clock 1' Q1 and Q2 are wrong.

1 mark penalty for every wrong entry from Clock2 onwards

– **Q5: 4 marks**

Q–6 **a)** What is the least number of bits required to represent:

i) 128 (decimal) in unsigned binary format, Answer: 8

ii) +128 (decimal) in two's complement signed format, Answer: 9

iii) -128 (decimal) in two's complement signed format, Answer: 8

iv) +15 (decimal) in two's complement signed format. Answer: 5

– **[2]**

b) i) Represent the unsigned number 1123 (decimal) in base 16 format (Hex code) as a 12 bit wide quantity. Answer: 463 in Hex

ii) Represent the same number (1123 decimal) in base 8 format (octal) as a 12 bit wide quantity. Answer: 2143 in octal

– **[2]**

c) What decimal signed number is represented by the 12 bit Hex number D28 if we are using 2's complement convention for signed numbers?

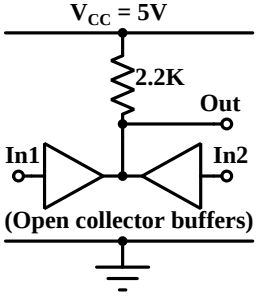
Answer: -728

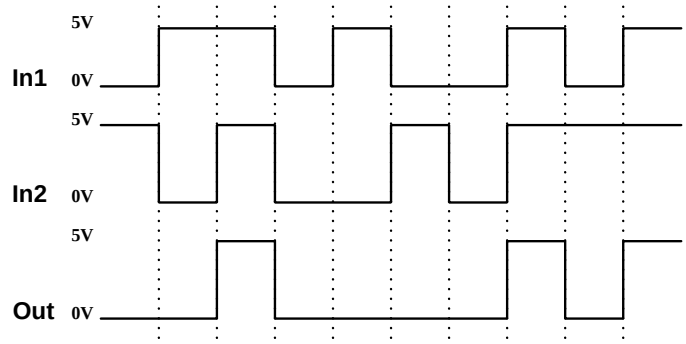
– **[1]**

– **[Q6: 2 + 2 + 1 = 5 marks]**

Q–7

Outputs of two **open collector** buffer gates are shorted as shown in the logic diagram on the right. Waveforms for the inputs applied to the two gates are shown below.

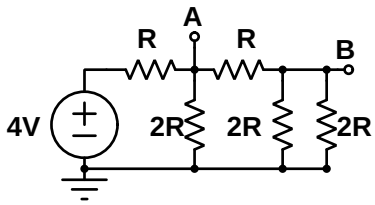




2 marks penalty for every wrong pulse.

Add the waveform at the terminal marked Out to the figure with the same time scale as In1 and In2. – [**Q7: 5marks**]

Q–8



Find the voltage at nodes A and B in the circuit shown on the left. The voltage source provides 4V.

Voltage at node A is: $\boxed{2\ \text{V}}$

Voltage at node B is: $\boxed{1\ \text{V}}$

– [**Q8: 2 marks**]

Paper Ends

Rough Work