BK4829 Registers Table

DRT01-230606-C01 V1.0

2023/6/5

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1. Registers' Definition

Register	Default	Description
REG_00<15>	*0*	*Soft Reset.* *1=Reset; 0=Normal.*
REG_02<15>	*Read Only*	*FSK Tx Finished Interrupt.*
REG_02<14>	*Read Only*	*FSK FIFO Almost Empty Interrupt Enable.*
REG_02<13>	*Read Only*	*FSK Rx Finished Interrupt Enable.*
REG_02<12>	*Read Only*	*FSK FIFO Almost Full Interrupt.*
REG_02<11>	*Read Only*	*DTMF/5TONE Found Interrupt.*
REG_02<10>	*Read Only*	*CTCSS/CDCSS Tail Found Interrupt.*
REG_02<9>	*Read Only*	*CDCSS Found Interrupt.*
REG_02<8>	*Read Only*	*CDCSS Lost Interrupt.*
REG_02<7>	*Read Only*	*CTCSS Found Interrupt.*
REG_02<6>	*Read Only*	*CTCSS Lost Interrupt.*
REG_02<5>	*Read Only*	*VoX Found Interrupt.*
REG_02<4>	*Read Only*	*VoX Lost Interrupt.*

REG_02<3>	*Read Only*	*Squelch Found Interrupt.*
REG_02<2>	*Read Only*	*Squelch Lost Interrupt.*
REG_02<1>	*Read Only*	*FSK Rx Sync Interrupt.*
REG_07<15:0>		*When <15:13>=0 for CTC1* *<12:0>=CTC1 frequency control word* *= freq(Hz)* 20.64888 for XTAL 13M/26M or* *=freq(Hz)*20.97152 for XTAL* *12.8M/19.2M/25.6M/38.4M* *When<15:13>=1 for CTC2(Tail 55Hz Rx detection)* *<12:0>=CTC2 (should below 100Hz)frequency* *control word* *= 25391/freq(Hz) for XTAL 13M/26M or* *= 25000/freq(Hz) for XTAL* *12.8M/19.2M/25.6M/38.4M* *When <15:13>=2 for CDCSS 134.4Hz*

		<12:0>=CDCSS baud rate frequency (134.4Hz) control word *= freq(Hz)* 20.64888 for XTAL 13M/26M or* *=freq(Hz)*20.97152 for XTAL 12.8M/19.2M/25.6M/38.4M* *When<15:13>=3 for CTC3(Tail 62Hz Rx detection)* *<12:0>=CTC3 (should below 100Hz)frequency control word* *= 25391/freq(Hz) for XTAL 13M/26M or* *= 25000/freq(Hz) for XTAL 12.8M/19.2M/25.6M/38.4M*
REG_08<15:0>		*<15>=1 for CDCSS high 12bit* *<15>=0 for CDCSS low 12bit* *<11:0>=CDCSS high/low 12bit code*
REG_09<15:0>		*DTMF/SelCall Symbol Coefficient for Detection.*

		<15:12>=Symbol Number *<7:0>=Coefficient.*
REG_0A<6>	*Read Only*	*GPIO6 (PIN28) Input Indicator.* *1=High; 0=Low.*
REG_0A<5>	*Read Only*	*GPIO5 (PIN29) Input Indicator.* *1=High; 0=Low.*
REG_0A<4>	*Read Only*	*GPIO4 (PIN30) Input Indicator.* *1=High; 0=Low.*
REG_0A<3>	*Read Only*	*GPIO3 (PIN31) Input Indicator.* *1=High; 0=Low.*
REG_0A<2>	*Read Only*	*GPIO2 (PIN32) Input Indicator.* *1=High; 0=Low.*
REG_0A<1>	*Read Only*	*GPIO1 (PIN1) Input Indicator.* *1=High; 0=Low.*
REG_0A<0>	*Read Only*	*GPIO0 (PIN2) Input Indicator.* *1=High; 0=Low.*
REG_0B<11:8>	*Read Only*	*DTMF/5Tone Code Received.*

REG_0B<7>	*Read Only*	*FSK Rx Sync Negative has been Found.*
REG_0B<6>	*Read Only*	*FSK Rx Sync Positive has been Found.*
REG_0B<4>	*Read Only*	*FSK Rx CRC Indicator.* *1=CRC Pass; 0=CRC Fail.*
REG_0C<15:14>	*Read Only*	*<14>:CDCSS positive code received* *<15>:CDCSS negative code received*
REG_0C<13:12>	*Read Only*	*CTCSS Phase Shift Received.* *00=No phase shift* *01=CTCSS0 120°phase shift,* *10= CTCSS0 180°phase shift* *11= CTCSS0 240°phase shift*
REG_0C<10:11>	*Read Only*	*<11>:CTC2(55Hz) received* *<10>:CTC1 received*
REG_0C<4>	*Read Only*	*<4>:CTC3(62Hz) received*

REG_0C<2>	*Read Only*	*VoX Indicator* *0: No* *1: Yes*
REG_0C<1>	*Read Only*	*Squelch result output.* *1=Link; 0=Loss*
REG_0C<0>	*Read Only*	*Interrupt Indicator.* *1=Interrupt Request; 0=No Request.*
REG_0D<15>	*Read Only*	*Frequency Scan Indicator.* *1=Busy; 0=Finished.*
REG_0D<10:0>	*Read Only*	*Frequency Scan High 16 bits.*
REG_0E<15:0>	*Read Only*	*Frequency Scan Low 16 bits.* *= REG_0D<10:0><<16 + REG_0E<15:0>, unit is 10Hz*
REG_10<15:0>	*0x0038*	*Rx AGC Gain Table[0]. (Index Max->Min is 3,2,1,0,-1)* *<9:8>=LNA Gain Short* *11=0dB; 10=-11dB; 01=-16dB; 00=-19dB.*

		<7:5>=LNA Gain *111=0dB; 110=-2dB; 101=-4dB; 100=-6dB;* *011=-9dB; 010=-14dB; 001=-19dB; 000=-24dB.* *<4:3>=MIXER Gain* *11=0dB; 10=-3dB; 01=-6dB; 00=-8dB.* *<2:0>=PGA Gain* *111=0dB; 110=-3dB; 101=-6dB; 100=-9dB;* *011=-15dB; 010=-21dB; 001=-27dB; 000=-33dB.*
REG_11<15:0>	*0x025a*	*Rx AGC Gain Table[1]. (Index Max->Min is 3,2,1,0,-1)* *Same as REG_10.*
REG_12<15:0>	*0x037b*	*Rx AGC Gain Table[2]. (Index Max->Min is 3,2,1,0,-1)* *Same as REG_10.*
REG_13<15:0>	*0x03de*	*Rx AGC Gain Table[3]. (Index Max->Min is 3,2,1,0,-1)* *Same as REG_10.*
REG_14<15:0>	*0x0000*	*Rx AGC Gain Table[-1]. (Index Max->Min is 3,2,1,0,-1)* *Same as REG_10.*

REG_19<15>	*1*	*Automatic MIC PGA Gain Controller (MIC AGC)* *Disable.* *1=Disable; 0=Enable.*
REG_1A<15:12>	*0b0101*	*Crystal vReg Bit.*
REG_1A<11:8>	*0b1000*	*Crystal iBit.*
REG_1F<3:0>	*0b1000*	*PLL CP bit.*
REG_24<5>	*0*	*DTMF/SelCall Enable.* *1=Enable; 0=Disable.*
REG_24<4>	*1*	*DTMF or SelCall Detection Mode.* *1=for DTMF; 0=for SelCall.*
REG_24<3:0>	*0xe*	*Max Symbol Number for SelCall Detection.*
REG_28<11:9>	*0b101*	*Rx DCC Filter(HPF1)* *000=Bypass DC filter;*
REG_28<8>	*0*	*Rx AF Noise Gate Enable.*
REG_28<7:0>	*0*	*Rx AF Noise Gate Level*
REG_29<11:9>	*0b011*	*Tx DCC Filter(HPF1)* *000=Bypass DC filter;*

REG_2A<13:8>	*0b010000*	*Noise Gate Time Constant.* *<5:3>for Release Time* *<2:0>for Attack Time.* *000=0 ms* *001=6 ms* *010=12 ms* *011=24 ms* *100=48 ms* *101=96 ms* *110=192 ms* *111=384 ms*
REG_2B<10>	*0*	*Disable AF Rx HPF300 filter.* *0=Enable; 1=Disable*
REG_2B<9>	*0*	*Disable AF Rx LPF3K filter.* *0=Enable; 1=Disable*
REG_2B<8>	*0*	*Disable AF Rx de-emphasis filter.* *0=Enable; 1=Disable*

REG_2B<2>	*0*	*Disable AF Tx HPF300 filter.* *0=Enable; 1=Disable*
REG_2B<1>	*0*	*Disable AF Tx LPF1 filter.* *0=Enable; 1=Disable*
REG_2B<0>	*0*	*Disable AF Tx pre-emphasis filter.* *0=Enable; 1=Disable*
REG_2C<14:12>	*0b011*	*AF Amplitude Detection Frame Length,(after Pre/De-emphasis)* *000=0 ms* *001=4 ms* *010= 8ms* *011=16 ms* *…* *111=28 ms*
REG_2C<11:6>	*0b010001*	*Pre/De-emphasis DRC Time Constant.* *<5:3>for Release Time.* *<2:0>for Attack Time.*

		000=0 ms *001=6 ms* *010=12ms* *011=24 ms* *100=48 ms* *101=96 ms* *110=192 ms* *111=384 ms*
REG_2C<5:0>	*34*	*Pre-emhpasis Gain(dB)* *24=0dB* *25=1dB* *34=10dB*
REG_2E<9:8>	*0x10*	*CTCSS/CDCSS Tx Gain2 Tuning (after Gain1).* *00=12dB; 01=6dB; 10=0dB; 11=-6dB*
REG_2F<13:8>	*24*	*De-emhpasis Gain(dB)* *24=0dB* *25=1dB*

		34=10dB
REG_2F<7:5>	*0b110*	*Tx Soft Limiter Factor* *000=bypass* *…* *111=hard limit*
REG_2F<4:0>	*24*	*Tx Soft Limiter Threshold* *0=0.5* *..* *31=0.99*
REG_30<15>	*0*	*VCO Calibration Enable.* *1=Enable, 0=Disable*
REG_30<13:10>	*0*	*Rx Link Enable (include LNA/MIXER/PGA/ADC).* *1111=Enable, 0000=Disable*
REG_30<9>	*0*	*AF DAC Enable.* *1=Enable, 0=Disable.*
REG_30<7:4>	*0*	*PLL/VCO Enable.* *1111=Enable, 0000=Disable*

REG_30<3>	*0*	*PA Gain Enable.* *1=Enable, 0=Disable*
REG_30<2>	*0*	*MIC ADC Enable.* *1=Enable, 0=Disable*
REG_30<1>	*0*	*Tx DSP Enable.* *1=Enable, 0=Disable*
REG_30<0>	*0*	*Rx DSP Enable.* *1=Enable, 0=Disable*
REG_31<3>	*0*	*Enable Compander Function.* *1= Enable; 0=Disable*
REG_31<2>	*0*	*Enable VOX detection.* *1=Enable; 0=Disable*
REG_31<1>	*0*	*Enable Scramble Function.* *1=Enable; 0=Disable*
REG_32<15:14>	*0b00*	*Frequency Scan Time.* *00=0.2 Sec; 01=0.4 Sec; 10=0.8 Sec; 11=1.6 Sec*
REG_32<0>	*0*	*Frequency Scan Enable.*

		1=Enable; 0=Disable.
REG_33<14>	*1*	*GPIO6 (PIN28) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<13>	*1*	*GPIO5 (PIN29) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<12>	*1*	*GPIO4 (PIN30) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<11>	*1*	*GPIO3 (PIN31) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<10>	*1*	*GPIO2 (PIN32) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<9>	*1*	*GPIO1 (PIN1) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<8>	*1*	*GPIO0 (PIN2) Output Disable.* *1=Output Disable; 0=Output Enable.*
REG_33<6>	*0*	*GPIO6 (PIN28) Output Value.*

		1= High when Output Enable; 0=Low when Output Enable.
REG_33<5>	*0*	*GPIO5 (PIN29) Output Value.* *1= High when Output Enable; 0=Low when Output Enable.*
REG_33<4>	*0*	*GPIO4 (PIN30) Output Value.* *1= High when Output Enable; 0=Low when Output Enable.*
REG_33<3>	*0*	*GPIO3 (PIN31) Output Value.* *1= High when Output Enable; 0=Low when Output Enable.*
REG_33<2>	*0*	*GPIO2(PIN32) Output Value.* *1= High when Output Enable; 0=Low when Output Enable.*
REG_33<1>	*0*	*GPIO1 (PIN1) Output Value.* *1= High when Output Enable; 0=Low when Output Enable.*
REG_33<0>	*0*	*GPIO0 (PIN2) Output Value.*

		1= High when Output Enable; 0=Low when Output Enable.
REG_34<15:12>	*0x0*	*GPIO3 (PIN31) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_34<11:8>	*0x0*	*GPIO2 (PIN32) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_34<7:4>	*0x0*	*GPIO1 (PIN1) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_34<3:0>	*0x0*	*GPIO0 (PIN2) Output Type Selection.* *0=High/Low* *1=Interrupt* *2=Squelch* *3=VoX* *4=CTCSS/CDCSS Compared Result* *5=CTCSS Compared Result* *6=CDCSS Compared Result* *7=Tail Detected Result*

		8=DTMF/5Tone Symbol Received Flag *9=CTCSS/CDCSS Digital Wave* *Others=Reserved*
REG_35<11:8>	*0x0*	*GPIO6 (PIN28) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_35<7:4>	*0x0*	*GPIO5 (PIN29) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_35<3:0>	*0x0*	*GPIO4 (PIN30) Output Type Selection.* *The Definitions is the same as REG_34<3:0>.*
REG_36<15:8>	*0*	*PA Bias output 0~3.2V* *0x00=0V* *…* *0xFF=3.2V*
REG_36<7>	*0*	*1=Enable PACTL output; 0=Disable(Output 0 V)*
REG_36<5:3>	*0b111*	*PA Gain1 Tuning.* *111(max)->000(min)*
REG_36<2:0>	*0b111*	*PA Gain2 Tuning.*

		111(max)->000(min)
REG_37<15>	*0*	*DSP Enable.*
REG_37<14:12>	*0b001*	*DSP Voltage Setting.*
REG_37<11>	*1*	*ANA LDO Selection.* *1=2.7v, 0=2.4v*
REG_37<10>	*1*	*VCO LDO Selection.* *1=2.7v, 0=2.4v*
REG_37<9>	*1*	*RF LDO Selection.* *1=2.7v, 0=2.4v*
REG_37<8>	*1*	*dac_drv2_en*
REG_37<7>	*0*	*ANA LDO Bypass.* *1=Bypass, 0=Enable.*
REG_37<6>	*0*	*VCO LDO Bypass.* *1=Bypass, 0=Enable.*
REG_37<5>	*0*	*RF LDO Bypass.* *1=Bypass, 0=Enable.*
REG_37<4>	*0*	*ANA LDO ENABLE*

REG_37<3>	*0*	*RF LDO ENABLE*
REG_37<2>	*0*	*1=Enable, 0=Disable.* *VCO LDO ENABLE*
REG_37<1>	*0*	*XTAL Enable.* *1=Enable, 0=Disable.*
REG_37<0>	*0*	*Band-Gap Enable.* *1=Enable, 0=Disable.*
REG_38<15:0>	*0x3A98*	*Frequency(Hz)= (freq_hi16<<16 + freq_lo16)*10*
REG_39<15:0>	*0x0271*	
REG_3B<15:0>	*0x5880*	*Crystal Frequency Low-16bits. LSB->5Hz*
REG_3C<15:8>	*0x4f*	*Crystal Frequency High-8bits.*
REG_3C<7:6>	*0b10*	*Crystal Frequency Mode Selection.* *00~=13MHz; 01~=19.2MHz; 10~=26MHz;* *11~=38.4MHz*
REG_3E<15:0>	*36458*	*Band Selection Threshold.* *~=VCO Max Frequency(Hz)/96/640*
REG_3F<15>	*0*	*FSK Tx Finished Interrupt Enable.*

		1=Enable; 0=Disable.
REG_3F<14>	*0*	*FSK FIFO Almost Empty Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<13>	*0*	*FSK Rx Finished Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<12>	*0*	*FSK FIFO Almost Full Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<11>	*0*	*DTMF/5TONE Found Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<10>	*0*	*CTCSS/CDCSS Tail Found Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<9>	*0*	*CDCSS Found Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<8>	*0*	*CDCSS Lost Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<7>	*0*	*CTCSS Found Interrupt Enable.* *1=Enable; 0=Disable.*

REG_3F<6>	*0*	*CTCSS Lost Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<5>	*0*	*VoX Found Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<4>	*0*	*VoX Lost Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<3>	*0*	*Squelch Found Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<2>	*0*	*Squelch Lost Interrupt Enable.* *1=Enable; 0=Disable.*
REG_3F<1>	*0*	*FSK Rx Sync Interrupt Enable.* *1=Enable; 0=Disable.*
REG_40<12>	*1*	*Enable RF Tx Deviation.* *1=Enable; 0=Disable*
REG_40<11:0>	*0x4D0*	*RF Tx Deviation Tuning (Apply for both in-band signal and sub-audio signal).* *0=min; 0xFFF=max*

REG_43<14:12>	*0b100*	*RF filter bandwidth (Apass=0.1dB)* *000 = 2 kHz* *001 = 2.5 kHz* *010 = 3 kHz* *011 = 3.5 kHz* *100 = 4kHz* *101 = 4.5 kHz* *110 =5.0kHz* *111 = 5.5kHz* *if REG_43<5>=1, RF filter bandwidth *=2;*
REG_43<11:9>	*0b000*	*RF filter bandwidth when signal is weak* *(Apass=0.1dB)* *000 = 2 kHz* *001 = 2.5 kHz* *010 = 3 kHz* *011 = 3.5 kHz* *100 = 4kHz*

		101 = 4.5 kHz *110 = ~~4.25~~ 5.0kHz* *111 = ~~4.5~~5.5 kHz* *if REG_43<5>=1, RF filter bandwidth *=2;*
REG_43<8:6>	*0b001*	*AF Tx LPF2 filter Band Width (Apass=1dB) Selection.* *100 = 5.5 kHz* *101 = 5.0 kHz* *110 = 4.5 kHz* *111 = 4 kHz* *000 = 3 kHz* *001 = 2.5 kHz* *010 = 2.75 kHz* *011 = 3.5 kHz*
REG_43<5:4>	*0b00*	*BW Mode Selection.* *00=12.5k; 01=6.25k; 10=25k/20k*
REG_43<2>	*0*	*Gain after FM Demodulation.* *1=6dB; 0=0 dB.*

REG_44<15:0>	*0x9009*	*300Hz AF Response coefficient for Tx.*
REG_45<15:0>	*0x31a9*	*300Hz AF Response coefficient for Tx.*
REG_46<10:0>	*0x50*	*Voice Amplitude Threshold for VOX=1 detect*
REG_47<13>	*1*	*AF Output Inverse Mode.* *1=Inverse*
REG_47<11:8>	*0x1*	*AF Output Selection.* *0x0=Mute;* *0x1=Normal AF Out;* *0x2=Tone Out for Rx (Should enable Tone1 first);* *0x3=Beep Out for Tx (Should enable Tone1 first and* *set REG_03[9]=1 to enable AF;* *0x6=CTCSS/CDCSS Out for Rx Test;* *0x8=FSK Out for Rx Test;* *Others=Reserved;*
REG_47<0>	*0*	*AF Tx Filter Bypass All.* *1=Bypass All AF Tx filter; 0=Normal.*
REG_48<9:4>	*0x3C*	*AF Rx Gain2.*

		-28dB~3.5dB, 0.5dB/step.
REG_48<3:0>	*0b1111*	*AF DAC Gain (after Gain1 and Gain2).* *1111=max; 0000=min; about 2dB/step*
REG_49<15:14>	*0b00*	*High/Low Lo Selection.* *0X=Auto High/Low Lo; 10=Low Lo; 11=High Lo.*
REG_49<13:7>	*0x50*	*RF AGC High Threshold. LSB->1dB*
REG_49<6:0>	*0x30*	*RF AGC Low Threshold. LSB->1dB*
REG_7D<6>	*0*	*AF Level Controller(ALC) Disable.* *1=Disable; 0=Enable.*
REG_4D<7:0>	*0x20*	*Glitch threshold for Squelch =0*
REG_4E<15:12>	*0b0110*	*Squelch=1 Delay Setting.*
REG_4E<11:8>	*0b1111*	*Squelch=0 Delay Setting.*
REG_4E<7:0>	*0x08*	*Glitch threshold for Squelch =1*
REG_4F<14:8>	*0x2F*	*Ex-noise threshold for Squelch =0*
REG_4F<6:0>	*0x2E*	*Ex-noise threshold for Squelch =1*
REG_50<15>	*0*	*Enable AF Tx Mute (for DTMF Tx or other* *applications).*

		1=Mute; 0=Normal
REG_51<15>	*0*	*1=Enable Tx CTCSS/CDCSS; 0=Disable*
REG_51<14>	*0*	*1= GPIO0 (PIN2) Input for CDCSS; 0=Normal Mode.*
REG_51<13>	*0*	*1=Transmit negative CDCSS code* *0=Transmit positive CDCSS code*
REG_51<12>	*0*	*CTCSS/CDCSS mode selection.* *1=CTCSS, 0=CDCSS*
REG_51<11>	*0*	*CDCSS 24/23bit selection.* *1=24bit, 0=23bit*
REG_51<10>	*0*	*1050Hz Detection Mode.* *1=1050/4 Detect Enable, CTC1 should be set to 1050/4 Hz*
REG_51<9>	*0*	*Auto CDCSS Bw Mode.* *1=Disable; 0=Enable.*
REG_51<8>	*0*	*Auto CTCSS Bw Mode.* *0=Enable; 1=Disable*
REG_51<6:0>	*0*	*CTCSS/CDCSS Tx Gain1 Tuning.*

		0=min; 0x7F=max
REG_52<15>	*0*	*Enable 120/180/240 degree shift CTCSS or 134.4Hz Tail when CDCSS mode. When Rx, you can set this bit=1 to clear CTCSS Phase Shift Detect.* *0=Normal, 1=Enable*
REG_52<14:13>	*0b00*	*CTCSS tail mode selection (only valid when REG_52<15>=1).* *00= for 134.4Hz CTCSS Tail when CDCSS mode.* *01= CTCSS0 120°phase shift,* *10= CTCSS0 180°phase shift* *11= CTCSS0 240°phase shift*
REG_52<12>	*0*	*CTCSS Detection Threshold Mode,* *1=~0.1%; 0=0.1 Hz*
REG_52<11:6>	*0x0A*	*CTCSS found detect threshold.*
REG_52<5:0>	*0x0F*	*CTCSS lost detect threshold.*
REG_53<13:0>	*0x11*	*ALC Time Constant.* *<5:3>for Release Time* *<2:0>for Attack Time*

		000= 0 ms *001=6 ms* *010=12ms* *011=24ms* *100=48ms* *101=96ms* *110=192ms* *111=384ms*
REG_53<4:2>	*4*	*ALC Amplitude Detection Frame Length* *000=0 ms* *001=2ms* *010=4ms* *…* *100=14ms*
REG_54<15:0>	*0x9009*	*300Hz AF Response coefficient for Rx.*
REG_55<15:0>	*0x31a9*	*300Hz AF Response coefficient for Rx.*

REG_58<15:13>	*000*	*FSK Tx Mode Selection.* *000 for FSK1.2K and FSK2.4K Tx;* *001 for FFSK1200/1800 Tx;* *011 for FFSK1200/2400 Tx;* *101 for NOAA SAME Tx*
REG_58<12:10>	*000*	*FSK Rx Mode Selection.* *000 for FSK1.2K, FSK2.4K Rx and NOAA SAME Rx;* *111 for FFSK1200/1800 Rx;* *100 for FFSK1200/2400 Rx;*
REG_58<9:8>	*00*	*FSK Rx Gain.*
REG_58<5:4>	*00*	*FSK Preamble Type Selection.* *11=0xAA; 10=0x55; 00=0xAA or 0x55 due to the MSB of FSK Sync Byte 0.*
REG_58<3:1>	*000*	*FSK Rx Band Width Setting.* *100 for FSK 2.4K and FFSK1200/2400;* *000 for FSK 1.2K;* *001 for FFSK1200/1800;*

		010 for NOAA SAME Rx
REG_58<0>	*0*	*FSK Enable.* *1=Enable; 0=Disable.*
REG_59<15>	*0*	*Clear TX FIFO, 1=clear*
REG_59<14>	*0*	*Clear RX FIFO, 1=clear*
REG_59<13>	*0*	*1=Enable FSK Scramble*
REG_59<12>	*0*	*1=Enable FSK RX*
REG_59<11>	*0*	*1=Enable FSK TX*
REG_59<10>	*0*	*1=Invert FSK data when RX*
REG_59<9>	*0*	*1=Invert FSK data when TX*
REG_59<7:4>	*0*	*FSK Preamble Length Selection* *0=1 byte; 1=2 bytes; 2=3 bytes; …; 15=16 bytes.*
REG_59<3>	*0*	*FSK Sync Length Selection.* *1=4 bytes (FSK Sync Byte 0,1,2,3)* *0=2 bytes (FSK Sync Byte 0,1)*
REG_5A<15:8>	*0x85*	*FSK Sync Byte 0 (Sync Byte 0 first, then 1,2,3)*
REG_5A<7:0>	*0xCF*	*FSK Sync Byte 1*

REG_5B<15:8>	*0xAB*	*FSK Sync Byte 2*
REG_5B<7:0>	*0x45*	*FSK Sync Byte 3*
REG_5C<6>	*1*	*CRC Option Enable.* *1=Enable; 0=Disable.*
REG_5D<15:8>	*0x0F*	*FSK Data Length(Byte) Low 8bits(Total 11 bits).* *For example, 0xF means 16 bytes length.*
REG_5D<7:5>	*0*	*FSK Data Length(Byte) High 3bits(Total 11 bits).*
REG_5E<9:3>	*64*	*FSK Tx FIFO (Total 128 Words) Almost Empty Threshold.*
REG_5E<2:0>	*4*	*FSK Rx FIFO (Total 8 Words) Almost Full Threshold.*
REG_5F<15:0>	*x*	*FSK Word Input/Output.*
REG_62<14:8>	*Read Only*	*Signal Strength after RxADC. Lsb->dB*
REG_63<7:0>	*Read Only*	*Glitch Total Number within about 10ms*
REG_64<15:0>	*Read Only*	*Voice Amplitude Out.*
REG_65<6:0>	*Read Only*	*Ex-noise indicator, dB/step. >10kHz AF*
REG_66<14:8>	*Read Only*	*Upper Channel Relative Power Strength*

REG_66<6:0>	*Read Only*	*Lower Channel Relative Power Strength*
REG_67<8:0>	*Read Only*	*0.5dB/step, RSSI (dBm) ~= REG_67<8:0>/2 – 160.*
REG_68<15>	*Read Only*	*CTCSS Scan Indicator.* *1=Busy; 0=Found.*
REG_68<12:0>	*Read Only*	*CTCSS Frequency.* *Frequency(Hz)* *= REG_68<12:0>/20.64888 for 13M/26M XTAL and* *= REG_68<12:0>/ 20.97152 for* *12.8M/19.2M/25.6M/38.4M XTAL*
REG_69<15>	*Read Only*	*CDCSS Scan Indicator.* *1=Busy; 0=Found.*
REG_69<14>	*Read Only*	*23 or 24 bit CDCSS Indicator.* *1=24 bit; 0=23 bit.*
REG_69<11:0>	*Read Only*	*CDCSS High 12 bits.*
REG_6A<11:0>	*Read Only*	*CDCSS Low 12 bits.*
REG_6E<15:9>	*ReadOnly*	*AF Freq Out, Nout. Freq=Nout*25390.625/Rout*

		*Or Freq=Nout*25000/Rout for 19.2M/38.4M*
REG_6E<8:0>	*ReadOnly*	*AF Freq Out, Rout. Freq=Nout*25390.625/Rout* *Or Freq=Nout*25000/Rout for 19.2M/38.4M*
REG_6F<7:0>	*Read Only*	*AF Tx/Rx Input Amplitude(dB)*
REG_70<15>	*0*	*Enable TONE1* *1=Enable; 0=Disable.*
REG_70<14:8>	*0*	*TONE1 tuning gain*
REG_70<7>	*0*	*Enable TONE2* *1=Enable; 0=Disable.*
REG_70<6:0>	*0*	*TONE2/FSK tuning gain*
REG_71<15:0>	*0x8517*	*TONE1/Scramble frequency control word.* *=freq(Hz)* 10.32444 for XTAL 13M/26M or* *=freq(Hz)* 10.48576 for XTAL* *12.8M/19.2M/25.6M/38.4M.*
REG_72<15:0>	*0x2854*	*TONE2/FSK frequency control word* *=freq(Hz)* 10.32444 for XTAL 13M/26M or*

		=freq(Hz) 10.48576 for XTAL* *12.8M/19.2M/25.6M/38.4M.*
REG_73<13:11>	*0b000*	*Automatic Frequency Correction(AFC) Range Selection.* *000=max; 111=min*
REG_73<4>	*0*	*Automatic Frequency Correction(AFC) Disable.* *1=Disable; 0=Enable.*
REG_74<15:0>	*0xf50b*	*3000Hz AF Response coefficient for Tx.*
REG_75<15:0>	*0xf50b*	*3000Hz AF Response coefficient for Rx.*
REG_78<15:8>	*0x48*	*RSSI threshold for Squelch=1, 0.5dB/step*
REG_78<7:0>	*0x46*	*RSSI threshold for Squelch =0, 0.5dB/step*
REG_79<15:11>	*8*	*VoX Detection Interval Time.*
REG_79<10:0>	*0x40*	*Voice Amplitude Threshold for VOX=0 detect*
REG_7A<15:12>	*8*	*VoX=0 Detection delay, *128ms*
REG_7B<15:0>	*0xae34*	*RSSI Table*
REG_7C<15:0>	*0x8000*	*RSSI Table*

REG_7D<6>	*0*	*AF Level Controller(ALC) Disable.* *1=Disable; 0=Enable.*
REG_7D<5:0>	*0x1c*	*MIC Sensitivity Tuning.* *0x00=min; 0x3F=max; 0.5dB/step*
REG_7E<15>	*0*	*AGC Fix Mode.* *1=Fix; 0=Auto.*
REG_7E<14:12>	*0b011*	*AGC Fix Index.* *011=Max, then 010,001,000,111,110,101,100(min).*
REG_7E<5:3>	*0b101*	*DC Filter Band Width for Tx (MIC In).* *000=Bypass DC filter;*
REG_7E<2:0>	*0b110*	*DC Filter Band Width for Rx (IF In).* *000=Bypass DC filter;*

2. Registers' Default Value

Register	Value(HEX)	Register	Value(HEX)	Register	Value(HEX)	Register	Value(HEX)
REG_00	*48x9*	*REG_20*	*0000*	*REG_40*	*34D0*	*REG_60*	
REG_01		*REG_21*	*06D8*	*REG_41*	*81C3*	*REG_61*	
REG_02		*REG_22*	*4D08*	*REG_42*	*6b5a*	*REG_62*	
REG_03		*REG_23*	*8410*	*REG_43*	*4048*	*REG_63*	
REG_04		*REG_24*	*8C5E*	*REG_44*	*9009*	*REG_64*	
REG_05	*7819*	*REG_25*	*C1BA*	*REG_45*	*31A9*	*REG_65*	
REG_06		*REG_26*	*0000*	*REG_46*	*A050*	*REG_66*	
REG_07		*REG_27*	*0000*	*REG_47*	*6140*	*REG_67*	
REG_08		*REG_28*	*0a00*	*REG_48*	*338f*	*REG_68*	
REG_09		*REG_29*	*A600*	*REG_49*	*2830*	*REG_69*	
REG_0A		*REG_2A*	*5109*	*REG_4A*	*5448*	*REG_6A*	
REG_0B		*REG_2B*	*0000*	*REG_4B*	*710d*	*REG_6B*	
REG_0C		*REG_2C*	*3462*	*REG_4C*	*A520*	*REG_6C*	
REG_0D		*REG_2D*	*4b18*	*REG_4D*	*A020*	*REG_6D*	

REG_0E		REG_2E	9608	REG_4E	6F08	REG_6E	
REG_0F		REG_2F	98d8	REG_4F	2F2E	REG_6F	
REG_10	0038	REG_30	0000	REG_50	0000	REG_70	0000
REG_11	025A	REG_31	0000	REG_51	0000	REG_71	8517
REG_12	037B	REG_32	0244	REG_52	028F	REG_72	2854
REG_13	03DE	REG_33	FF00	REG_53	1130	REG_73	4682
REG_14	0000	REG_34	0000	REG_54	9009	REG_74	F50B
REG_15	8005	REG_35	0000	REG_55	31A9	REG_75	F50B
REG_16	8080	REG_36	003F	REG_56	1021	REG_76	E380
REG_17	7839	REG_37	1F00	REG_57	0000	REG_77	A8FF
REG_18	4525	REG_38	3A98	REG_58	0000	REG_78	4846
REG_19	9041	REG_39	0271	REG_59	0000	REG_79	4040
REG_1A	5850	REG_3A	049A	REG_5A	85CF	REG_7A	889A
REG_1B	2200	REG_3B	5880	REG_5B	AB45	REG_7B	AE34
REG_1C	0000	REG_3C	4F88	REG_5C	56F9	REG_7C	8000
REG_1D	2aab	REG_3D	0000	REG_5D	0F00	REG_7D	E51c
REG_1E	4C51	REG_3E	8E6A	REG_5E	3044	REG_7E	302E

REG_1F	*5454*	*REG_**3F***	*0000*	*REG_**5F***		*REG_**7F***	

修订历史

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1.0	2023/6/5	首次发布
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