Military 12540

Phase-Frequency Detector

ELECTRICALLY TESTED PER:
5962-8775201

The 12540 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the 1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of the Phase Detector #1 of the 4044.

- Operating Frequency = 80 MHz typical

ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+7.0	V_{dc}
Output Voltage	V_{OUT}		+5.5	V_{dc}
Input Voltage	V_{IN}		+5.5	V_{dc}
Operating Temperature Range	T_A	-55	+125	°C
Storage Temperature Range	T_{stg}	-65	+175	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8775207
3) 883: 12540/BXAJC

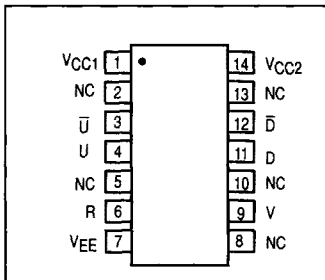
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: C

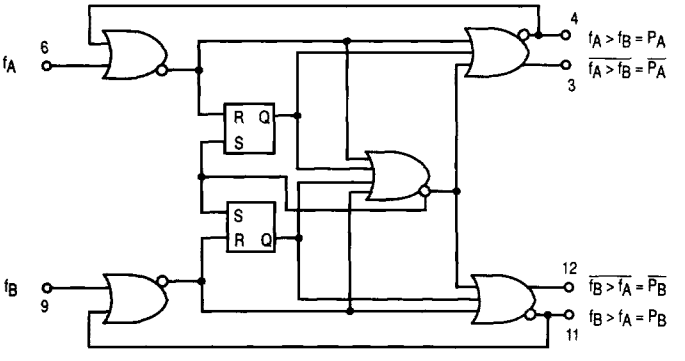
PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CC1}	1	GND
NC	2	OPEN
$\overline{U}$	3	51Ω to V_{TT}
U	4	51Ω to V_{TT}
NC	5	OPEN
R	6	2 kΩ to V_{TT}
V_{EE}	7	V_{CC}
NC	8	OPEN
V	9	2 kΩ to V_{TT}
NC	10	OPEN
D	11	51Ω to V_{TT}
$\overline{D}$	12	51Ω to V_{TT}
NC	13	OPEN
V_{CC2}	14	GND

BURN - IN CONDITIONS:
V_{CC} = 6.0 V MAX/ 5.0 V MIN



LOGIC DIAGRAM



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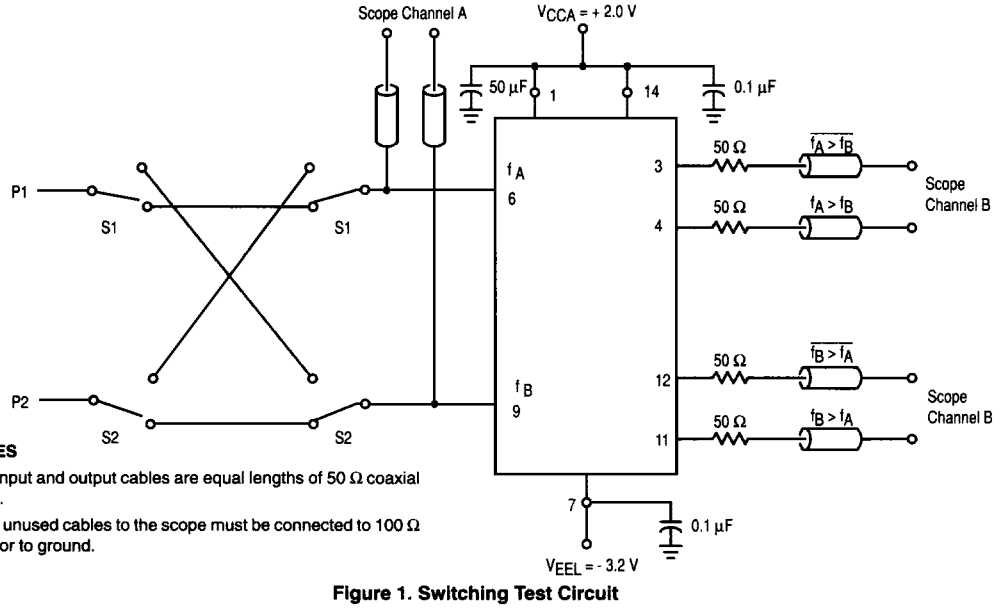

NOTES

1 All input and output cables are equal lengths of 50 Ω coaxial cable.

2. All unused cables to the scope must be connected to 100 Ω resistor to ground.

Figure 1. Switching Test Circuit

Functional Truth Table

INPUT		OUTPUT			
f_A	f_B	$f_A > f_B$	$f_B > f_A$	$\overline{f_A > f_B}$	$\overline{f_B > f_A}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = DON'T CARE

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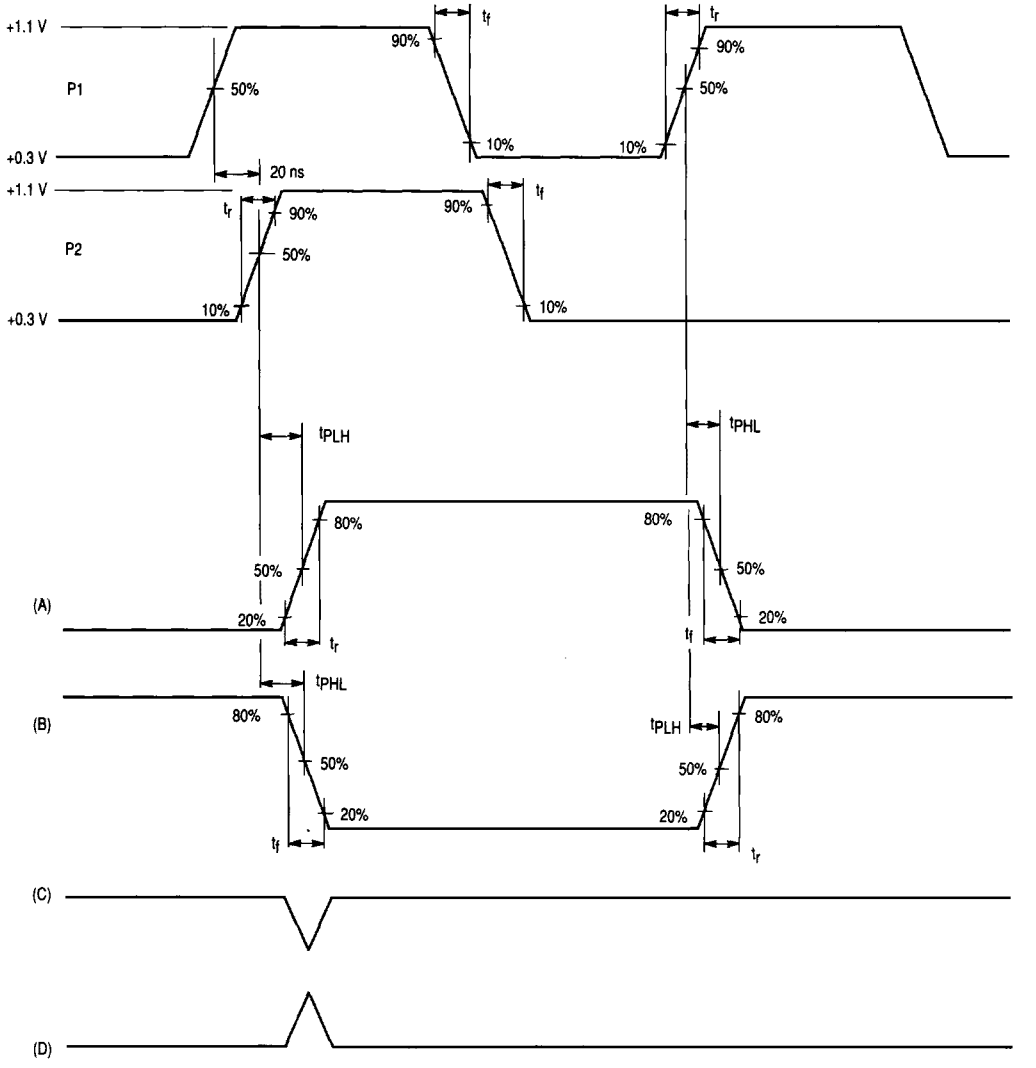

NOTES

1. P1, P2:
   a) PRF = 5.0 MHz.
   b) Duty Cycle 50%.
   c) $t_r = t_f = 1.5$ ns ± 0.2 ns (10% to 90%)

Figure 2. Test Circuit Waveforms

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QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}
T_A = 25 °C	+ 4.22	+3.21	+3.895	+3.525	+5.0	0
T_A = 125 °C	+ 4.37	+3.24	+4.000	+3.600	+5.0	0
T_A = -55 °C	+4.12	+3.14	+3.745	+3.490	+5.0	0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 kΩ to + 3.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH}	R - 1	V_{EE}	*	V_{CC}	P.U.T.
V_{OH}	High Voltage Output	4.07	4.22	4.175	4.37	3.92	4.12	V		3, 4, 11, 12	7	6, 9	1, 14	3, 4, 11, 12
V_{OL}	Low Voltage Output	3.21	3.44	3.24	3.515	3.14	3.405	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
V_{OHA}	Threshold Voltage High	4.05	4.22	4.155	4.37	3.90	4.12	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
V_{OLA}	Threshold Voltage Low	3.21	3.46	3.24	3.535	3.14	3.425	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
I_{INH}	Input Current High		350					μA	6, 9		7		1, 14	6, 9
I_E	Total Power Supply Current	-115	-60					μA			7		1, 14	7

NOTE: (This device will meet standard MECL logic levels using V_{EE} = - 5.2 Vdc and V_{CC} = 0V).
1. The outputs of the device must be tested by sequencing through the truth table for V_{OH}, V_{OL} tests.
2. The outputs of the device must be tested by sequencing through the truth table for V_{OHA}, V_{OLA} tests.
All input, power supply, and ground voltages must be maintained between tests.
3. Preconditioning for AC tests is accomplished by applying P1 for a minimum of two pulses prior to P2.
* = Per truth table.

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QUIESCENT LIMIT TABLE

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	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EEL}
T_A = 25 °C	+ 4.22	+ 3.21	+ 3.895	+ 3.525	+ 2.0	-3.0 or -3.2
T_A = 125 °C	+ 4.37	+ 3.24	+ 4.000	+ 3.600	+ 2.0	-3.0 or -3.2
T_A = -55 °C	+ 4.12	+ 3.14	+ 3.745	+ 3.490	+ 2.0	-3.0 or -3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 kΩ to 0.0 V					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{CCA}	P_1	P_2	V_{EEL}	P.U.T.
t_r	Rise Time		3.4		3.8		3.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_f	Fall Time		3.4		3.8		3.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+4+)	0	4.6	0	5.0	0	4.6	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+12+)	0	6.0	0	6.6	0	6.0	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+3-)	0	4.5	0	4.9	0	4.5	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+11-)	0	6.4	0	7.0	0	6.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+11+)	0	4.6	0	5.0	0	4.6	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+3+)	0	6.0	0	6.6	0	6.0	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+12-)	0	4.5	0	4.9	0	4.5	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+4+)	0	6.4	0	7.0	0	6.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12