

MA. 4248

**Message Entry and Read-out Device
(MEROD)**

Technical Manual



Racal-Comsec Limited

Milford Industrial Estate, Tollgate Road, Salisbury, Wilts., England.

Tel. Salisbury 23911 Telex: 477276

Prepared by Group Technical Handbooks Department, Racal Group Services Limited

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6. Replace the modules one at a time until the unit functions correctly. The unit can be functionally tested either:
 - (1) In the system.
 - (2) Using a Final Unit Test Jig (ST 45131).
 - (3) Back-to-back test.
7. It may be possible to locate a faulty component by reference to the circuit description (Part 5); the Final Unit Test procedure (Paragraph 9) may help to pin-point the source of a fault. Detailed fault-finding to component level requires the use of special equipment and is the subject of a separate publication.

FUNCTIONAL TEST

8. If it is necessary to check a unit while it is not fitted in an operational system, carry out a functional test. The functional test using a Final Unit Test Jig (Paragraph 9) is comprehensive; the back-to-back test (Paragraph 24) checks most functions but does not check the PTT signal output, error-correction or battery charging.

FINAL UNIT TEST

9. Equipment required:
 - (1) MA 4248 Final Unit Test Jig (ST 45131).
 - (2) DMM d.c. current range 0 to 2 A (e.g. Racal Dana Model 4003).
10. Note that the procedure assumes links LK2, LK4 and LK7 are present on the Main Processor Board. Make temporary links if necessary.

Overall Test

11. (1) With the test jig switched off, connect the HF, SATELLITE and PRINTER connectors to the Unit Under Test.
- (2) Connect the ammeter between the current test terminals and set the switch to METER.
- (3) Set the ammeter to the 2 amps range.
- (4) Turn on the test jig.
- (5) Check that the unit displays SELF TEST COMPLETE UNIT O.K.
- (6) Check that the test jig PASS indicator is on, indicating that it is operational.
- (7) Note the reading on the ammeter: if it is greater than 1 amp, turn off the test jig. (The reading should be 0.8 to 0.9 amp if a battery is fitted, 70 to 150 mA if a battery is not fitted to the unit).
- (8) Switch the meter switch to DIRECT.

2.
 - (1) Connect the REM KBD connector to the Unit Under Test.
 - (2) Select TEST NUMBER 0 and the correct printer speed on the test jig.
 - (3) Press the START TEST button. The TEST RUNNING indicator is on. The test takes approximately 2½ minutes to run.
 - (4) Check that the PASS indicator is on when the test is complete. If a FAIL indicator is on, follow the appropriate procedure detailed in Paragraphs 21 to 22.

On completion of the test routine, Z should be displayed in all thirty-two character positions on the display.

13.
 - (1) Press each character key in turn and check that the appropriate character appears in the display to the left of the cursor position.
 - (2) Press the → and ← keys and check that the characters scroll in the appropriate direction.
 - (3) Press the ☒ key and check that the character above the cursor line is deleted.
 - (4) Press the STORE and CLEAR keys simultaneously, and check that TRANSMIT MEMORY CLEARED appears in the display.
 - (5) Press the SEND, READ and ENTER keys in turn, and check that the corresponding indicator is on while each mode is selected.
14.
 - (1) Press the LIGHT key. Check that the backlight is on, and the mode indicators dim. Check that the backlight goes off after approximately ten seconds.
15.
 - (1) Press and hold down the OFF key. The display should go blank. Release the key and check that the unit displays SELF TEST COMPLETE UNIT O.K.
16. In Paragraphs 11 and 12 the unit has automatically carried out tests 1 to 5. Carry out Test 6 (1000 character message test) as follows:
 - (1) Select TEST NUMBER 6.
 - (2) Press the START TEST button. The test takes approximately 7½ minutes to run. If a failure occurs, see Paragraph 23.
17.
 - (1) If there has been no failure, turn off the test jig and disconnect the Unit Under Test.

Test 1 Failure

18. Fail 1 indicates a failure in Test 1, which checks for continuity on the external supply and 0 V connections. With the test jig still connected, select TEST NUMBER 1 and press the START TEST button. The FAIL indicator that is on at the end of the test indicates the type of fault:
- (1) Fail 1: Open circuit 0 V pin on one or more of the connectors.
 - (2) Fail 2: Open circuit V ext pin on one or more of the connectors.

in Test 2 Failure

19. Fail 2 indicates a failure in Test 2, which operates the Enter Format Ø mode and then uses Format 1 to display Z in all character positions. At the end of the test, control is returned to the Unit Under Test keyboard to enable key and display operation testing. With the test jig still connected, select TEST NUMBER 2 and press the START TEST button. The FAIL indicator that is on at the end of the test indicates the type of fault:
- (1) Fail 1: Failed in the Format Ø set-up mode. Suspect the Main Processor Board.
 - (2) Fail 2: Failed in Format 1 character entry. Suspect the Main Processor Board.

Test 3 Failure

20. Fail 3 indicates a failure in Test 3, which enters characters into the transmit store and then scrolls and edits the store. With the test jig still connected, select TEST NUMBER 3 and press the START TEST button. The FAIL indicator that is on at the end of the test indicates the type of fault:
- (1) Fail 1: Failed in the Format Ø set-up mode. Suspect the Main Processor Board and then the Power Board.
 - (2) Fail 2: Failed in entering a message. Suspect the Main Processor Board and then the Power Board.
 - (3) Fail 3: Failed in editing a message. Suspect the Main Processor Board.
 - (4) Fail 4: Failed in selecting Enter mode. Suspect the Main Processor Board.
 - (5) Fail 5: Failed to print Tx message correctly. Check the printer speed then suspect the Main Processor Board and the Power Board.

Test 4 Failure

21. Fail 4 indicates a failure in Test 4, which checks that the unit can send and receive HF messages. With the test jig still connected, select TEST NUMBER 4 and press the START TEST button. The FAIL indicator that is on at the end of the test indicates the type of fault:
- (1) Fail 1: Failed in the Format Ø set-up mode. Suspect the Main Processor Board.
 - (2) Fail 2: Failed to transmit an HF message correctly. Suspect the Sync I/O Board.
 - (3) Fail 3: Failed to receive an HF Allcall message. Suspect the Sync I/O Board.
 - (4) Fail 4: Failed to receive an HF Selcall message. Suspect the Sync I/O Board.
 - (5) Fail 5: Failed to error-correct an HF message which had maximum allowable errors. Suspect the Main Processor Board and the Sync I/O Board.
 - (6) Fail 6: Failed to print a received HF message. Suspect the Main Processor Board and the Power Board.

Test 5 Failure

22. Fail 5 indicates a failure in Test 5, which checks that the unit can send and receive satellite radio messages. With the test jig still connected, select TEST NUMBER 5 and press the START TEST button. The FAIL indicator that is on at the end of the test indicates the type of fault:
- (1) Fail 1: Failed in the Format Ø set-up mode. Suspect the Main Processor Board.
 - (2) Fail 2: Failed when transmitting low and high speed messages. Suspect the Sync I/O Board and Main Processor Board and then the Power Board.
 - (3) Fail 3: Failed to receive correctly a high-speed Allcall message. Suspect the Sync I/O Board and the Main Processor Board, and then the Power Board.
 - (4) Fail 4: Failed to receive correctly a high-speed Selcall message. Suspect the Sync I/O Board.
 - (5) Fail 5: Failed to receive correctly a high-speed message containing maximum errors. Suspect the Sync I/O Board and then the Main Processor Board.
 - (6) Fail 6: Failed to receive correctly a low-speed Selcall message. Suspect the Sync I/O Board.

Test 6 Failure

23. Test 6 (Paragraph 13) enters a 1000 character message, sends and checks it and then checks for correct reception of a 1000 character HF message. The FAIL indicator that is on at the end of the test indicates the type of fault.
- (1) Fail 1: Failed in the Format Ø set-up mode. Suspect the Main Processor Board.
 - (2) Fail 2: Failed to transmit 1000 characters correctly. Suspect the Main Processor Board then the Sync I/O Board.
 - (3) Fail 3: Failed to receive a 1000 character message correctly. Suspect the Sync I/O Board and then the Main Processor Board.

BACK-TO-BACK TEST

24. Connect the unit-under-test to a fully-tested MA 4248, using cable assembly 452976; if internal batteries are not fitted, connect power to the two units (12 to 32 V d.c. approx. 120 mA). Connect a printer, if available.
25. Operate the unit-under-test in all modes, sending and receiving, and check that the read-out/print-out is correct.
26. Note that this test does not check the PTT output, error correction or battery charging. The test can be performed only if both units are set for 25 mV rms or greater output. A comprehensive functional test can be carried out only by using the unit in an operational system or a Final Unit Test Jig.

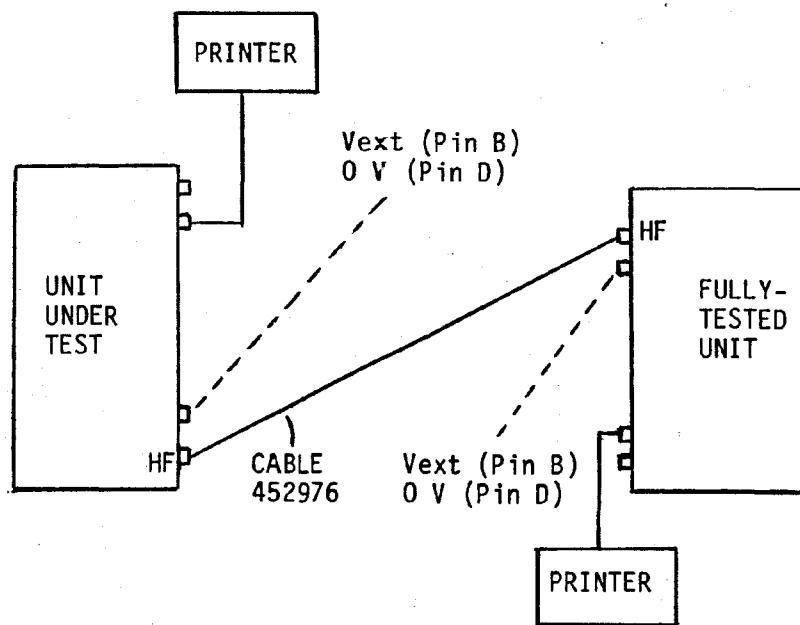


Fig. 6.1 Back-To-Back Test: Equipment

RETURNING TO SERVICE

27. When a unit has been opened, the fault rectified, and the unit tested, check that the desiccator sachets are blue (and not pink); replace if necessary; then carry out a pressure test (Chapter 3) to check that the unit is correctly sealed. If necessary charge the battery.

CHAPTER 2

DISMANTLING AND REPLACEMENT

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MA 4248

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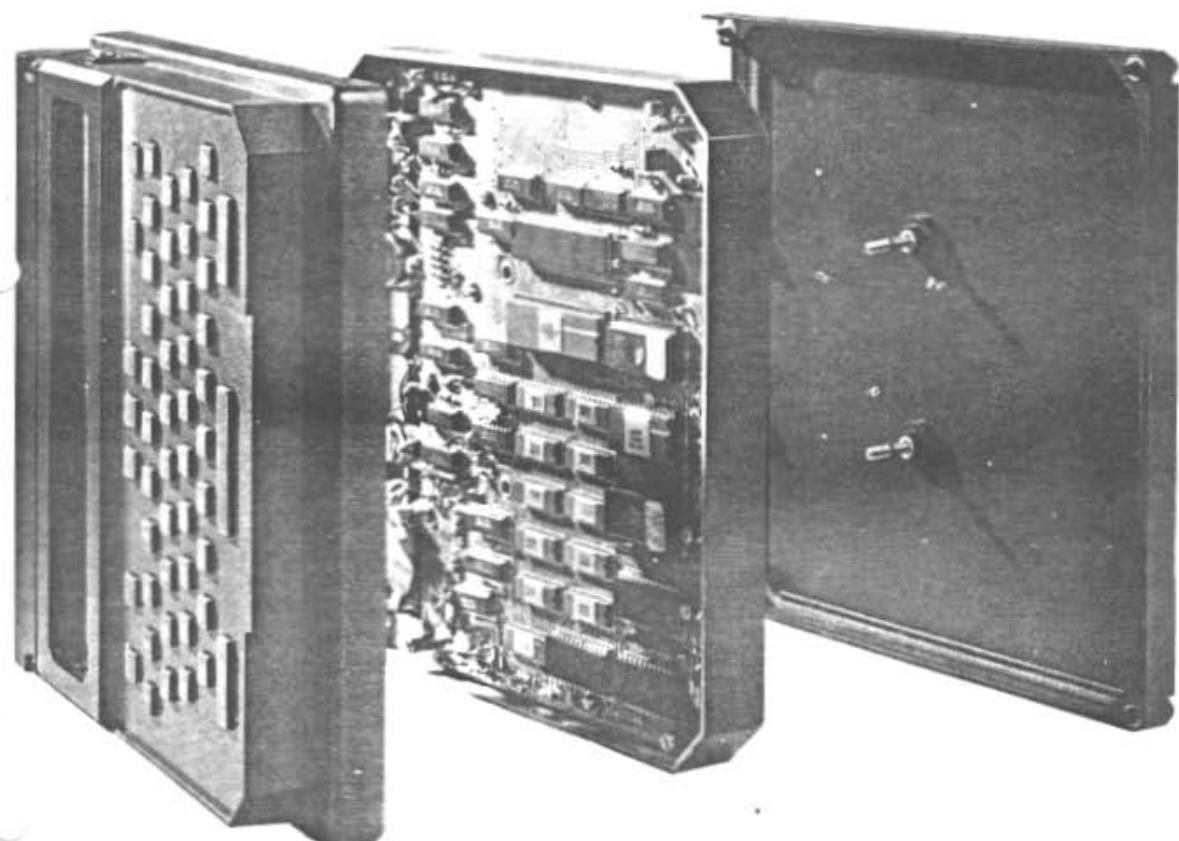
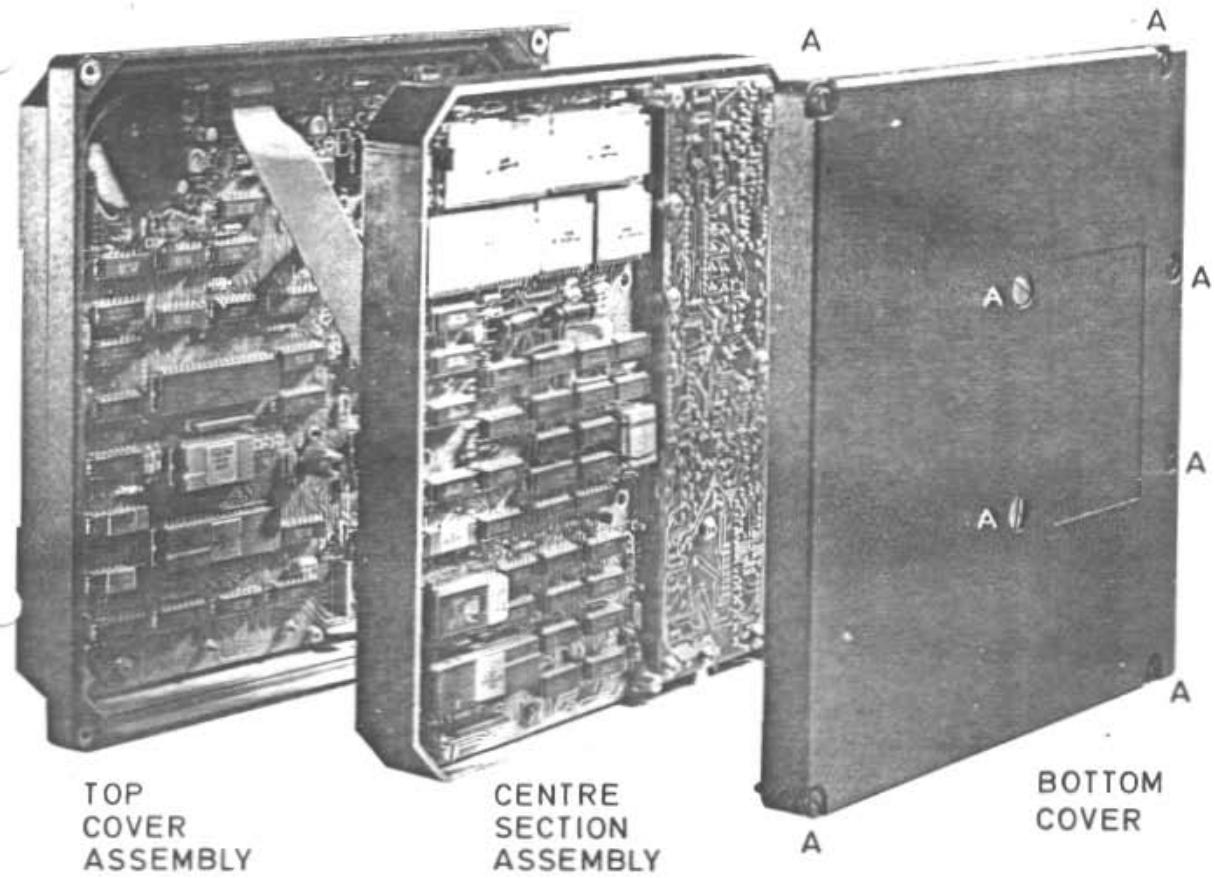


Fig. 6.2.1 MA 4248: Access to Inside the Unit

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CHAPTER 2

DISMANTLING AND REPLACEMENT

TABLE 1 TOOLS REQUIRED FOR DISMANTLING MA 4248

Screwdrivers	Flat-blade, approx 5 mm. Pozidrive, 1-point (for M3 screws) Pozidrive, 0-point (for M2.5 screws)
Nutdrivers	5.5 mm (for M3-threaded nuts). 5 mm (for M2.5-threaded nuts).
Open-ended spanner	3/8 inch across-the-flats.

ACCESS TO THE INSIDE OF THE MA 4248

- CAUTION 1. Disconnect all cables from the rear of the unit before dismantling it.
2. The unit is sealed to keep out dirt and moisture: do not dismantle it unless this is necessary, and dismantle only in a clean dry atmosphere; then carry out a pressure test before returning the unit to service.
1. (1) From the underside of the unit, slacken the eight M4 slot-head screws that secure the base to the top part of the unit. (Screws marked A in Figure 6.2.1. All eight screws are captive screws (O-rings hold them in place); the two centre screws are special screws with O-rings used as sealing washers, the other six have crinkle washers).
 - (2) Carefully separate the unit into three parts, as shown in Figure 6.2.1.
 - (3) When re-assembling the unit, check that the RFI/Weather gaskets are correctly positioned in the grooves in the top cover and bottom cover, with the wire-mesh side facing towards the centre (as in Figure 6.2.8).
 - (4) Before resealing a unit, check that the desiccator sachets are blue (and not pink); replace if necessary.

REMOVING THE MAIN REPLACEABLE MODULES

Main Processor Board Assembly

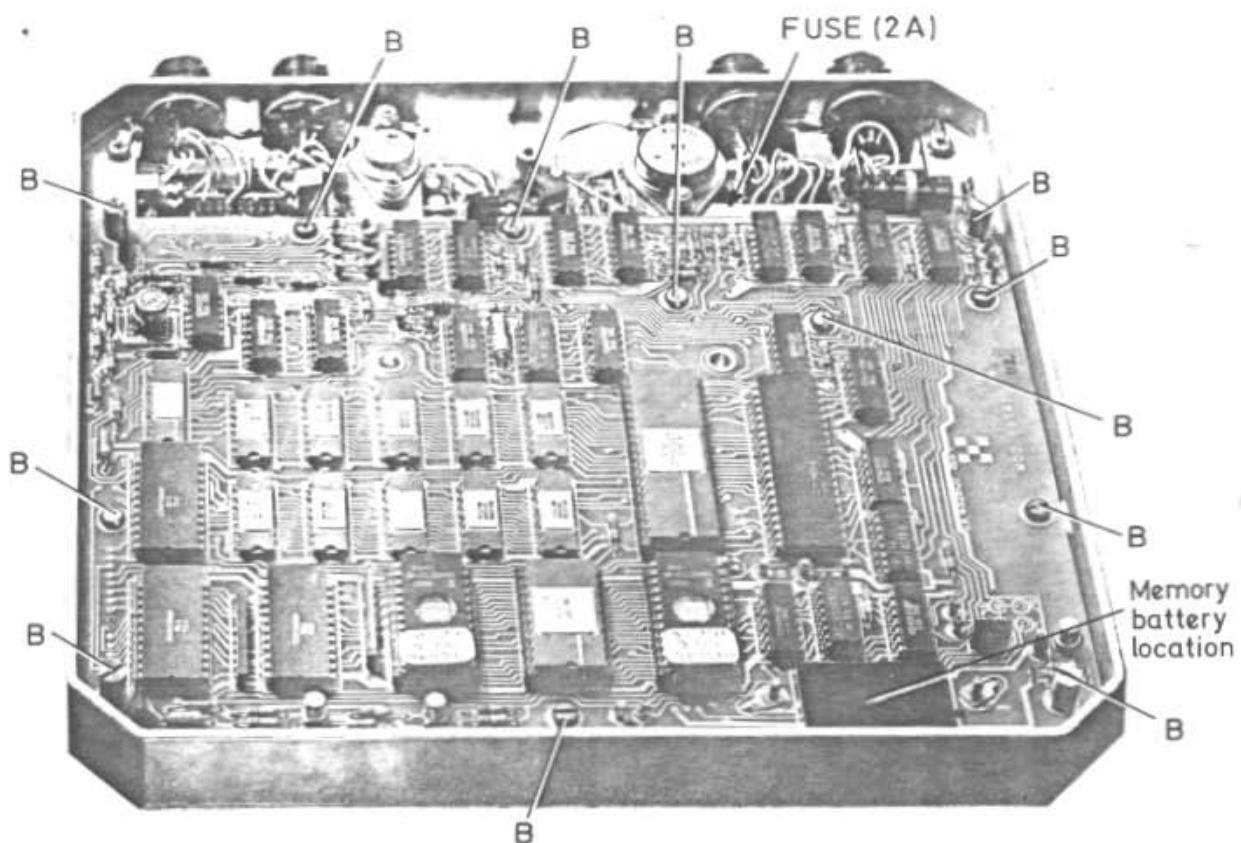
2. (1) Remove the eight slot-head screws and four slotted pillars (special screws) that secure the assembly to the centre section frame. (Screws and pillars marked B in Figure 6.2.2. All have plain washers under crinkle washers).
(2) Lift the board (complete with memory battery) from the centre section assembly.

Sync I/O Board Assembly

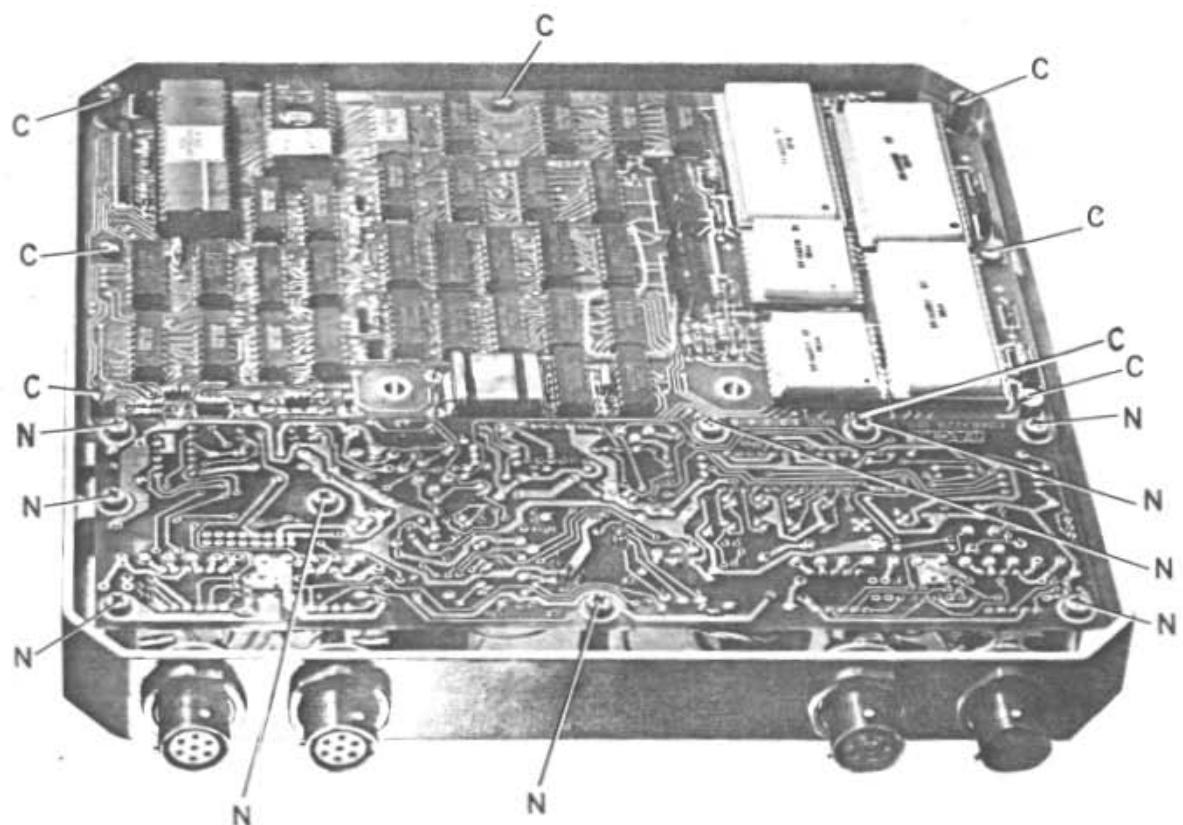
3. (1) Remove the four slot-head screws and four slotted pillars (special screws) that secure the assembly to the centre section frame. (Screws and pillars marked C in Figure 6.2.3. All have plain washers under crinkle washers).
(2) Lift the board from the centre section assembly.

Power Module Assembly

4. The Power Module Assembly includes the Power Board, centre section frame, external connectors.
 - (1) Disconnect the ribbon cable that connects the centre section to the top cover assembly: press the clips at the ends of the socket connector (on the Power Board) away from each other, and pull out the plug connector.
 - (2) Remove the Main Processor Board Assembly (Paragraph 2) and Sync I/O Board Assembly (Paragraph 3).
 - (3) Refit the Main Processor Board Assembly and Sync I/O Board Assembly to the replacement Power Module Assembly (make sure the strip connectors are in position); return the ribbon cable.



Removing the Main Processor Board Assembly(452607) Fig.6.2.2



Removing the Sync I/O Board Assembly(452606)

Fig.6.2.3

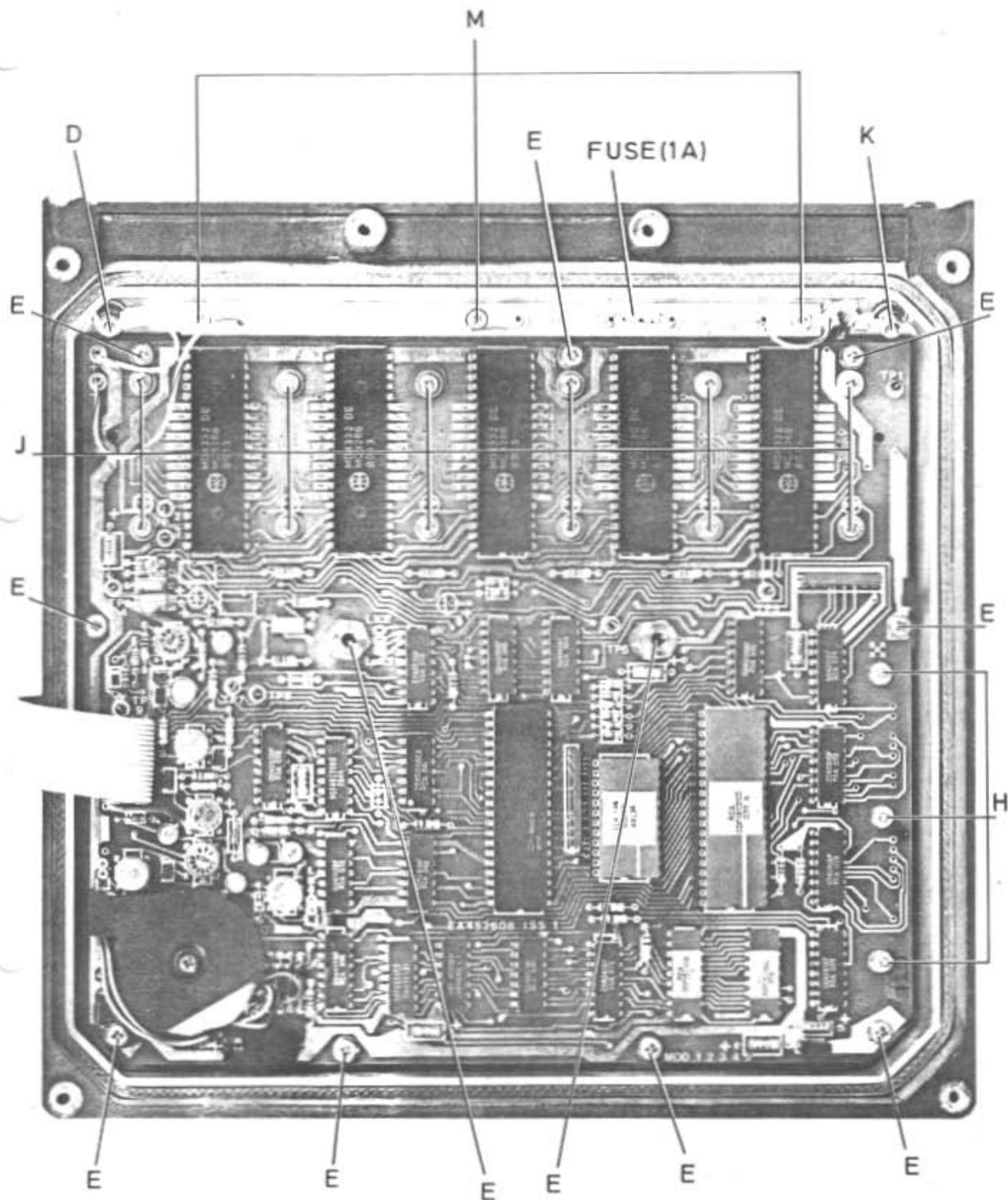


Fig.6.2.4 Removing the Man/Machine Interface Module Assembly (452635)

Man/Machine Interface Module Assembly

5. The Man/Machine Interface Module Assembly includes the Man/Machine Interface Board Assembly, Keyboard Assembly (PCB), plastic moulding (Display Board Moulding) and associated components.
 - (1) Disconnect the ribbon cable at the centre-section end (Paragraph 4(1)).
 - (2) Unsolder the wire from the Man/Machine Interface Board to the Fuseboard.
 - (3) Remove the M3 nut that secures the wire from the Man/Machine Interface Board to the +ve battery terminal. (Nut marked D in Figure 6.2.4).
 - (4) Remove the nine M3 slot-head (some units have cross-head) screws and two hexagonal pillars (PCB spacers) that secure the Man/Machine Interface Module Assembly to the top casting. (Screws and pillars marked E in Figure 6.2.4. The screws have crinkle washers; the one in the bottom left hand corner (i.e. through the toroidal transformer moulding) has a plain washer under a crinkle washer).
 - (5) When reassembling, return the nine screws and two pillars in the following order:
 - (a) Hexagonal pillars.
 - (b) The three longer screws at the top edge of the board (i.e. nearest to the Fuseboard).
 - (c) The other six screws.

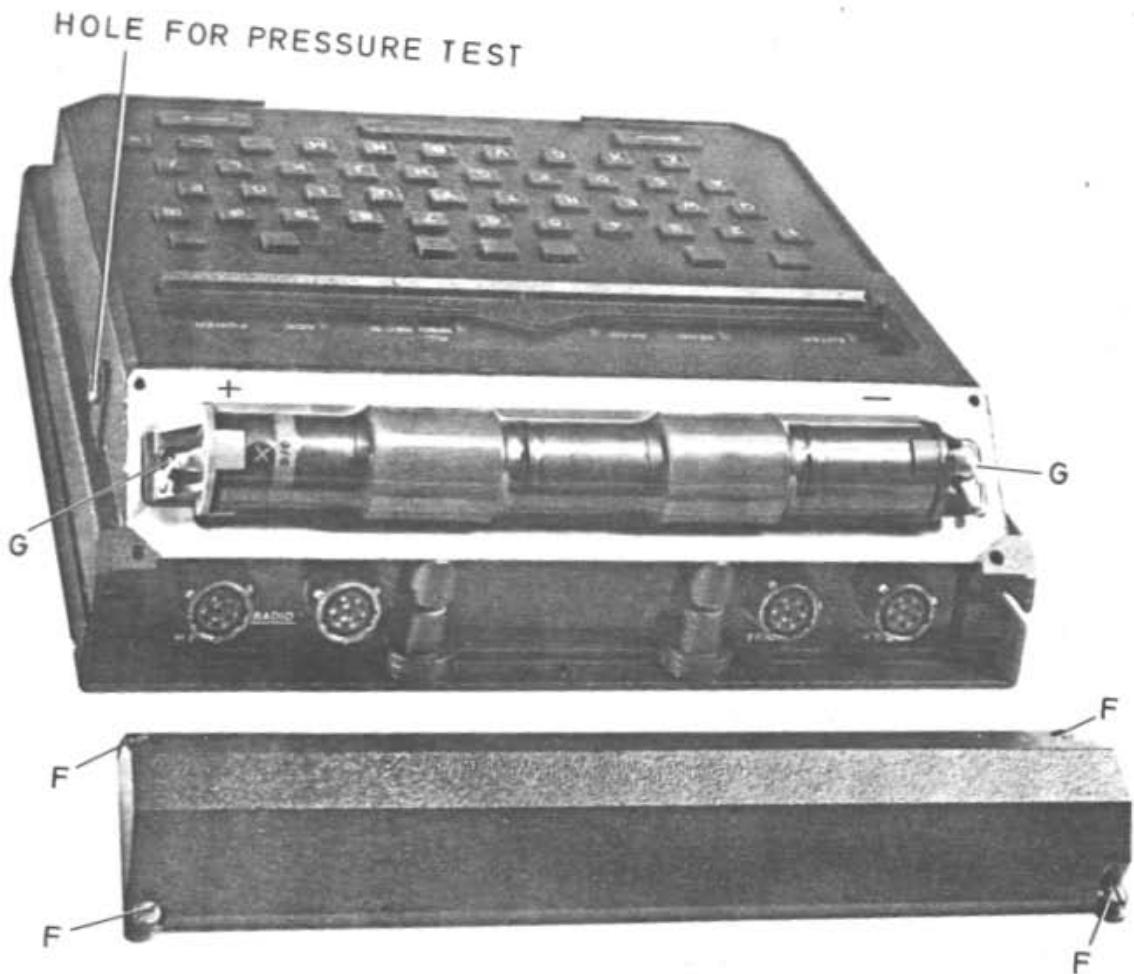


Fig. 6.2.5

Removing the Battery

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DISMANTLING THE MAIN MODULES

NOTE: Before reassembling an assembly, refer to the note on elastomeric connectors, Paragraph 18.

Man/Machine Interface Module Assembly

9. The Man/Machine Interface Module Assembly can be broken-down into its component parts as described in Paragraphs 10 to 15.

Keyboard Assembly (PCB)

10. (1) Remove the three M2.5 nuts that secure the mounting studs of the Keyboard Assembly (PCB) to the Man/Machine Interface Module Assembly. (Nuts marked H in Figure 6.2.4. The nuts have crinkle washers). Carefully separate the Keyboard Assembly from the module. Note that the two 11-way connector strips that go via apertures in the plastic moulding may now be free to fall out when the module is turned over, so carefully remove them.

Display and Backlight

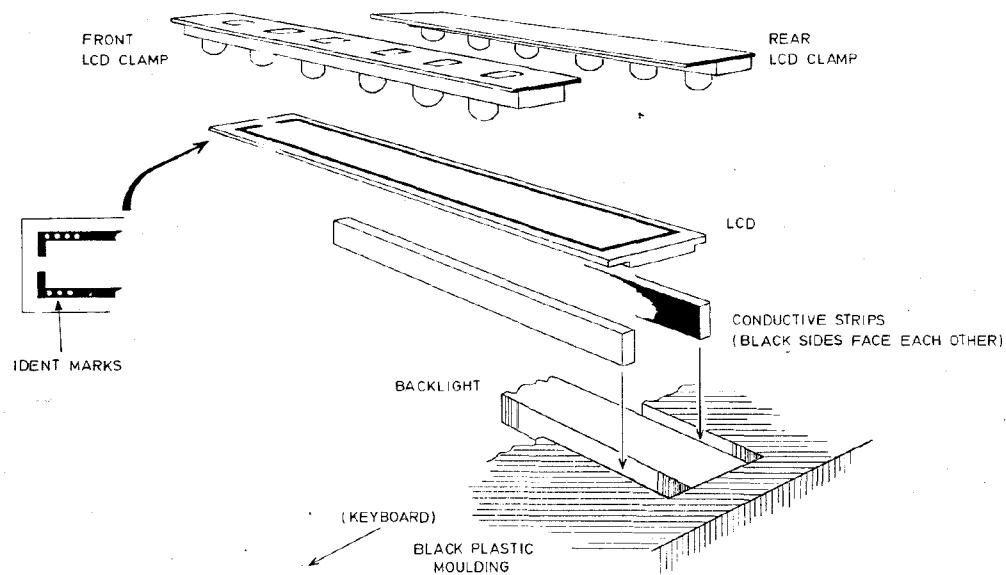
11. (1) Slacken the twelve M2.5 screws that secure the LCD clamps. (Screws marked J in Figure 6.2.4. The screws have insulating washers). Note that when all screws are removed, the LCD and associated components are free to fall out, so hold the module by the LCD clamps while removing the screws, then turn the assembly over to remove the display and clamps. Keep the Man/Machine Interface Board in position until the LCD and associated components have been removed (i.e. until Paragraph 11(3)).
- (2) Carefully lift off the LCD clamps, LCD and conductive strips (shown in Figure 6.2.6).
- (3) Separate the Man/Machine Interface Board from the plastic moulding. Unsolder the wires from the backlight to the board and lift off the backlight assembly. The light slides out from its plastic holder.

12. When reassembling, the order is as follows:

- (1) Slide the backlight into its holder, place the holder on its support pad then position the assembly on the Man/Machine Interface Board. Small pegs at each end of the holder fit into holes in the PCB, and ensure correct alignment. Push the wires through the holes at the edges of the PCB and solder them into the holes.
- (2) Place the Man/Machine Interface Board in position against the plastic moulding. There are two locating pips on the moulding, near the ends of the LCD aperture.
- (3) Insert the two conductive strips into the gaps between the backlight holder and the sides of the aperture in the black plastic moulding. Ensure that the black faces of the connector strips face each other (see Figure. 6.2.6). (Locate the strips at the left hand ends of the slots, with the clearance at the right-hand end).
- (4) Place the LCD in position with the left-hand reference edge against the locating pip on the plastic moulding. The end with the ident spots goes to the left (viewed from the keyboard). (See Figure 6.2.6).
- (5) Place the front and rear LCD clamps in position. Take care not to damage the LEDs. Insert the twelve screws that secure the clamps. Tighten the screws evenly.

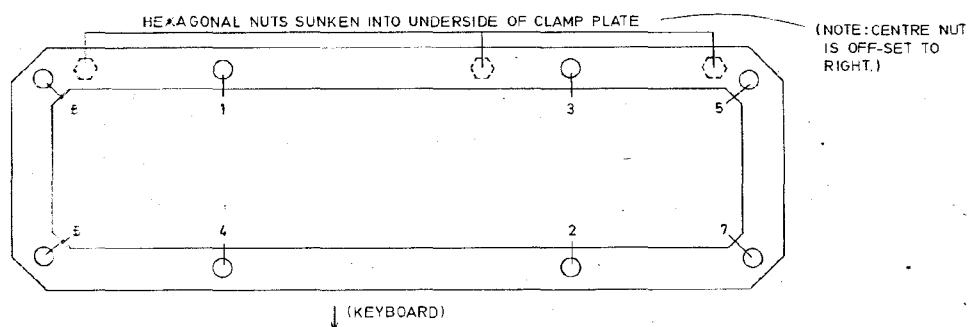
Top Cover Assembly (Top Casting Assembly)

13. The flexible keysheet can be lifted out from the top casting when the Man/Machine Interface Module Assembly has been removed. If the three fibre-glass spacers (in the space bar and scroll keys) are removed from their slots in the keysheet, note when reassembling that the straight edges are at the bottoms of the slots.
14. To remove the Fuseboard, unsolder the wire from the Man/Machine Interface Board, remove the M3 nut that secures the wire from the Fuseboard to the -ve battery terminal. (Nut marked K in Figure 6.2.4), and remove the three M2.5 cross-head screws that secure the Fuseboard to the top casting. (Screws marked M in Figure 6.2.4. The screws have crinkle washers).
15. The LCD window is secured by eight M3 cross-head screws (and crinkle washers). When reassembling, locate the sealing ring in the groove in the top casting, position the window (with the built-in gasket side downwards), then locate the clamp plate (with the hexagonal nuts facing downwards) over the window. Insert all screws before tightening any of them; tighten evenly in the order shown in Figure 6.2.7.
16. The polarising screen (if fitted) is held in place by the two viewing-screen-holders, one at each end of the screen, which clip into recesses in the top cover assembly.



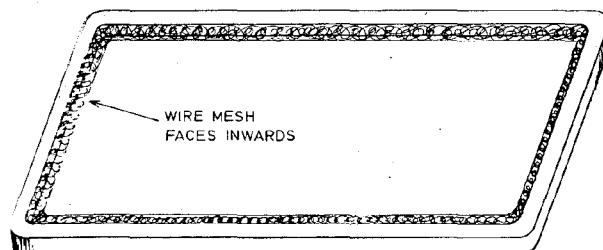
Fitting the LCD

Fig.6.2.6



Order of Tightening LCD Window Screws

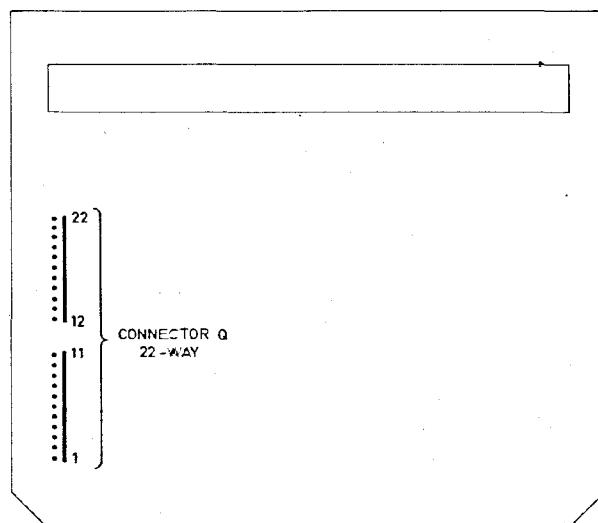
Fig.6.2.7



Orientation of RFI/ Weather Gaskets

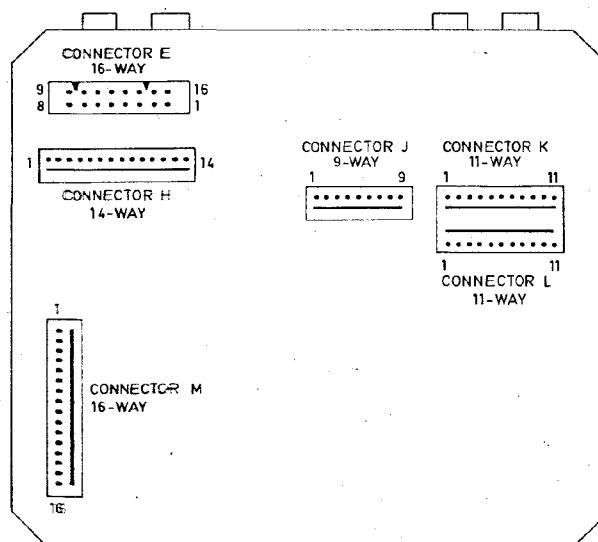
Fig.6.2.8

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VIEWED FROM KEYBOARD SIDE

TOP COVER ASSEMBLY



VIEWED FROM MAIN PROCESSOR BOARD SIDE

CENTRE SECTION

Fig.6.2.9

Internal Connectors

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Power Board

17. (1) Remove the nine M3 screws that secure the Power Board to the centre section frame (screws marked N in Figure 6.2.3. The screws have crinkle washers).
- (2) Carefully hinge the board away from the frame by pulling the edge of the board nearest the centre of the frame. This provides access to unsolder the wires that connect the board to the power transistors. Label the wires or make a note of their destinations (to facilitate reassembly). (The Power Board can be removed complete with rear connectors: remove the nuts that hold the rear connectors to the centre frame).

Elastomeric Connectors

18. The connector strips in the elastomeric connectors can be pulled out and replacement strips inserted. The orientation of the strips is shown in Figure 6.2.9. When handling elastomeric connectors, take care to prevent cracking and contamination, which result in high-resistance contacts. It is recommended that new connectors are fitted whenever the associated boards have been removed. Also, before refitting the boards, clean the board contacts that touch the elastomeric connectors (e.g. rub them gently with a soft pencil-eraser).

PRESSURE TEST

19. (1) Remove the slot-head M4 screw from the right-hand side of the top cover (Figure 6.2.5). Check that the sealing ring on the screw is undamaged; replace it if necessary.
- (2) Connect an airline to the M4 threaded hole in the top cover and pressurise the unit to 2.5 to 3 psi (above atmosphere pressure).
- (3) Place the pressurised unit in a container of water such that the water covers the seals. Wait for about one minute for trapped air to be released then look for bubbles. Move the unit around in the water. If bubbles appear, investigate the leak: one of the gaskets may not be seated properly, or it may be bridged.
- (4) Remove the unit from the water, remove any surface water, disconnect the air line, return the M4 screw (check that the sealing ring is on the screw); dry the unit before using it or opening it.

CHAPTER 3

COMPONENTS LIST

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CHAPTER 3

COMPONENTS LIST

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
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MAIN ASSEMBLIES

Top Cover Assembly	452636
Centre Section Assembly	452638
Battery Assembly	452728
Bottom Cover	452509

TOP COVER ASSEMBLY (452636)

Top Casting Assembly	452634
Man/Machine Interface Module Assembly	452635
Fuseboard Assembly	452693
Keysheet Moulding (Flexible)	452346
Fibreglass Spacer (for Space Bar)	452596/1
Fibreglass Spacer (for Scroll Key)	452596/2
PCB Spacer (hexagonal pillar)	452648

CENTRE SECTION ASSEMBLY (452638)

Power Module Assembly	452637
Sync I/O Board Assembly	452606
Main Processor Board Assembly	452607
14-way Connector Strip (H)	461151
9-way Connector Strip (J)	461152
11-way Connector Strip (K)	461153
11-way Connector Strip (L)	461154
16-way Connector Strip (M)	461156

BATTERY ASSEMBLY (452738)

Battery Pack (1 amp)	461166
Battery End Cap (+)	452645/1
Battery End Cap (-)	452645/2

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
<u>TOP-CASTING ASSEMBLY (452634)</u>					
		Battery Compartment Cover			452511
		Screened Window			452600
		Window Clamp Plate			452599
		Window Sealing Ring			452603
<u>MAN/MACHINE INTERFACE MODULE ASSEMBLY (452635)</u>					
		Man/Machine Interface Board Assembly			452608
		Keyboard Assembly			452609
		Front LCD Clamp			452757
		Rear LCD Clamp			452758
		Display Board (Black Plastic) Moulding			452602
		Liquid Crystal Display			461162/2
		11-way Connector Strip (Q)			461156
<u>FUSE BOARD ASSEMBLY (452693)</u>					
	1 amp Fuse				D02154
<u>POWER MODULE ASSEMBLY (452637)</u>					
		Power Board Assembly			452610
		Centre Frame			452363
		Transistor MJ 2955			D01834
		Transistor 2N4898			919780
	100 uF	Capacitor, 40 V			D02361
SKD		HF Radio Connector Assembly			452705
SKC		Satellite Radio Connector Assembly			452704
SKB		Printer Connector Assembly			452703
SKA		Connector Assembly (Not used)			452702

Cct. Ref.	Value	Description	Rat.	Tol %	Racial Part Number
<u>MAN/MACHINE INTERFACE BOARD ASSEMBLY (452608)</u>					
<u>Resistors (ohms)</u>					
R1	1 M	Carbon Film	1/4	5	D01959
R2	1 M	Carbon Film	1/4	5	D01959
R3	1 M	Carbon Film	1/4	5	D01959
R4	1 M	Carbon Film	1/4	5	D01959
R5	100 k	Carbon Film	1/4	5	D01944
R6	1 M	Carbon Film	1/4	5	D01959
R7	22 k	Carbon Film	1/4	5	D01934
R8	1 M	Variable		20	937423
R9	56 k	Metal Oxide	1/4	2	D02168
R10	182 k	Metal Film	1/4	0.5	D01854
R11	110 k	Metal Film	1/4	0.5	D01853
R12	110 k	Metal Film	1/4	0.5	D01853
R13	182 k	Metal Film	1/4	0.5	D01854
R14	Not used				
R15	Not used				
R16	10 M	Carbon Film	1/3	10	925472
R17	330 k	Metal Oxide	1/4	2	D02169
R18	10 M	Carbon Film	1/3	10	925472
R19	6k8	Carbon Film	1/4	5	D01928
R20	27 k	Carbon Film	1/4	5	D01935
R21	15 k	Carbon Film	1/4	5	D01932
R22	68 k	Carbon Film	1/4	5	D01941
R23	47 k	Carbon Film	1/4	5	D01939
R24	47 k	Carbon Film	1/4	5	D01939
R25	330 k	Carbon Film	1/4	5	D01952
R26	680 k	Carbon Film	1/4	5	D01957
R27	680 k	Carbon Film	1/4	5	D01957
R28	1k5	Carbon Film	1/4	5	D01920
R29	1k5	Carbon Film	1/4	5	D01920
R30	1k5	Carbon Film	1/4	5	D01920
R31	1k5	Carbon Film	1/4	5	D01920
R32	1k5	Carbon Film	1/4	5	D01920
R33	1k5	Carbon Film	1/4	5	D01920
R34	100 k	Carbon Film	1/4	5	D01944
R35	100 k	Carbon Film	1/4	5	D01944
R36	100 k	Carbon Film	1/4	5	D01944
RML1	10 k	SIL Network	1.2	2	938367
RML2	22 k	SIL Network	1	2	D01858

Cct. Ref.	Value	Description	Rate	Tol %	Racial Part Number
<u>Capacitors (F)</u>					
C1	15 u	Tubular Tantalum	6	10	D01845
C2	Not used				
C3	Not used				
C4	1 n.	Ceramic Monolithic	100		935865
C5	6u8	Tubular Tantalum	25	10	D02023
C6	1 n	Ceramic Monolithic	100		935865
C7	Not used				
C8	Not used				
C9	6u8	Tubular Tantalum	25	10	D02023
C10	15 u	Tubular Tantalum	6	10	D01845
C11	1 u	Tubular Tantalum	25	10	932038
C12	470 p	Ceramic Monolithic	100		D01841
C13	1 n	Ceramic Monolithic	100		935865
C14	470 p	Ceramic Monolithic	100		D01841
C15	15 u	Tubular Tantalum	6	10	D01845
C16	220 u	Electrolytic	10	-10 +50	D02161
C17	15 u	Tubular Tantalum	6	10	D01845
C18	15 u	Tubular Tantalum	6	10	D01845
C19	15 u	Tubular Tantalum	6	10	D01845
C20	0u47	Ceramic Monolithic			D01842
C21	10 u	Tubular Tantalum	20	10	932042
C22	0u47	Ceramic Monolithic			D01842
C23	0u47	Ceramic Monolithic			D01842
C24	15 u	Tubular Tantalum	6	10	D01845

Transformer

T1 Torroidal 461143

Diodes

D1	1N4149	923222
D2	1N4149	923222
D3	1N4149	923222
D4	1N4149	923222
D5	1N4149	923222

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D6		1N4149			923222
D7		1N4149			923222
D8	Not used				
D9	Not used				
D10	Not used				
D11		1N4149			923222
D12		1N4149			923222
D13		1N4149			923222
D14		1N4149			923222
D15		Light-emitting			D01840
D16		Light-emitting			D01840
D17		Light-emitting			D01840
D18		Light-emitting			D01840
D19		Light-emitting			D01840
D20		Light-emitting			D01840
D21		1N4149			923222
D22		1N4149			923222
D23		1N4149			923222

Transistors

TR1	BC108	915460
TR2	BC178B	932182
TR3	BC178B	932182
TR4	BC108	915460
TR5	BC178B	932182

Integrated Circuits

ML1	Eight-channel Multiplexer/demultiplexer	D02460
ML2	32-Word x 8-Bit Static RAM	934727
ML3	32-Word x 8-Bit Static RAM	934727
ML4	Quad Clocked D-type Latches	930873
ML5	Quad Two-input OR Gates	928640
ML6	Triple Three-input NAND Gates	D02157
ML7	Decade Counter	D01807
ML8	Eight-channel Multiplexer/demultiplexer	D02460
ML9	Microprocessor	D02143
ML10	1 k byte ROM	461141

MA 4248

Part 6
3-5

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
ML11		UART			D01827
ML12		Quad Two-input AND Gates			928641
ML13		Dual D-type Bistables			D01805
ML14		Programmable Op Amp			D02514
ML15		Op Amp			D01801
ML16		Programmable Op Amp			D02514
ML17		Eight-channel Multiplexer/demultiplexer			D02460
ML18		Hex Schmitt Triggers			D01191
ML19		Quad D-type Bistables			D01821
ML20		Triplex Two-channel Multiplexer/demultiplexer			930864
ML21		Programmable Op Amp			D02514
ML22		Programmable Op Amp			D02514
ML23		Eight-channel Multiplexer/demultiplexer			D02460
ML24		Hex D-type Bistables			D01820
ML25		Eight-stage Shift Register			935450
ML26		Hex D-type Bistables			D01820
ML27		Triplex two-channel Multiplexer/demultiplexer			930864
ML28		Op Amp			D01801
ML29		32-bit LCD Driver			D01816
ML30		32-bit LCD Driver			D01816
ML31		32-bit LCD Driver			D01816
ML32		32-bit LCD Driver			D01816
ML33		32-bit LCD Driver			D01816
ML34		Quad Exclusive-OR Gates			D01811

Miscellaneous

Conductive Strip (at sides of LCD)	461147
LCD Backlight	461139
DIL 24-way connector	933813
DIL 40-way connector	933814
Socket (at end of ribbon cable)	D01867
Transipad	929728
Avlug	914054
Test Point	924853

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
<u>SYNC I/O BOARD ASSEMBLY (452606)</u>					
<u>Resistors (ohms)</u>					
R1	1 M	Carbon Film	1/4	5	D01959
R2	56 k	Carbon Film	1/4	5	D01940
R3	3k3	Carbon Film	1/4	5	D01924
R4	220 k	Carbon Film	1/4	5	D01948
R5	220 k	Carbon Film	1/4	5	D01948
R6	220 k	Carbon Film	1/4	5	D01948
R7	220 k	Carbon Film	1/4	5	D01948
R8	220 k	Carbon Film	1/4	5	D01948
R9	220 k	Carbon Film	1/4	5	D01948
R10	10 M	Carbon Film	1/3	10	925472
R11	220 k	Carbon Film	1/4	5	D01948
R12	220 k	Carbon Film	1/4	5	D01948
R13	270	Carbon Film	1/4	5	D01910
R14	270	Carbon Film	1/4	5	D01910
R15	47	Carbon Film	1/4	5	D01501
RML1	10 k	SIL Network	1.2	2	938367
<u>Capacitors (F)</u>					
C1	10 n	Ceramic Monolithic	100	20	932021
C2	47 p	Ceramic	100	20	933576
C3	47 p	Ceramic	100	20	933576
C4	10 u	Electrolytic	40	20	D02163
C5	10 u	Electrolytic	40	20	D02163
C6	15 u	Tubular Tantalum	6	10	D01845
C7	15 u	Tubular Tantalum	6	10	D01845
C8	15 u	Tubular Tantalum	6	10	D01845
C9	15 u	Tubular Tantalum	6	10	D01845
C10	6u8	Tubular Tantalum	4	10	D01844
C11	6u8	Tubular Tantalum	4	10	D01844
C12	6u8	Tubular Tantalum	4	10	D01844
C13	6u8	Tubular Tantalum	4	10	D01844
C14	6u8	Tubular Tantalum	4	10	D01844
C15	0u47	Ceramic Monolithic			D01842

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
C16	0u47	Ceramic Monolithic			D01842
C17	0u47	Ceramic Monolithic			D01842
C18	0u47	Ceramic Monolithic			D01842
C19	15 u	Tubular Tantalum	6	10	D01845
C20	15 u	Tubular Tantalum	6	10	D01845
C21	15 u	Tubular Tantalum	6	10	D01845
C22	15 u	Tubular Tantalum	6	10	D01845

Integrated Circuits

ML1	Space-Filter Hybrid	466007
ML2	Modulator Hybrid	466011
ML3	Dual D-type Bistables	D01806
ML4	Dual D-type Bistables	D01806
ML5	Triple Three-input NOR Gates	D01809
ML6	Quad Two-input AND Gates	D01815
ML7	Quad Two-input OR Gates	D01814
ML8	7-stage Binary Counter	D01808
ML9	Programmable Bit-rate Generator	D01824
ML10	Dual D-type Bistables	D01806
ML11	Triple two-channel Multiplexer/demultiplexers	930864
ML12	Triple two-channel Multiplexer/demultiplexers	930864
ML13	Triple two-channel Multiplexer/demultiplexers	930864
ML14	AGC Hybrid	466010
ML15	Quad D-type Bistables	D01821
ML16	Programmable 4-bit Counter	D01822
ML17	Hex Inverters	D01813
ML18	1kx1 RAM	D01828
ML19	7-stage Binary Counter	D01808
ML20	Dual D-type Bistables	D01806
ML21	Quad Exclusive OR Gates	D01811
ML22	Quad Two-input NAND Gates	D01804
ML23	Quad 64-bit Static Shift Registers	D01825
ML24	Mark-Filter Hybrid	466008
ML25	Detector Hybrid	466009
ML26	Hex Inverters	D01813
ML27	Dual Four-bit Binary Counters	D01819
ML28	Dual Four-bit Binary Counters	D01819
ML29	Quad Clocked D-type Latches	930873
ML30	BCD to Decimal Decoder	D01810

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML31		BCD-to-decimal Decoder			D01810
ML32		Microprocessor			D02143
ML33		8-stage Static Shift Register			927050
ML34		Hex D-type Bistables			D01820
ML35		Hex Strobed Buffer/Inverters			D01817
ML36		Hex Strobed Buffer/Inverters			D01817
ML37		32-word x 8-bit RAM			934727
ML38		1 k byte ROM			461142

Miscellaneous

XL1	Crystal 2.4576 MHz	461063
	Crystal Support Pad	452811
	DIL 24-way connector	933813
	DIL 40-way connector	933814
	Avlug	914054
	Test Point	924853

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
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MAIN PROCESSOR BOARD ASSEMBLY (452607)

Resistors (ohms)

			<u>W</u>		
R1	220 k	Carbon Film	1/4	5	D01948
R2	100 k	Carbon Film	1/4	5	D01944
R3	27 k	Carbon Film	1/4	5	D01935
R4	100 k	Carbon Film	1/4	5	D01944
R5	220 k	Carbon Film	1/4	5	D01948
R6	220 k	Carbon Film	1/4	5	D01948
R7	1 k	Carbon Film	1/4	5	D01918
R8	220 k	Carbon Film	1/4	5	D01948
R9	100 k	Carbon Film	1/4	5	D01944
R10	1 k	Carbon Film	1/4	5	D01918
R11	220 k	Carbon Film	1/4	5	D01948
R12	220 k	Carbon Film	1/4	5	D01948
R13	27 k	Carbon Film	1/4	5	D01935
R14	220 k	Carbon Film	1/4	5	D01948
R15	100 k	Carbon Film	1/4	5	D01944
R16	47 k	Carbon Film	1/4	5	D01939
R17	220 k	Carbon Film	1/4	5	D01948
R18	1 M	Carbon Film	1/4	5	D01959
R19	220 k	Carbon Film	1/4	5	D01948
R20	220 k	Carbon Film	1/4	5	D01948
R21	15 k	Carbon Film	1/4	5	D01932
R22	47 k	Carbon Film	1/4	5	D01939
R23	100 k	Carbon Film	1/4	5	D01944
R24	Not used				
R25	47 k	Carbon Film	1/4	5	D01939
R26	100 k	Carbon Film	1/4	5	D01944
R27	10 k	Carbon Film	1/4	5	D01930
R28	10 k	Carbon Film	1/4	5	D01930
R29	100 k	Carbon Film	1/4	5	D01944
R30	10 k	Carbon Film	1/4	5	D01930
R31	10 k	Carbon Film	1/4	5	D01930
R32	22 k	Carbon Film	1/4	5	D01934
R33	100 k	Carbon Film	1/4	5	D01944
R34	470	Carbon Film	1/4	5	D01913
R35	100 k	Carbon Film	1/4	5	D01944
R36	100 k	Carbon Film	1/4	5	D01944
RML1	10 k	SIL Network	1.2	2	938367
RML2	10 k	SIL Network	1.2	2	938367
RML3	100 k	SIL Network	1	2	D01859

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
<u>Capacitors (F)</u>					
C1	1 u	Tubular Tantalum	25	10	932038
C2	1 u	Tubular Tantalum	25	10	932038
C3	1 u	Tubular Tantalum	25	10	932038
C4	1 u	Tubular Tantalum	35	10	932034
C5	1 u	Tubular Tantalum	35	10	932034
C6	1 u	Tubular Tantalum	35	10	932034
C7	47 u	Tubular Tantalum	6	10	D01846
C8	15 u	Tubular Tantalum	6	10	D01845
C9	0u47	Ceramic Monolithic			D01842
C10	0u47	Ceramic Monolithic			D01842
C11	15 u	Tubular Tantalum	6	10	D01845
C12	0u47	Ceramic Monolithic			D01842
C13	0u47	Ceramic Monolithic			D01842
C14	15 u	Tubular Tantalum	6	10	D01845
C15	15 u	Tubular Tantalum	6	10	D01845

Diodes

D1	1N4149	923222
D2	1N4149	923222
D3	1N4149	923222
D4	1N4149	923222
D5	1N4149	923222
D6	Light-emitting	927620

Transistors

TR1	BC108	915460
TR2	BC178B	932182
TR3	BC178B	932182

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
<u>Integrated Circuits</u>					
ML1		Hex Inverters			D01812
ML2		Dual 1-of-4 Decoders			927051
ML3		Quad two-input NAND Gates			935453
ML4		Dual 4-bit Latches			D01818
ML5		Dual 4-bit Latches			D01818
ML6		Dual J-K Bistables			D01829
ML7		UART			D01827
ML8		Microprocessor			D02143
ML9		1 k x 4 RAM			D01826
ML10		1 k x 4 RAM			D01826
ML11		1 k x 4 RAM			D01826
ML12		1 k x 4 RAM			D01826
ML13		1 k x 4 RAM			D01826
ML14		Dual 4-bit Latches			D01818
ML15		Triplex Three-input AND Gates			927158
ML16		1 k x 4 RAM			D01826
ML17		1 k x 4 RAM			D01826
ML18		1 k x 4 RAM			D01826
ML19		1 k x 4 RAM			D01826
ML20		1 k x 4 RAM			D01826
ML21		A/D Converter			D01800
ML22		Triple Three-input OR Gates			927159
ML23		Dual D-type Bistables			D01805
ML24		Hex D-type Bistables			D01820
ML25		Dual 1-of-4 Decoders			927051
ML26		CMOS 14-Stage Ripple Carry Binary Counter/divider			930875
ML27		Hex D-type Bistables			D01820
ML28		Hex Strobed Buffer/inverters			D01817
ML29		Dual D-type Bistables			D01805
ML30		Programmable Op Amp			D02514
ML31		Triple Three-input NAND Gates			935452
ML32		Quad Two-input OR Gates			928640
ML33		Hex Inverters			D01812
ML34		Dual Complementary Pair plus Inverters			D01803
ML35		Quad Two-input NAND Gates			935453
ML36		Triple 2-channel Multiplexer/demultiplexers			930864
ML37		Programmable Bit-rate Generator			D01824
ML38		Quad 2-to-1 Data Selectors			D01823
ROM A&C		8 k byte ROM			461146
ROM B		1 k byte ROM			461145

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
<u>Miscellaneous</u>					
		Memory Battery Pack			452759
		Battery Insulator			452597
		DIL 24-way Connector			933813
		DIL 40-way Connector			933814
		Avlug			914054

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
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POWER BOARD ASSEMBLY (452610)

Resistors (ohms)

R1	15 k	Carbon Film	1/2	5	D01932
R2	15 k	Carbon Film	1/2	5	D01932
R3	1	Carbon Film	1/3	5	923887
R4	1	Carbon Film	1/3	5	923887
R5	470 k	Carbon Film	1/2	5	D01955
R6	1 k	Carbon Film	1/2	5	D01918
R7	1 k	Carbon Film	1/2	5	D01918
R8	560	Carbon Film	1/2	5	D01914
R9	560	Carbon Film	1/2	5	D01914
R10	100	Carbon Film	1/2	5	D01905
R11	27 k	Carbon Film	1/2	5	D01935
R12	10 k	Carbon Film	1/2	5	D01930
R13	22 k	Carbon Film	1/2	5	D01934
R14	22 k	Carbon Film	1/2	5	D01934
R15	470	Carbon Film	1/2	5	D01913
R16	56k2	Metal Film	1/2	0.5	D01852
R17	56k2	Metal Film	1/2	0.5	D01852
R18	82 k	Carbon Film	1/2	5	D01943
R19	10 k	Metal Film	1/2	0.5	D01850
R20	10 k	Carbon Film	1/2	5	D01930
R21	10 k	Metal Film	1/2	0.5	D01850
R22	2k7	Carbon Film	1/2	5	D01923
R23	100 k	Carbon Film	1/2	5	D01944
R24	220 k	Carbon Film	1/2	5	D01948
R25	2k7	Carbon Film	1/2	5	D01923
R26	4M7	Carbon Film	1/3	5	D01856
R27	6k8	Carbon Film	1/2	5	D01928
R28	6k8	Carbon Film	1/2	5	D01928
R29	1k2	Carbon Film	1/2	5	D01919
R30	22 k	Carbon Film	1/2	5	D01934
R31	39	Carbon Film	1/2	5	D01900
R32	22 k	Carbon Film	1/2	5	D01934
R33	22 k	Carbon Film	1/2	5	D01934
R34	39	Carbon Film	1/2	5	D01900
R35	100 k	Carbon Film	1/2	5	D01944
R36	220 k	Carbon Film	1/2	5	D01948
R37	1k2	Carbon Film	1/2	5	D01919
R38	100 k	Carbon Film	1/2	5	D01944
R39	6k8	Carbon Film	1/2	5	D01928
R40	6k8	Carbon Film	1/2	5	D01928

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R41	100 k	Carbon Film	1/4	5	D01944
R42	39	Carbon Film	1/4	5	D01900
R43	39	Carbon Film	1/4	5	D01900
R44	12 k	Carbon Film	1/4	5	D01931
R45	10 k	Variable		20	920312
R46	47	Carbon Film	1/4	5	D01939
R47	10 k	Carbon Film	1/4	5	D01850
R48	1 M	Carbon Film	1/4	5	D01959
R49	1 M	Carbon Film	1/4	5	D01959
R50	4k7	Carbon Film	1/4	5	D01926
R51	1 M	Carbon Film	1/4	5	D01959
R52	47k	Carbon Film	1/4	5	D01939
R53	220	Carbon Film	1/4	5	D01909
R54	220	Carbon Film	1/4	5	D01909
R55	1 M	Carbon Film	1/4	5	D01959
R56	4M7	Carbon Film	1/3	5	D01856

Capacitors (F)

V

C1	Not used				
C2	Not used				
C3	Not used				
C4	0u47	Ceramic Monolithic			D01842
C5	0u47	Ceramic Monolithic			D01842
C6	0u47	Ceramic Monolithic			D01842
C7	0u47	Ceramic Monolithic			D01842
C8	0u47	Ceramic Monolithic			D01842
C9	10 n	Ceramic Monolithic	100	20	932021
C10	10 n	Ceramic Monolithic	100	20	932021
C11	10 n	Ceramic Monolithic	100	20	932021
C12	10 n	Ceramic Monolithic	100	20	932021
C13	10 n	Ceramic Monolithic	100	20	932021
C14	10 n	Ceramic Monolithic	100	20	932021
C15	10 n	Ceramic Monolithic	100	20	932021
C16	10 n	Ceramic Monolithic	100	20	932021
C17	3u3	Tubular Tantalum	35	10	D01843
C18	1 u	Tubular Tantlaum	25	10	932038
C19	6u8	Tubular Tantalum	4	10	D01844
C20	47 u	Tubular Tantalum	6	10	D01846

Cct. Ref.	Value	Description	Rate	Tol %	Racial Part Number
C21	10 u	Tubular Tantalum	20	10	932042
C22	Not used				
C23	150 u	Electrolytic	16	-10 +50	921531
C24	1 n	Ceramic Monolithic	100	10	935865
C25	3u3	Tubular Tantalum	35	10	D01843
C26	1 u	Tubular Tantalum	25	10	932038
C27	1 u	Electrolytic	100	-10 +25	D02162
C28	10 n	Ceramic Monolithic	100	20	932021
C29	10 n	Ceramic Monolithic	100	20	932021
C30	10 n	Ceramic Monolithic	100	20	932021
C31	10 n	Ceramic Monolithic	100	20	932021
C32	0u47	Ceramic Monolithic			D01842
C33	0u47	Ceramic Monolithic			D01842
C34	10 n	Ceramic Monolithic	100	20	932021
C35	10 n	Ceramic Monolithic	100	20	932021
C36	0u47	Ceramic Monolithic			D01842
C37	Not used				
C38	Not used				
C39	15 u	Tubular Tantalum	6	10	D01845
C40	15 u	Tubular Tantalum	6	10	D01845
C41	Not used				
C42	0u47	Ceramic Monolithic			D01842
C43	0u47	Ceramic Monolithic			D01842
C44	10 n	Ceramic Monolithic	100	20	932021
C45	10 n	Ceramic Monolithic	100	20	932021

Inductors (H)

L1	100 u	Choke	D02153
L2	100 u	Choke	D02153
L3	100 u	Choke	D02153
L4	100 u	Choke	D02153
L5	0u22	Choke	D01862
L6	0u22	Choke	D01862
L7	0u22	Choke	D01862
L8	100 u	Choke	D02153
L9	100 u	Choke	D02153
L10	100 u	Choke	D02153

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
L11	100 u	Choke			D02153
L12	100 u	Choke			D02153
L13	100 u	Choke			D02153
L14	100 u	Choke			D02153
L15	100 u	Choke			D02153
L16	0u47	Choke			D01863
L17	0u47	Choke			D01863
L18	100 u	Choke			D02153
L19	1 u	Choke			926500
L20	3u3	Choke			D02285
L21	3u3	Choke			D02285

Transformer

T1	Ferrite Cored	461144
----	---------------	--------

Diodes

D1	1N4002	923564
D2	1N4149	923222
D3	1N4149	923222
D4	1N4149	923222
D5	1N4149	923222
D6	Zener BZX 85-C33V	D01839
D7	1N4149	923222
D8	1N4149	923222
D9	Zener BZX 83-B9V1	D01837
D10	1N4149	923222
D11	Light-emitting	927620
D12	1N4002	923564
D13	1N4002	923564
D14	1N4002	923564
D15	1N4002	923564
D16	1N4002	923564
D17	1N4149	923222
D18	1N4149	923222
D19	1N4149	923222
D20	1N4149	923222

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D21		1N4149			923222
D22		Zener BZY 88-C3V9			461157
D23		Zener MZ4687			D02512
D24		1N4149			923222
D25		1N4149			923222
D26		Zener BZY 88-C4V7			914067
D27		Zener BZX 85-C18V			D01838

Transistors

TR1	BC108	915460
TR2	BC178	932182
TR3	M116	D01832
TR4	BC178	932182
TR5	BFY51	908753
TR6	BFY51	908753
TR7	BC177	D01833
TR8	BC108	915460
TR9	BC178	932182
TR10	Not used	
TR11	BC178	932182
TR12	BC108	915460
TR13	BC178	932182
TR14	BC108	915460
TR15	BC108	915460
TR16	BC178	932182
TR17	BC178	932182
TR18	BC108	915460
TR19	BC108	915460
TR20	BC178	932182
TR21	BC178	932182
TR22	BC108C	D01835
TR23	Not used	
TR24	BC108C	D01835
TR25	BC108	915460

Cct. Ref.	Value	Description	Rat	Tol %	Racial Part Number
<u>Integrated Circuits</u>					
ML1		Dual Op Amps			D02697
ML2		Dual Op Amps			D01986
ML3		Hex Schmitt Triggers			D01191
<u>Miscellaneous</u>					
RLA		Reed Relay			D01864
FS1		2 amp Fuse			D02155
		Transipad			929728
		Transipad (larger)			D02165
		Avlug			914054

Cct. Ref.	Value	Description	Rate	Tol %	Racial Part Number
--------------	-------	-------------	------	----------	-----------------------

HF RADIO SOCKET ASSEMBLY, SKD (452705)

Socket, with 7 socket-contacts D01873

Capacitors (F)			V		
C1	10 n	Ceramic Monolithic	100	20	932021
C2	0u47	Ceramic Monolithic			D01842
C3	33 n	Ceramic Monolithic	100	-20 +80	D02284
C4	10 n	Ceramic Monolithic	100	20	932021
C5	10 n	Ceramic Monolithic	100	20	932021
C6	10 n	Ceramic Monolithic	100	20	932021

SATELLITE RADIO SOCKET ASSEMBLY, SKC (452704)

Socket, with 7 socket-contacts D01873

Capacitors (F)			V		
C7	10 n	Ceramic Monolithic	100	20	932021
C8	0u47	Ceramic Monolithic			D01842
C9	0u47	Ceramic Monolithic			D01842
C10	10 n	Ceramic Monolithic	100	20	932021
C11	10 n	Ceramic Monolithic	100	20	932021
C12	10 n	Ceramic Monolithic	100	20	932021

PRINTER SOCKET ASSEMBLY, SKB (452703)

Socket, with 7 socket-contacts D01870

Capacitors (F)			V		
C13	0u47	Ceramic Monolithic			D01842
C14	0u47	Ceramic Monolithic			D01842
C15	10 n	Ceramic Monolithic	100	20	932021
C16	10 n	Ceramic Monolithic	100	20	932021
C17	10 n	Ceramic Monolithic	100	20	932021
C18	10 n	Ceramic Monolithic	100	20	932021

UNUSED (REMOTE KEYBOARD) SOCKET ASSEMBLY SKA (452702)

Socket, with 7 socket-contacts 929912

Capacitors (F)			V		
C19	10 n	Ceramic Monolithic	100	20	932021
C20	10 n	Ceramic Monolithic	100	20	932021
C21	10 n	Ceramic Monolithic	100	20	932021
C22	0u47	Ceramic Monolithic			D01842
C23	10 n	Ceramic Monolithic	100	20	932021
C24	10 n	Ceramic Monolithic	100	20	932021

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
--------------	-------	-------------	-----	----------	----------------------

ITEMS ON MAIN ASSEMBLY

	10 nF	Polarising Screen	452728
		Clip-on Holder for Polarising Screen	452719/1&2
		Screw (M4x6) for Sealing the Unit	926311
		Sealing Washer	451240
		Weather Gasket (for Centre Section)	452652/1
		Weather Gasket for Battery Compartment	452652/2
		Capacitor, Ceramic, 100 V, 20 % (between Fuse Board and Top Casting)	932021
		Desiccator Sachet	D02584

PLUGS THAT CONNECT TO REAR OF UNIT

For SKD (HF Radio)	D01873
For SKC (Satellite Radio)	D01873
For SKB (Printer)	D01872
For SKA (Not used)	D01874
1m of 6-core screened cable (for printer)	926670
2m of 12-core screened cable (for radio or battery charger)	926671

RECEIVING A MESSAGE

10. Messages are received as either Data In, via connector pin L6, or as Tone In, via connector pin L4 and the modem (Paragraph 30). The Sat input, via connector pin L7, determines whether direct data input or input via the modem is used: Sat high switches Data In through switch ML11a, Sat Low switches the modem demodulator output through. Sat also goes to the EFI (pin 24) input to the processor, ML32, and the bit rate generator, ML9, where it sets conditions for either satellite or HF reception as applicable.

DETECTING A PREAMBLE

11. The received data is written into RAM ML18. The RAM is, in effect, eight separate 64-bit shift registers. Address lines from counter ML8 select one register at a time, at $8 \times$ bit rate, so a received data bit is written into each of the eight registers in turn. High-going edges of $8 \times$ Bit Rate Clock clock bistable ML4a; the resulting low Q output (pin 2) clocks counter ML8 (which addresses the next 64-bit shift register in the RAM); the high Q output (pin 1) is clocked into bistable ML4b by the next high-going edge of the 1.2288 MHz clock. The resulting high Q output (pin 13) from bistable ML4b does the following:
- (1) Applies a high signal to the input of the first stage of the correlation clock counter, 64-bit shift register ML23d, and resets the associated bistables, ML3a, ML3b.
 - (2) Inhibits clock pulses via NOR gate ML5a.
 - (3) Resets bistable ML4a.
12. The low Q output (pin 12) from bistable ML4b goes to the WR (pin 15) input of RAM ML18 where it causes the current state of the received data line to be written into the currently-addressed shift register in the RAM.
13. The next 1.2288 MHz pulse clocks bistable ML4b making its Q output low; the RAM write period is ended and the inhibit is removed from NOR gate ML5a. 1.2288 MHz pulses via the NOR gate causes counter ML19 to scan through the selected 64-bit shift register in the RAM, thus the contents of the register are read out serially via pin 8.

Correlation Counters

14. The data output from the RAM goes to exclusive-OR gates ML21a, ML21b. The other input to ML21b is the Selcall reference from ML23c, which is being clocked around at the same rate as the RAM data (by 1.2288 MHz pulses). Counter ML27, which is also being clocked at 1.2288 MHz, is enabled by the output from the exclusive-OR gate; it therefore counts the number of correlations between the 64-bit sample from the RAM and the 64 bits of Selcall data. Likewise counter ML28 counts the correlations between the RAM data and the Allcall reference from ML23b.

Correlation Clock Counter

15. When 64 comparisons have been made (i.e. after 64 1.2288 MHz pulses) an Interrupt Signal is sent to the processor, as follows. At the end of the comparison period, the high bit that was loaded into the correlation clock counter (paragraph 11(1)), clocked through the counter by 1.2288 MHz pulses, reaches the Q63 output (pin 2), and is clocked through the Q output (pin 1) of bistable ML3a and then through the Q output (pin 13) of bistable ML3b. This inhibits clock pulses via NOR gate ML5a, and goes via the interrupt gates to initiate a processor interrupt.

Interrupt Gates

16. While the unit is looking for a preamble, the Message Detected signal to inverter ML17e is low; the inverter's output to AND gate ML6d is high, so the high Q output from ML3 b (Paragraph 15) causes a high-going signal to clock bistable ML10a. The input to pin 5 of the bistable is, during a receive operation, high, so a low Interrupt signal is output from the \bar{Q} output, pin 2. (When the processor performs an interrupt cycle, its SC0 and SC1 outputs both go high; this applies a reset signal to pin 4 of bistable ML10a (via ML17b, ML21c and ML5b), to remove the Interrupt signal).
17. In its Interrupt routine the processor examines the correlator counts. The processor performs an Input 4 instruction (N2 high). Control line decoder ML31 enables the outputs of buffer ML35 (via ML26f) so that the data read onto the data bus is the count value from the Selcall counter ML27. The counter contains the number of correct correlations with the Selcall preamble. The processor then performs an Input 1 instruction (NO high) which reads the data through buffer ML36 from the Allcall counter ML28. The counter contains the number of correct correlations with the Allcall preamble.
18. The processor can thus determine whether or not a preamble has arrived: if the count is 54 (from a possible 64), or an inverse correlation of 10 or less, the processor recognises that a preamble has arrived.
19. At the next 8 x Bit Rate Clock high-going transition, the sampling sequence (Paragraph 11) starts again. The state of the received data line is written into the next 64-bit shift register in the RAM, then the contents of that register are checked against the Selcall and Allcall references. This sequence occurs eight times for each received data bit length, so, if a preamble arrives under ideal conditions, eight successful correlations occur. However, two or more successful correlations are sufficient. When a non-correlation occurs following two or more correlations, the processor switches from the preamble-search cycle to receive the message.

CLOCK RECOVERY

20. In order to clock the incoming data into the received data register at the optimum time (at the centre of each data bit), the processor carries out a clock-recovery operation. The processor first centres the clock on the data: knowing the number of successful preamble correlations that occurred, the processor calculates when the centre of the next bit is due (i.e. one bit period after the middle of the successful correlations).
21. The processor outputs the calculated counter-preset value to bistables ML15 using an Output 6 instruction (N1 and N2 high). The processor then presets preamble counter ML16 to the value latched through the bistables, using an Output 5 instruction (N2 and N0 high). The processor then resets the value in ML15 to eight. The counter counts down on every 8 x Bit Rate clock pulses, reaches zero, then presets to eight and counts down again. Each time ML16 is set to a count of eight its Q3 output (pin 15) goes high, which, inverted by inverter ML17d, is used as Bit Rate Clock to clock the data into the received data register, ML33. Thus the count initially set into ML16 by the processor determines the time at which an incoming data bit is clocked into register ML33.
22. To keep the Bit Rate Clock high-going transitions at the mid-points of the data bits, the processor reads the state of the clock on the last positive data transition that occurs before the received data is read-in from the received data register ML33 (Paragraph 24). Positive-going transitions of the data signal clock the state of the Bit Rate Clock signal through bistable ML10b; when data is output from ML33, switch ML11b switches the \bar{Q} output (pin 12) from the bistable onto the bit 7 line of the data bus.
23. If the data is being clocked dead-centre, leading edges of the data bits coincide with negative-going transitions of the clock; if the clock is early, it is already low, if it is late it is still high. Therefore, a high \bar{Q} output from the bistable indicates an early clock, low indicates a late clock. The processor counts early/late clocks and when one exceeds the other by 128, it makes an adjustment by setting a new number into ML16 (for one bit period): it reduces the starting count of the counters cycle by one (to seven) to advance the Bit Rate Clock signal, or increases the starting count by one (to nine) to retard the Bit Rate Clock signal. After one bit period, the counter is set back to its previous starting position (eight).

ACCEPTING MESSAGE DATA

24. Received data goes to pin 2 of 8-stage shift-and-store register ML33 where it is clocked-in by high-going edges of Receive Clock at pin 3. Each time the Q output (pin 12) of counter ML16 goes high (i.e. at data rate), the resulting output from OR gate ML7d causes bistable ML10a to send a low Interrupt signal to the processor, and strobes the data in the ML33 input register into its output register. When six interrupts have occurred, the processor performs an Input 5 instruction (N2 and NO high) to read-in the contents of ML33: the ML33 enable input (pin 15) is set high by control line decoder ML31, and the contents of the ML33 output register are output onto the data bus.

SENDING DATA TO MAIN PROCESSOR

25. When the Data I/P Enable signal, which enters the board via connector pin M8 and goes to the EFZ (pin 23) input of the processor, is high, the processor can send data out from the board via the parallel data bus. The processor performs an Output 7 instruction: the output from pin 4 of control line decoder ML30 leaves the board as I/O Data Clock via connector pin M4, to strobe the data from the bus (into a recipient device).

END OF MESSAGE

26. While data is being received, the high Message Detected signal to switch ML13c switches through the Postamble reference, stored in register ML23a, to the correlation circuit. The detection procedure is as for Selcall and Allcall preamble detection (Paragraph 11). When correlation occurs, the processor sends a block count and an End-of-Message character to the main processor, and resets the Message Detected signal low. The processor examines the correlator count at bit rate (on every Interrupt) when looking for a Postamble. Only one correlation is required.

LOW/HIGH-SPEED SATELLITE PREAMBLES

27. In satellite data operation, the processor looks for a preamble at 300 baud; it sets its Q output, from pin 4, high, which sets the S3 input (pin 11) of the bit rate generator. When a 300 baud preamble has been recognised, the processor resets its Q output low and looks for a 1200 baud preamble. If a 1200 baud preamble arrives, the subsequent operation remains at 1200 baud; if no 1200 baud preamble arrives (within the required time), the processor resets the rate to 300 baud to receive a 300 baud message.

SENDING A MESSAGE

28. Data for transmission is transferred to the RAM from the Main Processor by DMA (Direct Memory Access). When a data character is ready for transfer into the RAM the DMA In line, which enters the board via connector pin M5, is set low; this requests the processor to execute a DMA In cycle as its next cycle. During the DMA cycle the processor's SCO output is set low and its SC1 output high; these signals are gated through inverter ML17b and NAND gate ML22d to provide a low I/O Data Dis signal, which leaves the board via connector pin M2. I/O Data Dis low is a request for the data character to be placed on the data bus.
29. Data is transferred in blocks of eight characters, which are written directly into the RAM. When sixteen characters have been stored, the processor makes the Q5 (pin 12) output from bistables ML34 low; this low output leaves the board via connector pin M7, to inhibit DMA transfer. The processor then makes the Q4 (pin 10) and Q3 (pin 7) outputs from ML34 high: the Q4 output goes via NAND gate ML22c and NOR gate ML5c to leave the board as PTT En via connector pin L8; the Q3 output, Tx Enable, inhibits Interrupt (from bistable ML10a pin 2) and enables the transmit circuits (low signal at pin 6 of bistable ML20a and pin 19 of modulator ML2).
30. The processor then outputs the message data using an Output 2 instruction (N1 high). Message data is output one bit at a time (on the data bus bit 0 line), at the low-going edges of the Bit Rate Clock signal (sensed by the processor using its EF3 input). The message bits are latched into bistable ML20a, then clocked into bistable ML20b at the high-going edges of Bit Rate Clock. If the Sat input is high, the Q output of ML20b is switched through switch ML11c and exclusive-OR gate ML21d to leave the board as Data Out via connector pin L5 (inverted if link LK1 is present). If Sat is low, the data goes via modulator ML2 (Paragraph 32) and leaves the board as Tone Out via connector pin L3.
31. When the processor has sent eight characters, it sets Data Req high to request another block of eight characters. When the End of Message character has been sent, the processor returns the board to the receive state: Tx Enable and PTT En low, Data Req high.

MODEM

Modulation

32. The modulator, ML2, accepts digital Data via pin 14 and Data via pin 18 when Tx Enable, at pin 19, is low. The 1.2288 MHz clock input (pin 20) clocks a pair of binary rate multipliers which produce two frequency clock signals; one frequency clock signal is selected at a time, according to the state of the data input. The selected frequency clock signal is divided down to drive a sinewave generator, and the resulting output from the modulator is 1303 Hz for a high data bit, 2100 Hz for a low data bit. Two outputs, one inverted, are produced for driving balanced systems.
33. The outputs can be 25 mV (resistors R13 and R14 are 270 ohms) or 2.5 mV (resistors R13 and R14 are 2k7 ohms).

Demodulator

34. The FSK input from an HF radio receiver enters the board via the Tone In line, connector pin L4; it is converted to digital data by a demodulator consisting of four hybrid circuits: automatic gain control, ML14; space filter, ML1; mark filter, ML24; detector, ML25.
35. The Tone In signal is a.c. coupled into ML14 via capacitor C1; it is amplified to a level suitable for the mark and space filters, ML24, ML1. The band-pass filters are centred on the two FSK frequencies in use: the mark filter at 1303 Hz, the space filter at 2100 Hz; both filters have a 350 Hz bandwidth. The filter outputs go to the detector, ML25; also, parts of the outputs are fed back to the automatic gain control hybrid, ML14, to keep the magnitude of the signal level to the detector approximately constant.
36. The detector rectifies the inputs from the filters, providing two outputs of opposite polarity, then sums the rectified signals to produce an envelope which carries the basic data information. To allow for unequal variations in the two frequency levels, the detector uses a decision threshold that varies according to the level present for each frequency: this adaptive threshold is generated from the envelope (see Figure 5.3.3). The threshold and envelope signals are applied to a comparator and the resulting digital data signal is output as Rx Data from pin 19 of ML25.
37. If link LK2 is fitted, the Ad En input (pin 15) of ML25 is held low: a fixed comparison point is used instead of the adaptive threshold.

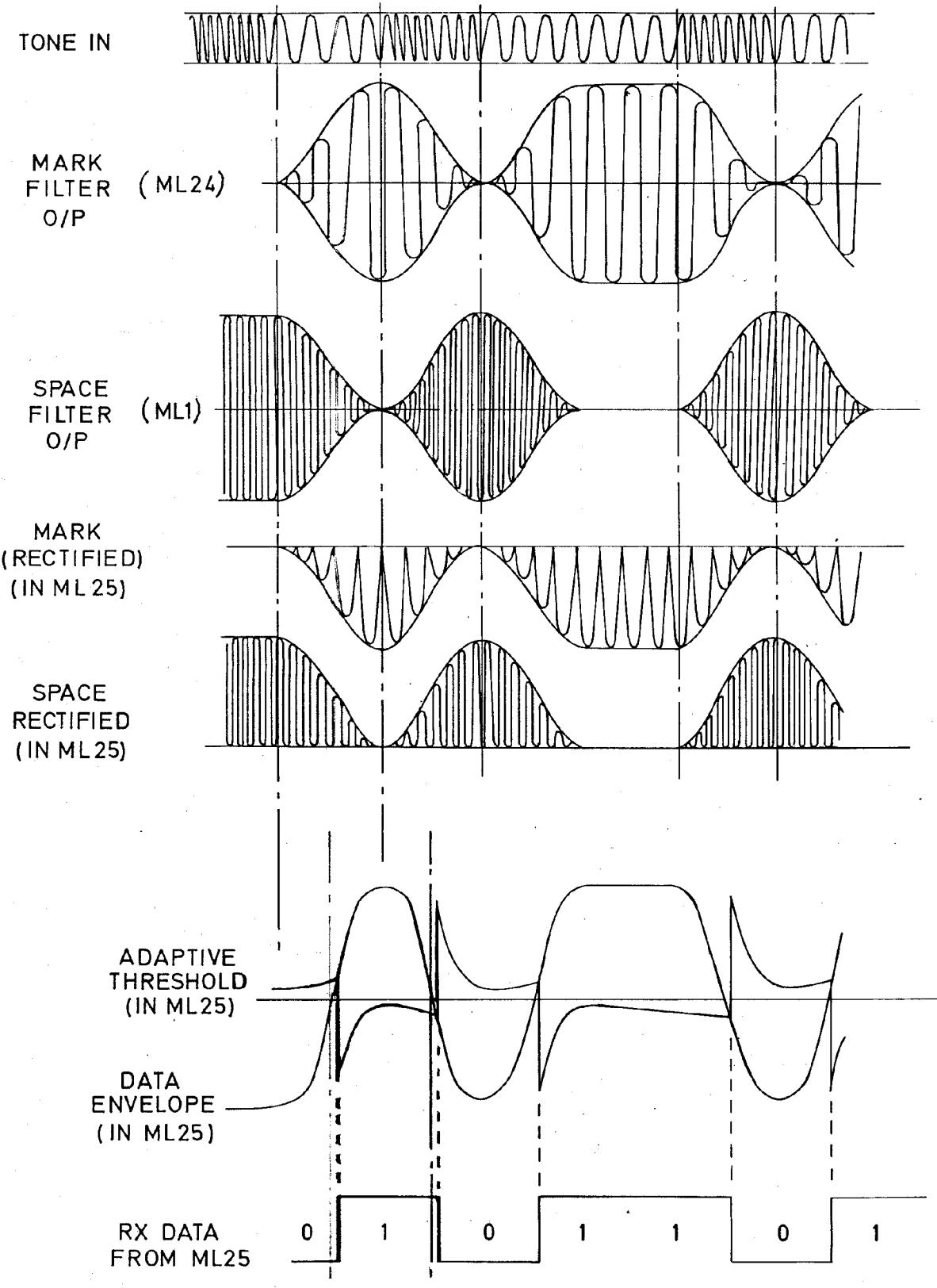


Fig.5.3.3

FSK Demodulation: Waveforms

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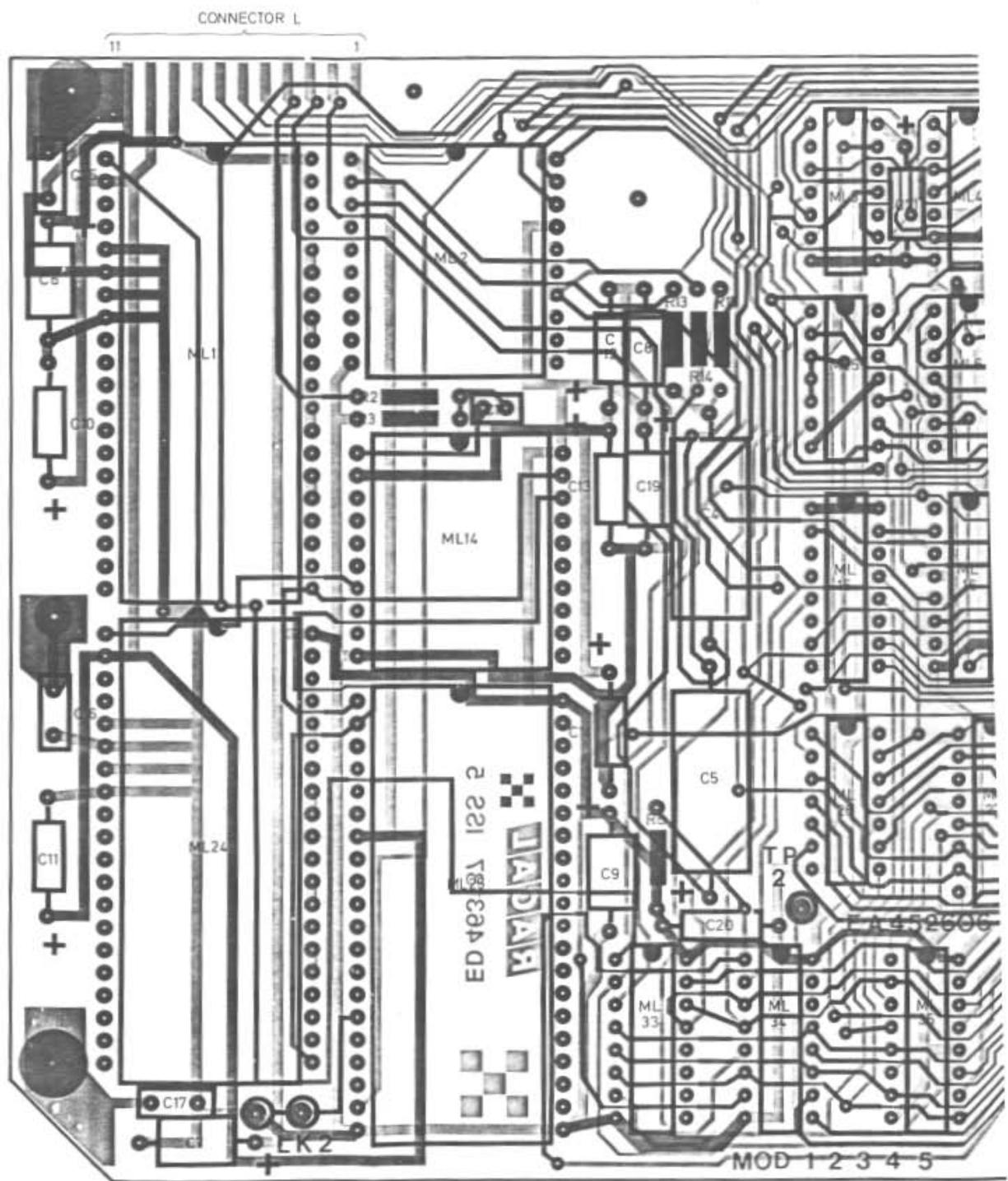
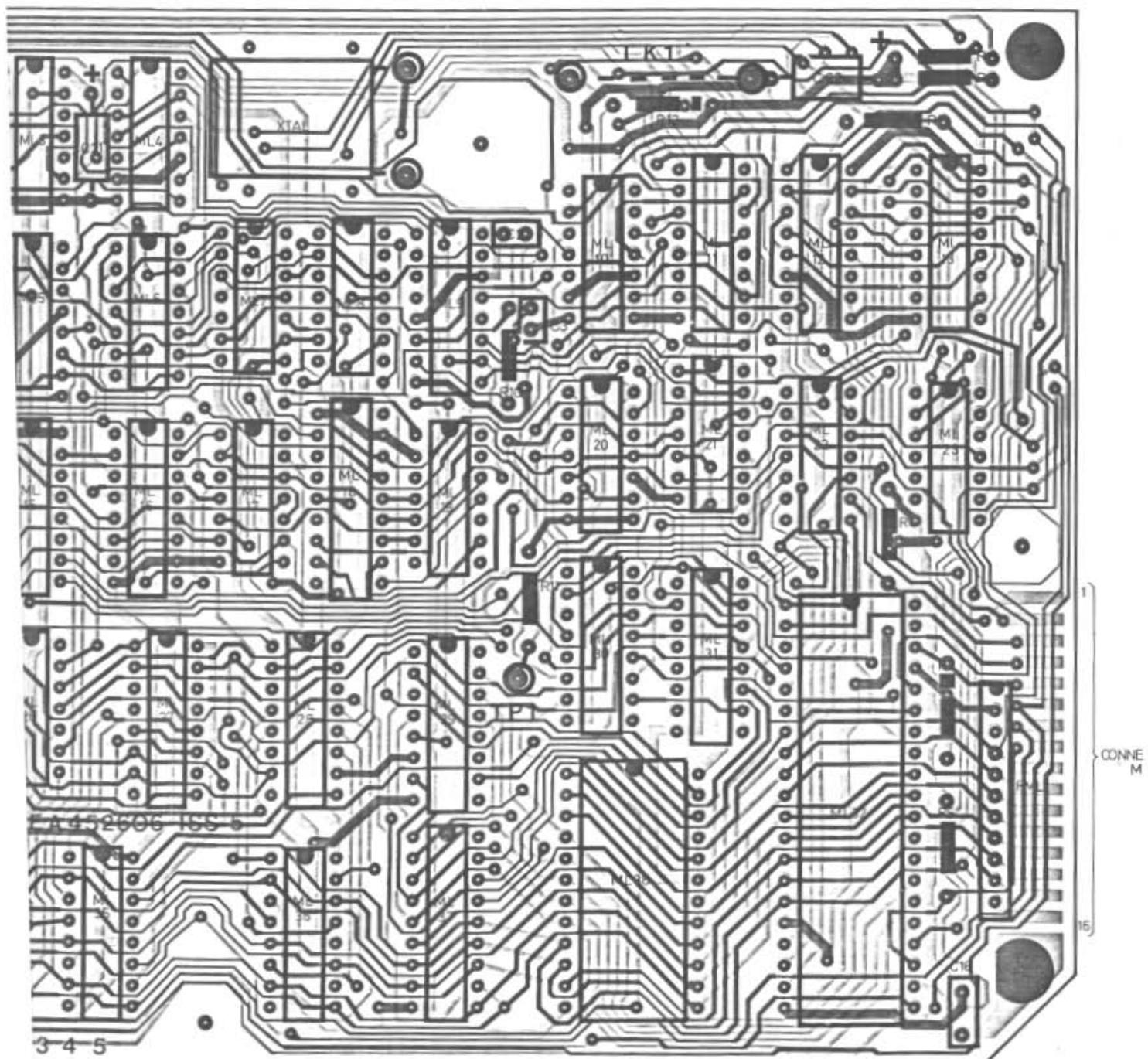


Fig.5.3.4 Sync I/O Board (452606): Layout



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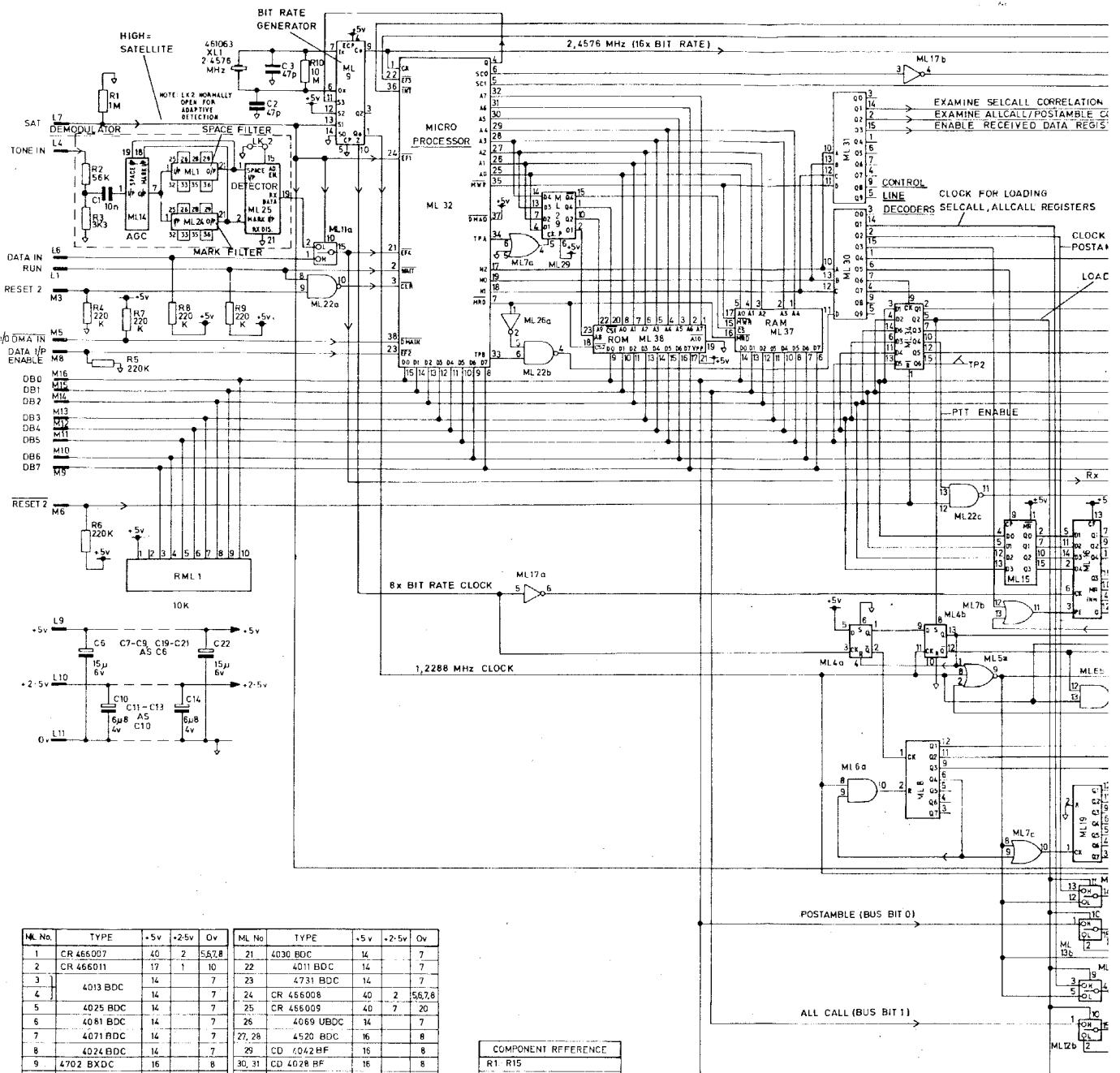
ISSUE 5/5/5, 1.81

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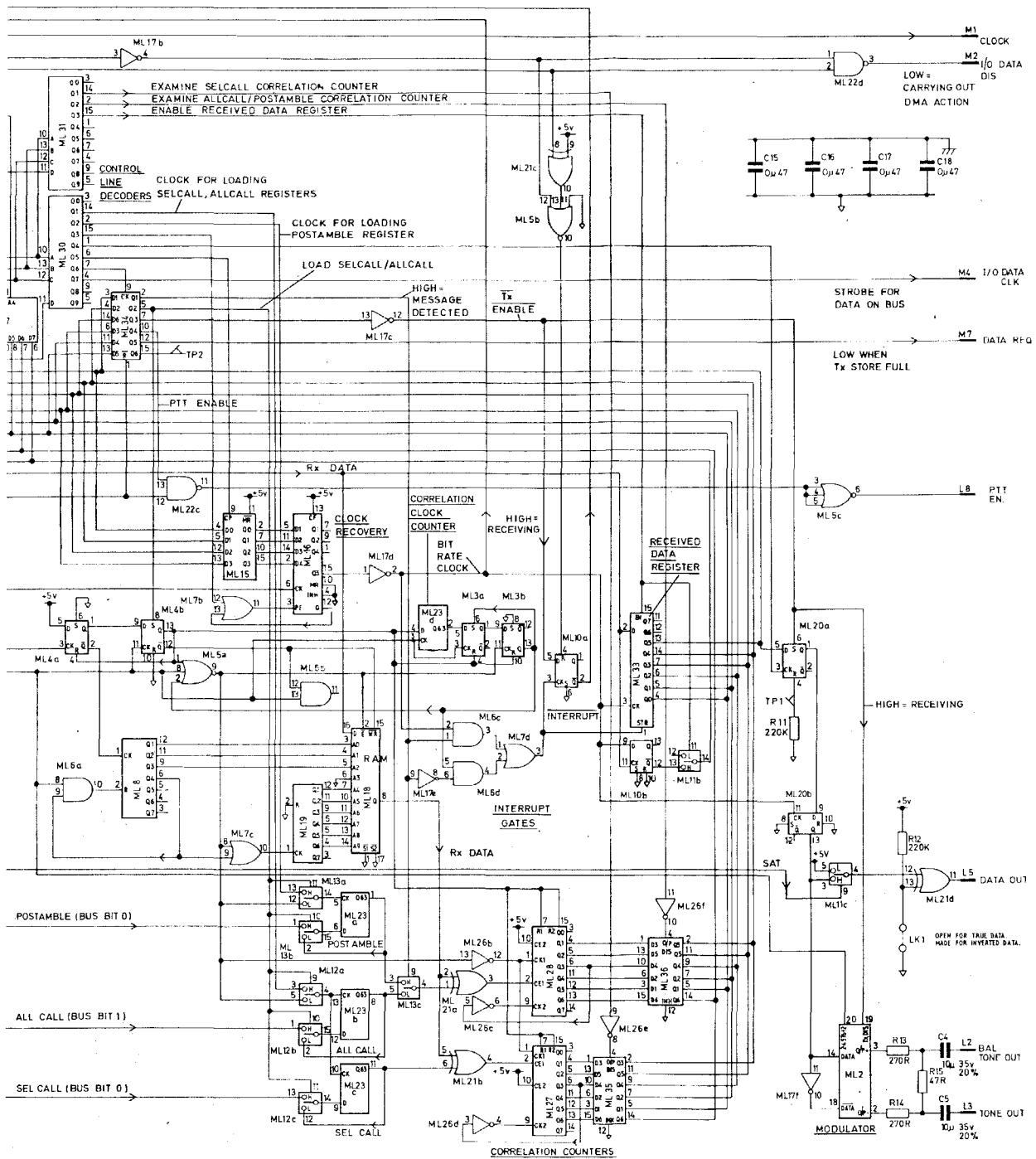
ISSUE 5/5/5, 1.81

1 2 3 4 5 6 7 8 9

ISSUE 5/5/5, 1.81



Synchronous I



Synchronous Input/Output Board (452606):Circuit

Fig.5.3.5

CHAPTER 4

MAIN PROCESSOR BOARD - 452607

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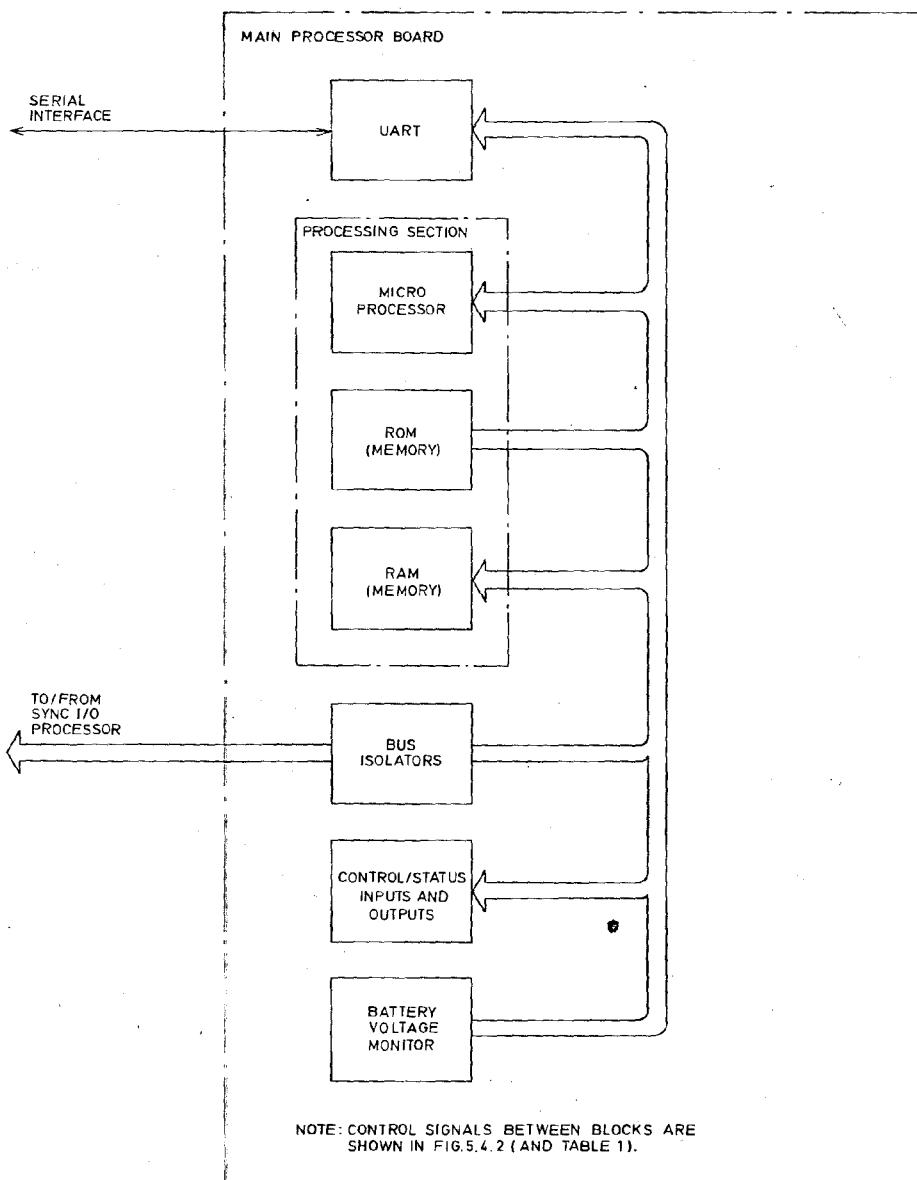


Fig.5.4.1

Main Processor Board:
Simplified Block Diagram

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CHAPTER 4

MAIN PROCESSOR BOARD - 452607

GENERAL

1. The Main Processor Board 452607 performs the main control functions in the unit. It contains the message stores, main program and working stores, and it performs all the message management and error protection/correction manipulation. The circuit is shown in Figure 5.4.4. The board contains the following functions:
 - (1) Microprocessor, which is the main processor in the unit.
 - (2) Main control program for the unit's activities (in ROM).
 - (3) User program providing facilities required by the particular system (e.g. additional prompts for the operator), (in ROM).
 - (4) Working storage for the processor during execution of routines, message storage, etc. (in RAM).
 - (5) Interface between the microprocessor and the Man/Machine Interface Board (via UART). The UART also interfaces with an external printer.
 - (6) Battery voltage and charge monitor.

THE PROCESSING SECTION

Brief Description

2. The microprocessor ML8 is the same as the processor described in Chapter 2, but with some additional control inputs and outputs used, as shown in Figure 5.4.2 and Table 1.
3. The processor's program is stored in ROMs A, B and C (Paragraph 4); its working store is RAMs ML9 to 13 and ML16 to 20.

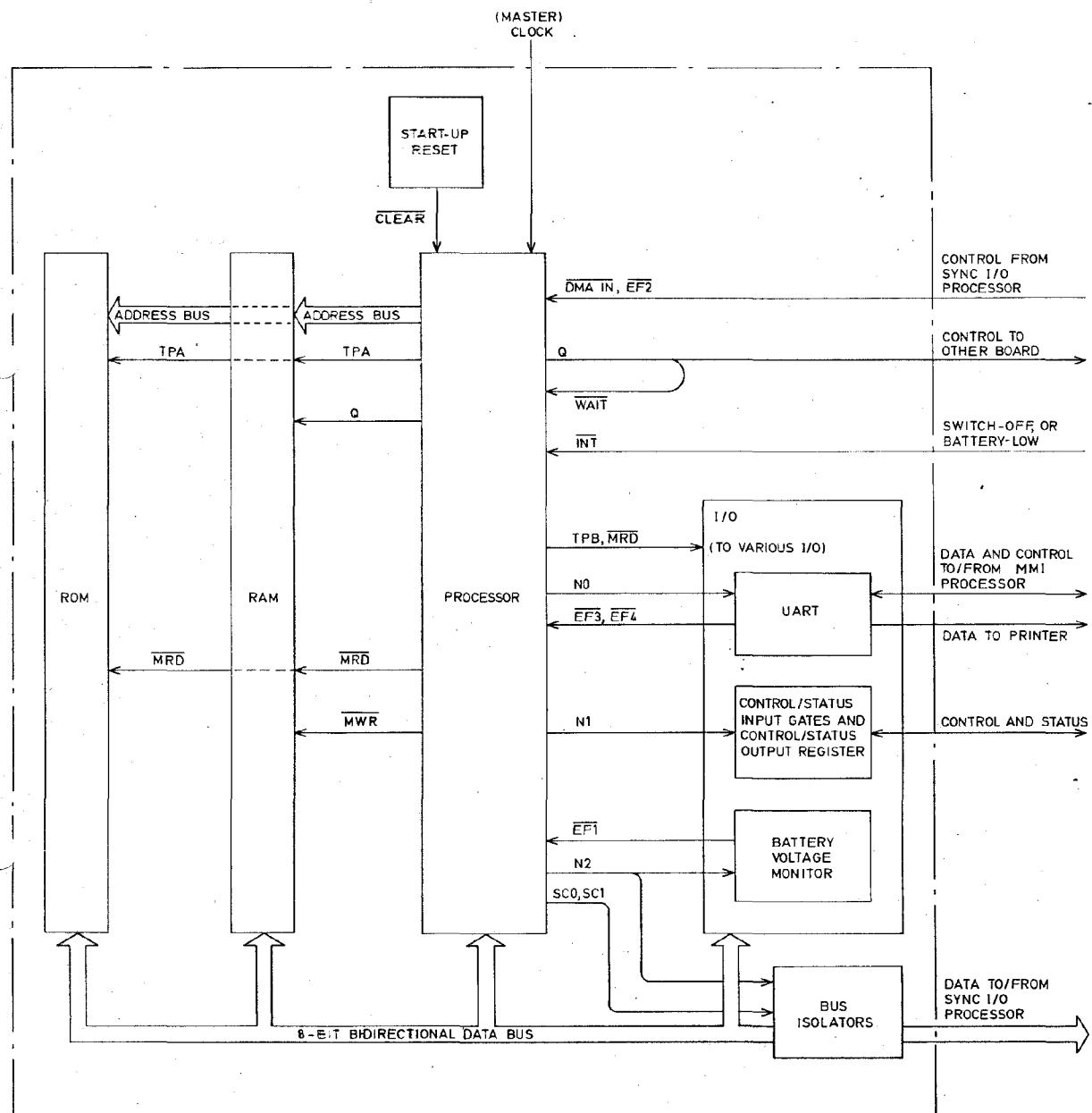


Fig.5.4.2

Simplified Block Diagram of the Processing Section as used on Main Processor Board

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TABLE 1 DIRECT COMMAND SIGNALS TO/FROM THE MICROPROCESSOR

Signal	Use	Description In Handbook								
<u>Inputs</u>										
EF1	Battery voltage check circuit has a sample ready.	Paragraph 49								
EF2	Data Req. Sync I/O processor ready for DMA transfer.	Paragraph 45								
EF3	UART has a received character in its buffer.	Paragraph 38								
EF4	UART ready to accept data for transmission.	Paragraph 39								
DMA In	I/O Data Ck. Requests a DMA transfer into the RAM.	Paragraph 43								
Int	Interrupts processor to inform it that battery voltage is very low, or a Req Off signal has been received (i.e. the OFF key has been pressed).	Paragraph 50								
<table border="1"> <tr> <th>Clear</th> <th>Wait</th> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>			Clear	Wait	0	1	1	0	1	1
Clear	Wait									
0	1									
1	0									
1	1									
	Resets processor to initial conditions.	Paragraph 16								
	Stops internal functioning of processor (Pause mode).	Paragraph 18								
	Normal functioning of processor (Run mode).	Paragraph 18								
<u>Outputs</u>										
<table border="1"> <tr> <th>SCO</th> <th>SC1</th> </tr> <tr> <td>0</td> <td>1</td> </tr> </table>			SCO	SC1	0	1				
SCO	SC1									
0	1									
	Carrying out DMA action.	Paragraph 44								
Q	Stops internal functioning of processor, inhibits writing into RAMs and turns the unit off.	Paragraphs 18 & 14								
NO	Processor reading data from UART; processor outputting to UART (to send data via serial interface)	Paragraph 38 Paragraph 39								
N1	Processor outputting status data to ML28; processor reading status data from ML27.	Paragraph 22 Paragraph 29								
N2	Processor outputting data to Sync I/O processor; processor reading battery voltage level from ML21.	Paragraph 45 Paragraph 49								

Program Store

4. The main program is stored in the 8k memory, ROM A. This contains the routines for Interleaving, De-interleaving, Error Detection and Correction, etc. The 1k memory, ROM B, stores the main housekeeping routine. The 2k EPROM (erasable programmable read-only memory), ROM C, if fitted, stores user programs, which can provide special prompts for the operator.

Store Addressing

5. The eight most-significant bits of the address (known as the high-order address) are latched through bistables ML24 by the low-going edge of TPA (inverted to high-going edge by inverter ML1b). The eight least-significant bits of the address (known as the low-order address) are used direct from the address bus. The address bits are decoded by decoders ML25a, ML2a, ML2b and associated gates to select a RAM or ROM (by making its CS input low), the remaining bits select the part of the RAM or ROM concerned with the data transfer. A list of addresses and the corresponding parts of the memory selected is given in Table 2.

TABLE 2 RAM AND ROM ADDRESSES

Address	RAM/ROM
0 to 19FF (0 to 8k)	ROM A
2000 to 23FF (8k to 9k)	ROM B
2800 to 29FF (10k to 12k)	ROM C
4000 to 43FF (16k to 17k)	ML9, ML16
4400 to 47FF (17k to 18k)	ML10, ML17
4800 to 4BFF (18k to 19k)	ML11, ML18
4C00 to 4FFF (19k to 20k)	ML12, ML19
5000 to 53FF (20k to 21k)	ML13, ML20

ROM Selection

6. ROM A is selected by a delayed MRD signal when the 8k and 16k address lines are low. The MRD signal, delayed by J-K bistables ML6a, ML6b (to allow the low-order address to stabilise on the address lines before the ROM is selected), the 8k address latched via ML24 pin 15, and the 16k address via bistable ML23b pin 13, make the output from OR gate ML22c low, thus selecting ROM A. The MRD signal delay is achieved by ML6a, ML6b as follows: the MRD signal from pin 7 of the processor goes low, it is

inverted by inverter ML1c and the next low-going Clock edge clocks it through J-K bistable ML6a, making the bistable's Q output from pin 15 high; the next low-going Clock edge clocks the ML6a output through J-K bistable ML6b, making the bistable's Q output from pin 10 low. (The bistables are reset when the processor's MRD output returns to high).

7. ROM B is selected by a delayed MRD signal when the 2k, 4k and 16k address lines are low and the 8k address line is high. The MRD signal inverted by ML1c then delayed by J-K bistable ML6a, the 8k address latched via ML24 pin 15, and the 16k address via bistable ML23b (from the Q output, pin 12, therefore inverted), are all high, so the output from NAND gate ML31c is low, thus enabling decoder ML2a. The decoder decodes the 2k address line from ML24 pin 10 (at its A input, pin 2) and the 4k address line from ML24 pin 12 (at its B input, pin 3); these are both low so the decoder's Q0 output from pin 4 is low, thus selecting ROM B.
8. ROM C is selected as the top half of ROM A if link LK8 is present; it is selected by addresses between 10k and 12k if link LK9 is present.
9. Link LK8 allows two 4k ROMs in the ROM A and ROM C positions to replace the normal 8k ROM A. Link 1 must in this case be present (to allow the A11 address line through to the ROM C position).
10. Link 9 allows the Q1 output from pin 5 of decoder ML2a to select ROM C. This output is low when the decoder is enabled (as in Paragraph 13), the 2k address line (via latch ML24 pin 10) is high and the 4k address line (via ML24 pin 12) is low.
11. The ROM outputs are buffered onto the data bus by ML4. The outputs from ML4 are enabled by a delayed MRD signal when the 16k address line is low (i.e. the processor is reading from an address below 16k). The delayed MRD signal from the Q output (pin 14) of J-K bistable ML6a, and the 16k address via bistable ML23b pin 13, both low, make the output from OR gate ML32d low; this goes via link LK5 (Memory Enable) to pins 3 and 15 of ML4, thus enabling the outputs.

Working Store

12. The working memory space is provided by ten 1k x 4 bit RAMs, ML10 to 13, ML16 to 20. The RAMs are addressed in pairs so that eight bits of data are written or read via the data bus at one time. A RAM is selected when its CS input (pin 8) is low, and data is written into the RAM, at the address defined by the ten address inputs, when WE (pin 10) is low. If WE is high, data at the defined address is read out.
13. Data is written into a RAM when the processor makes its MWR output (pin 35) low and the required RAM location is addressed, Paragraph 5). The low MWR signal makes the En (enable) input of decoder ML25b low. During normal operation the A input (pin 2) of the decoder (Q from the processor) is low and the B input (pin 3) (Reset 2) is high, so the Q2 output (pin 6) from the decoder is made low. This output goes to the WE inputs of all RAMs.
14. If the Q signal is high (unit turning-off) or Reset 2 is low (unit not yet running normally), the WE signal is inhibited, thus preventing spurious data from being written into RAMs during turn-on and turn-off.

START-UP RESET

15. When power is initially applied to the board, the Reset 1 signal, output via connector pin H3, and the Reset 2 signal, output via connector pin M6, are both low, thus providing start-up reset signals to the Main Processor Board and other boards. Reset 2, inverted by inverter ML1e, is used to reset the UART, ML7 and leaves the board as Reset 2 via connector pins M3 and H7.
16. The low signal to the CTr input (pin 3) of the microprocessor, and high (via NAND gate ML3b) signal to the Wait input (pin 2), reset the processor to its initial conditions.
17. As capacitor C1 charges through resistor R2, switch ML36a switches the +5 V rail to the Reset 1 line, thus terminating the low Reset 1 signal. This starts capacitor C2 charging through resistors R3 and R13. When the threshold of ML34a pin 6 is reached, ML34a and ML34b switch to make the Reset 2 line high. Resistor R18 supplies hysteresis to the ML34a, ML34b circuit to give a clean switch-over.
18. The processor is then in the Run mode, with CTr and Wait both high. When Wait goes low because of a high Q output from the processor (via NAND gate ML34b), the Pause mode, in which the processor remains inactive, is entered. This occurs as the unit is turned-off, to provide a clean stop to the processor's activities.

TIMING GENERATION

Clock Generator

19. The timing signals required by the board are converted from Clock, which enters the board via connector pin M1, by clock generator ML37. The outputs from pins 9 and 6 are at the same frequency as the input Clock signal; the former goes to the clock input (pin 1) of processor ML8 and to J-K bistable ML6a; the latter goes via inverter ML33e to leave the board as Master Clk at connector pin H5. The Q1 output from pin 2 of ML37 is Clock $\div 4$, used by the battery voltage monitor circuit; the Q2 output from pin 3 is Clock $\div 8$ which, after further division by counter ML26 to provide Clock $\div 256$, leaves the board as Inv Ck via connector pin J6 and (inverted by inverter ML33f) as Inv CK via connector pin J5.
20. The Z output from pin 10 of the clock generator provides the clock for transfers over the UART-controlled serial interface. The Z output varies according to the bit rate selected by the S0, S1, S2, S3 inputs (pins 14, 13, 12, 11 respectively). The inputs to S0, S1, S2, S3 are from switch ML38. When the input to pin 1 of the switch is low (for data transfer to/from the MMI processor, Paragraph 39), the A inputs via pins 2, 5, 11, 14 are switched through to the clock generator; the A inputs are set for 1800 baud (i.e. the Z output from the clock generator is 16 x 1800 because the UART requires a 16 x bit rate clock).

21. When the input to pin 1 of the switch is high, the B inputs via pins 3, 6, 10, 13 are switched through (to provide the clock for printer outputs, Paragraph 39). The B inputs are determined by links LK13, LK11, LK10, LK12 which connect their associated switch inputs to 0 V. The links required for various bit rates are shown in Table 3. Note that the clock rate (i.e. the Z output from the bit rate generator) is 16 x bit rate (as required by the UART).

TABLE 3 PRINTER-SPEED LINK SETTINGS

Link 13	Link 11	Link 10	Link 12	Bit Rate (baud)
✓	✓	✓	✓	Not used
✓	✓	✓		Not used
✓	✓		✓	50
✓	✓			75
✓		✓	✓	134.5
✓		✓		200
✓			✓	600
✓				2400
	✓	✓	✓	9600
	✓	✓		4800
	✓		✓	1800
	✓			1200
		✓	✓	2400
		✓		300
			✓	150
				110

CONTROL/STATUS INPUTS

22. Six control/status signals are input to the processor via the control/status input gates, inverting buffers ML28. The processor performs an Input 2 instruction which causes its N1 and ~~MRD~~ outputs to go high. These signals make the output from NAND gate ML35c low, thus removing the output-disable signal from the control/status input buffers.
23. Bit 0 indicates whether link LK4 is present. If the link is present, the processor adds half a second of phase reversals to the start of transmitted messages. If there is no link, the processor adds one second of phase reversals.
24. Bit 1 is high when an external power supply is connected, i.e. Charger, which enters the board via connector pin H10, is low.
25. Bit 2 is high when the battery voltage is low, i.e. Batt Low, which enters the board via connector pin H9, is low.
26. Bit 3 is low when a satellite/digital radio is connected, i.e. Sat, which enters the board via connector pin H8, is high.
27. Bit 4 is low when the UART has transmitted a character, i.e. when the UART's TRE output from pin 24, is high.
28. Bit 5 is high when a printer is connected, i.e. CTS (CTerminate To Send), which enters the board via connector pin H14, is low.

CONTROL/STATUS OUTPUTS

29. Five control/status bits are output by the processor via the control/status output register, bistables ML27. The processor performs an Output 2 instructions which causes its N1 output to go high while ~~MRD~~ is low. When TPB goes high, the output of AND gate ML15a goes high, thus clocking the data bus bits into the control/status output register.
30. Bit 0 is high when the processor is ready for a DMA transfer. It goes via the Q1 output (pin 2) of the bistables, and leaves the board as Data I/P En via connector pin M8 (Paragraph 43).
31. Bit 1 is high to initiate a battery voltage reading. It goes via the Q2 output (pin 5) of the bistables, to bistable ML29a (Paragraph 48).
32. Bit 2: Not used (Paragraph 42).
33. Bit 3 is high to connect the battery monitor line through to the A/D converter (Paragraph 48). It goes via the Q4 output (pin 10) of the bistables.
34. Bit 4 is low when the processor turns-on battery charging. It goes via the Q5 output (pin 12) of the bistables and leaves the board as Charge via connector pin H11.

35. Bit 5 is high when the serial output from the UART is for a printer; low when the UART is transferring data to/from the MMI processor (Paragraph 39). It goes via the Q6 output (pin 15) of the bistables.

SERIAL INTERFACE VIA UART

36. Serial data transfer to/from the board is performed with the UART (Universal Asynchronous Receiver/Transmitter) ML7. The timing signal for the UART is generated by the clock generator (Paragraph 20). It goes to the RRC (pin 17) and TRC (pin 40) inputs of the UART to time both receive and transmit operations, and it leaves the board as Data Clk via connector pin H2. UART operation is described in Chapter 2; operation on the Main Processor Board is described briefly in Paragraphs 37 to 42.

Receiving from the Serial Interface

37. Serial data enters the board as Kbd Data via connector pin J9 and goes via OR gate ML32a, NAND gate ML31a and inverter ML33c to the RRI input (pin 20) of the UART. If a remote keyboard is in use, Rem Kbd Detect, which enters the board via connector pin J8, is high, thus holding the output from the OR gate high (and inhibiting Kbd Data). The Rem Kbd Data signal, which enters the board via connector pin J2, is gated through ML31a to the UART.
38. When the UART has received a character, its DR output goes high; this signal goes to the EF3 input of the processor. In response the processor performs an Input 1 instruction during which the NO line goes high; both inputs to NAND gate ML3c are then high and the resulting low RRD signal to the UART causes it to output the data from its receive register.

Sending via the Serial Interface

39. The processor uses its EF4 input to sense whether the UART is ready to read data. EF4 at pin 21 is the TBRE (transmit buffer register empty) signal from pin 22 of the UART. To send data, the processor performs an Output 1 instruction during which the NO output is high. When TPB goes high, with MRD low, all inputs to NAND gate ML31b are high, so the TBRL signal to the UART goes low, thus loading data from the data bus into the UART. The UART outputs the data in serial form, via OR gate ML32b, as Disp Data, which leaves the board via connector pin H4; or the data goes via OR gate ML32c as Print Data via connector pin J7; the choice depends on the sense of the Q6 output (pin 15) from bistables ML27 (high for Print Data, low for Disp Data, set by the processor: Paragraph 35). Inversion of the Print Data signal occurs in ML33d if link LK3 is present; no inversion occurs if link LK2 is present.

Parity Bits in the UART

40. The UART does not check parity in the received data and does not use the parity facility in the data it sends as Disp Data. Whether or not it uses a parity bit in the data it sends as Print Data depends on the setting of links LK6 and LK7.

1. A parity bit is added to the data if PI (pin 35) is low. Therefore, if link LK6 is present, parity is added (the output from inverter ML33b must be low for a Print Data output). Odd parity is used (pin 39 is connected to 0 V). If link LK7 is present, PI is held high, so parity is not used.

Number of Bits in Character

42. The UART sends five bits of data in a character for Print Data (CLS2, pin 37, low), and seven bits of data in a Disp Data character (CLS2 high). This is controlled by the Q6 output from ML27 (Paragraph 35).

DIRECT MEMORY ACCESS

Receiving Data

43. The processor sets the Q̄1 output (pin 2) from bistables ML27 high (see Paragraph 30) when it is ready to receive data by direct memory access from an external processor. This signal leaves the board as Data I/O En via connector pin M8. The data transfer occurs when I/O Data C1k, which enters the board via connector pin M4, goes high. This makes the Q̄ output (pin 2) from bistable ML23a low (unless the bistable is directly reset by Reset 2 low (Paragraph 15)) causing a high input to the processor at DMA In (pin 38).
44. I/O Data Clock high loads bits 0 to 7 of the data bus, which enter the board via connector pins ML16 to M9, into latches ML5. The data is output to the board's data bus when the processor makes SC1 high and SCO low during a DMA cycle to remove the inhibit from pins 3 and 15 of the latches. The SCO, SC1 action also resets bistable ML23a via NAND gate ML3a, thus removing the low DMA In signal.

Sending Data

45. To send data via the parallel data bus to the Sync I/O Board, the processor performs an Output 4 instruction during which its N2 output goes high. This can occur only if the Data Req signal, which enters the board via connector pin M7 and is connected to the processor's EF2 input (pin 23), is logic high. When the TPB high pulse occurs, with MRD low, the output from AND gate ML15b is made high. This strobes data from the board's data bus into latches ML14. It also clocks bistable ML29b to produce a low Q̄ output (pin 2) which leaves the board as I/O DMA In, via connector pin M5, to inform the recipient processor that data is available.
46. In reply, I/O Data Dis, which enters the board via connector pin M2, is set low, thus removing the disable signals from pins 3 and 15 of latches ML14, so the data in the latches is output onto the external data bus.
47. The low I/O Data Dis signal also goes via NAND gate ML3d to directly reset bistable ML29b, thus removing the low I/O DMA In output signal.

CHECKING BATTERY VOLTAGE

48. To check the battery voltage, the processor sets the Q2 output (pin 5) and the Q4 output (pin 10) from bistables ML27 high (Paragraphs 31, 33). The Q4 output turns-on transistor TR1; this in turn causes transistor TR2 to switch Batt Mon, which enters the board via connector pin H13, through to the sense input, pin 6, of the A/D converter, ML21. The Q2 output from ML27 is clocked through bistable ML29a to make the WR input (pin 3) of the A/D converter low. This initiates a conversion cycle. A 1.25 V reference voltage (pin 9) is provided by amplifier ML30 and resistors R22, R21 from the +5 V supply.
49. When conversion is completed, the A/D converter makes its INT (interrupt) output (pin 5) low; this goes to the processor's E/F input. To read out the conversion, the processor performs an Input 4 instruction. The N2 output goes high, so when MRD goes high the output from NAND gate ML35d is low: this makes the RD (read) input (pin 2) of the A/D converter low, causing it to output the 8-bit result.

POWER-DOWN

50. Req Off, which enters the board via connector pin H6, goes low to request turn-off. This causes a high output from NAND gate ML35a, which, inverted by inverter ML33a, makes the INT input (pin 36) to the processor low, thus initiating an interrupt. This also occurs when Batt V Low, which enters the board via connector pin J1, is low.
51. The Interrupt routine stores the current status and message pointers, then sets the Q output high, making the Run signal from ML3b pin 11 low to turn the unit off. If the processor detects that an external power supply is connected (Paragraph 24), the program does not set the Q line.
52. The Req Off signal (Paragraph 50) also, after a delay, removes the Run signal, making the CLR input (pin 3) to the processor low. This resets the processor so that if, for some reason the normal running of the program has failed and the processor is in a stalled condition, the processor can start again in order to carry out the turn-off procedure (Paragraph 51).

Memory-Protection during Power-Down

53. The program stored in the ROMs is not affected by the removal of power; power is needed only during read operations. The workspace RAMs require power or their contents are lost; a back-up battery on the board provides power for the RAMs when the external supply is removed.
54. When the board is powered-up, the Run signal goes high, so N-channel transistor ML34c conducts and P-channel transistor ML34d is off (ML34c and ML34d are a complementary pair). Therefore, transistor TR3 conducts and Vram is supplied from the +5 V supply. The silver-zinc battery is charged via resistor R34 and LED D6.
55. When the board is powered-down, the low Run signal causes ML34d to conduct and ML34c to turn-off. Therefore, Vram is provided by the silver-zinc battery via ML34d.

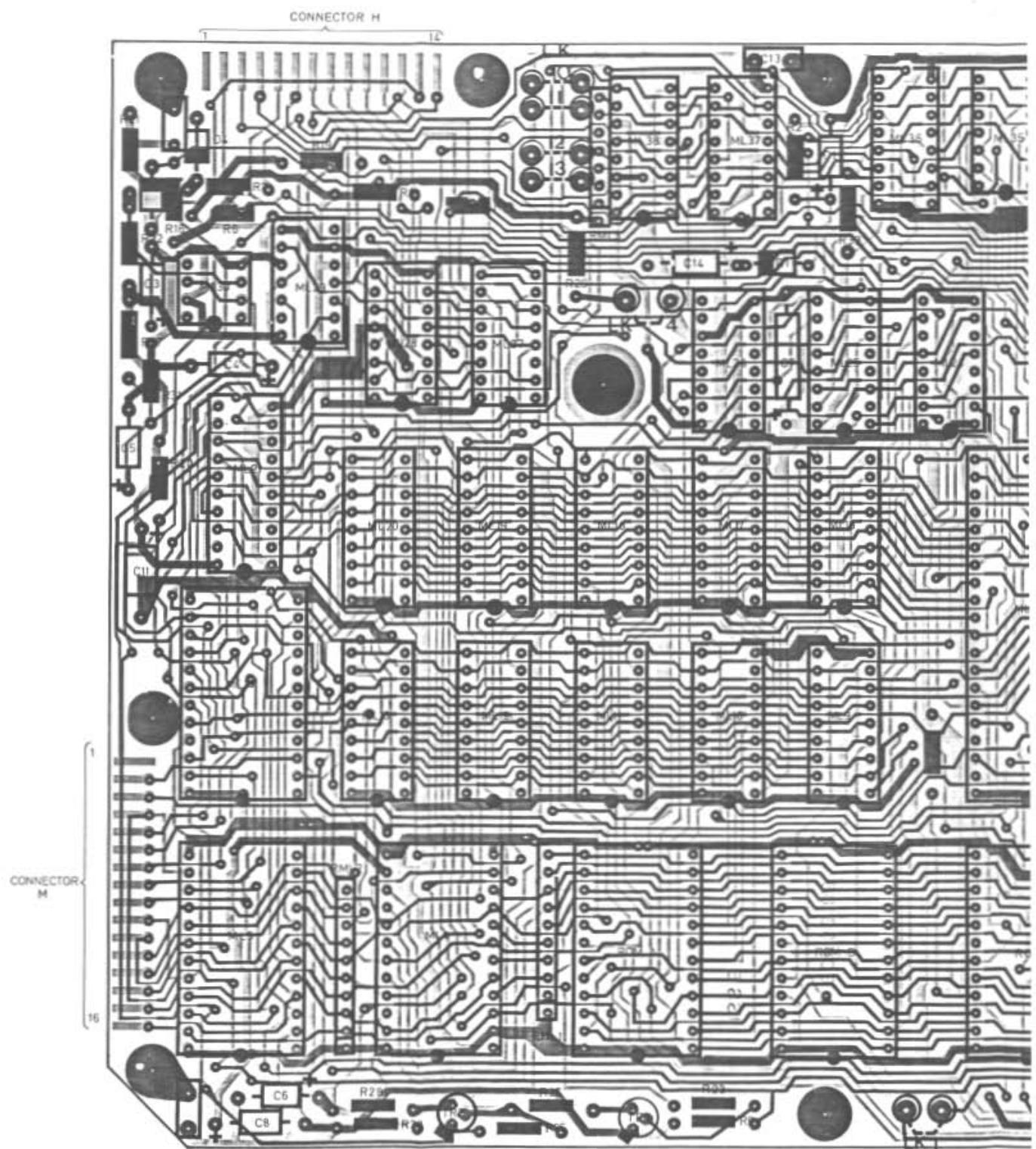
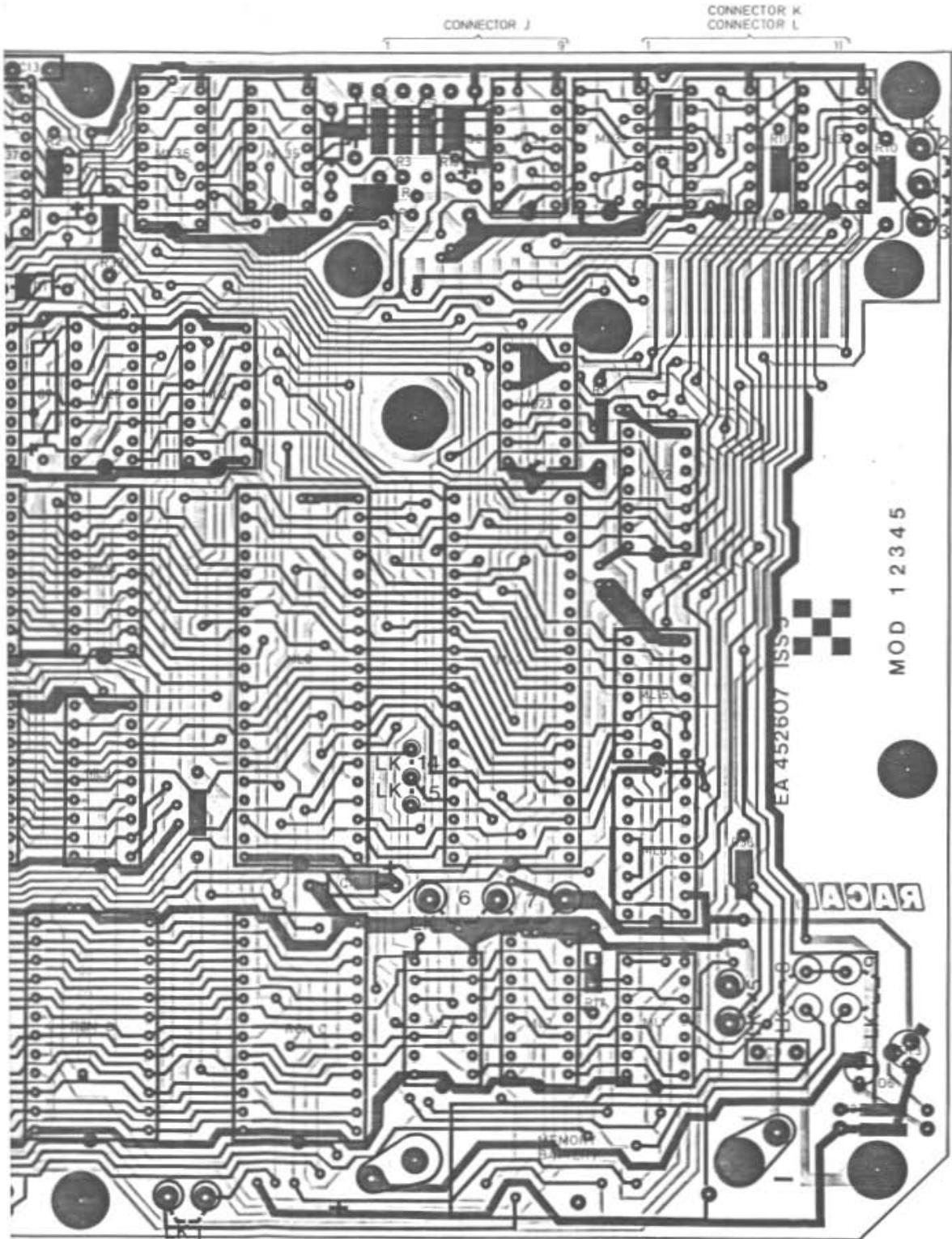
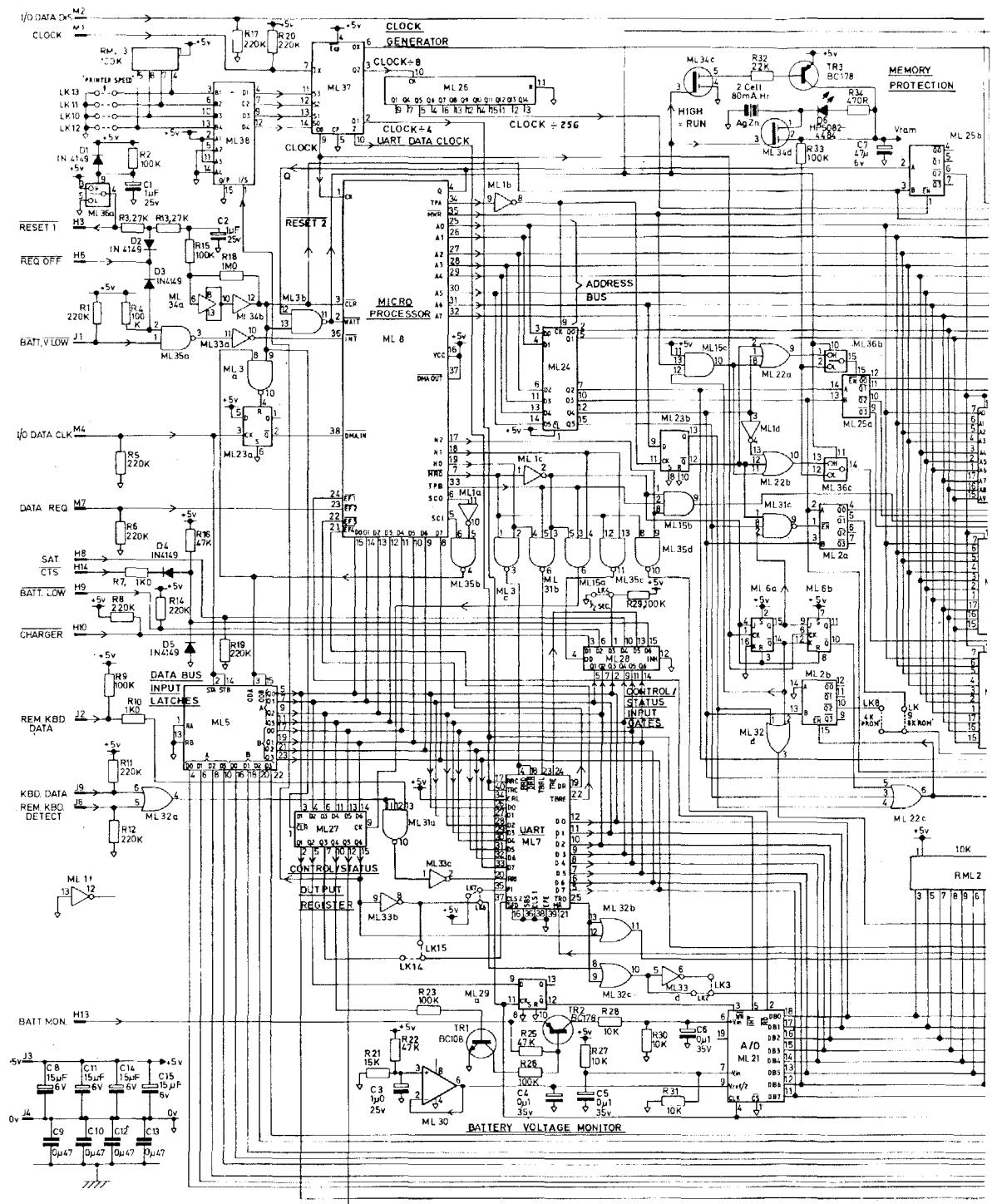
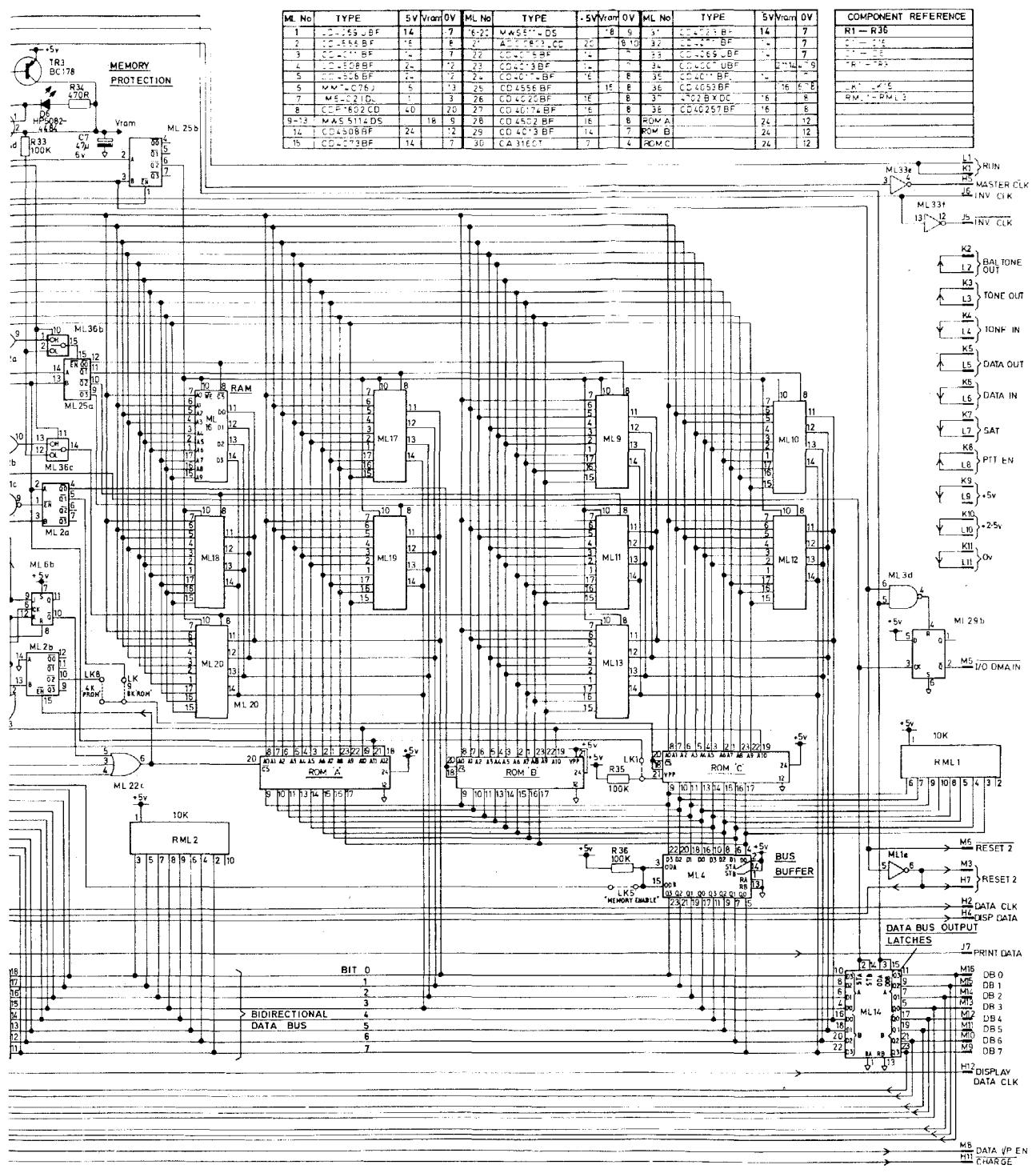


Fig.5.4.3 Main Processor Board (452607): Layout



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Main Processor Board (452607): Circuit

Fig.5.4.4

CHAPTER 5

POWER BOARD - 452610

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Fig. No.

- 5.5.1 Power Board: Layout
- 5.5.2 Power Board: Circuit

CHAPTER 5

POWER BOARD - 452610

GENERAL

1. The Power Board 452610 provides supply rails for the unit and interfaces with external equipment; the circuit is shown in Figure 5.5.2. The board contains the following functions:
 - (1) +5 V regulation.
 - (2) -5 V and -15 V generation.
 - (3) Battery-low indication.
 - (4) Battery charging.
 - (5) Data signal level conversion (to/from MIL STD 188-114 levels).
 - (6) PTT generation.
 - (7) RF decoupling.

+5 V SUPPLY

Regulation

2. The +5 V regulated supply, output at connector pins E14, J3, K9, A/E, is from either Vext, input at connector pins B/B, C/B, D/B; or Batt +ve, input via connector pins E2, E15, via transistor TR23. The output from the transistor is also fed back to the regulating part of the circuit: it goes via R44 and R45 to the base of TR20; also, with Zener diode D23, it provides a reference voltage input to TR20.
3. If the output from the regulating transistor TR23 is low, TR20 (which has its emitter clamped by reference diode D23 and its base driven from a potentially divided value of the output voltage) conducts more, causing the darlington pair TR22 and TR24 to conduct more. This increases the base current of the regulating transistor and thereby increases the current output to make the output voltage rise. If the output from the transistor is high, the opposite occurs: TR20, TR22, TR23 conduct less, reducing the current output and therefore the output voltage.

Switching-on

4. When external power is applied, Vext, limited by Zener diode D22 provides a reference voltage for TR20, and (via D20) turns on TR19. Once the regulating transistor TR23 begins to conduct, the reference is produced in the normal way, by D23 (Paragraph 3).
5. If external power is not present, regulation is initiated by a low Req On signal, which enters the board via connector pins A/C and E12. The low

signal switches the battery +ve supply through TR13 to provide the reference supply (with D22) and turn on TR19. The low Req On signal is present only while a key is being pressed to turn the unit on: when the regulator has started-up, the reference voltage is provided in the normal way, by D23 (Paragraph 3), and TR19 is held on by Run (high), which enters the board via connector pin K1.

-5 V and -15 V GENERATION

6. The -5 V and -15 V supplies are generated from Inv Clk and its inverse, Inv CTK, which enter the board via connector pins J6 and J5 respectively, by an inverter circuit consisting of transformer T1 and associated components. The Inv Clk and Inv CTK signals are ac-coupled to transistors TR2 and TR4; the transistors are held off when Reset I, which enters the board via connector pin H3, is low. Transistors TR6 and TR5 which are connected to opposite ends of the transformer's primary winding, turn on alternately thereby creating a 5 V peak a.c. signal across the primary.

The outputs from the transformer's secondary windings are rectified and smoothed to provide a -5 V supply and a -15 V supply; the latter leaves the board via connector pin E11.

BATTERY-LOW INDICATION

8. When the battery output is at a satisfactory level, TR21 is conducting. When the collector-emitter voltage of TR23 drops below 0.6 V, TR21 turns off, turning-off TR25. This causes the input to Schmitt inverter ML3c to go high. The resulting low output of inverter ML3c leaves the board via connector pin H9 as Batt Low.
9. A battery very low signal is produced when the inverting input to comparator ML2b (pin 6) goes above 2.5 V indicating that the regulator is unable to maintain regulation and TR23 is saturating. The output from the comparator leaves the board as Batt V Low via connector pin J1.

BATTERY CHARGING

The battery is charged by a constant-current circuit consisting of TR10 and associated components. The charging circuit is fed by Vext (connector pins B/B, C/B, D/B) via fuse FS1 and provides charging current to the battery via the Batt +ve connections (connector pins E2, E15). While Vext is present, the Charger signal, which leaves the board via connector pin H10, is low.

11. When the Charge signal, which enters the board via connector pin H11 is low, TR3 is off, so the -ve input of comparator ML1a is held at a reference voltage produced by R18, R11 and D11. ML1a compares the voltage across resistors R3 and R4 in the Batt -ve line (connector pins E1 and E16) with the reference, and adjusts the current through TR7 and hence the charge current through TR10 to balance its two inputs. The voltage across R3 and R4 is proportional to the current passing into the battery. If the voltage at the collector of TR10 rises above 10 volts, Zener diode D9 starts to conduct, changing the current feedback at ML1a pin 5 to a

voltage feedback, thereby turning the circuit into a voltage regulator. This facility is used when no battery is fitted, or when the battery is being charged at a low temperature (to prevent cell voltages from rising above their maximum).

12. When Charge is high, TR3 conducts, almost short-circuiting R11, thus lowering the reference to ML1a, and a small trickle charge goes via TR10 (in addition to the unit running current).

DATA SIGNAL-LEVEL CONVERSION

Input Data

13. Data In (from satellite radio) enters the board via connector pin C/F. If the data is balanced input, connector pin C/G is also used; otherwise C/G is connected to 0 V. The data signal, divided by resistors to define the thresholds, goes to comparator ML2a which converts it to logic levels; the comparator output leaves the board via connector pin K6.

Output Data

14. Data Out is converted to a current-limited +5 V/-5 V signal by transistors TR8, TR9, TR11, TR12 and associated resistors. When Data Out, which enters the board via connector pin K5, is high it turns on TR8, which turns on TR12, connecting +5 V to the Data Out output, connector pin CC, via current-limiting resistor R34. When Data Out (input) is low, TR9, and TR12 conduct, connecting -5 V to Data Out (output) via current-limiting resistor R31. Print Data is converted in a similar way by TR15, TR16, TR17, TR18.

PTT GENERATION

15. When PTT En, which enters the board via connector pin K8, is high, TR14 conducts, energising relay RLA. Relay contact RLA/1 closes and connects PTT (connector pin D/C) to 0 V.

RF DECOUPLING

16. The Power Board provides RF decoupling for all signals to/from the unit. Two capacitors and a choke are used for each line (one capacitor is located on the associated socket; see Figure 5.1.6).

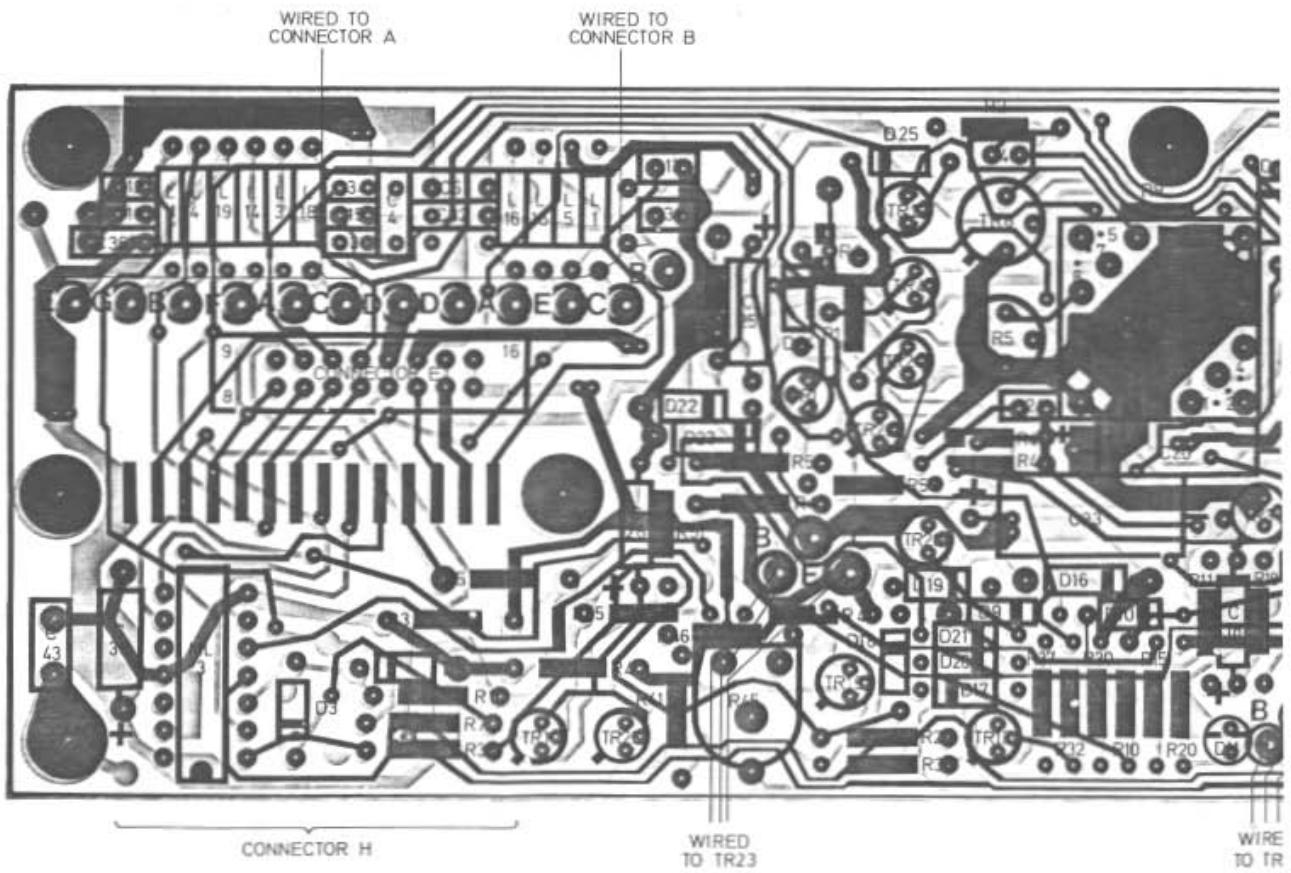
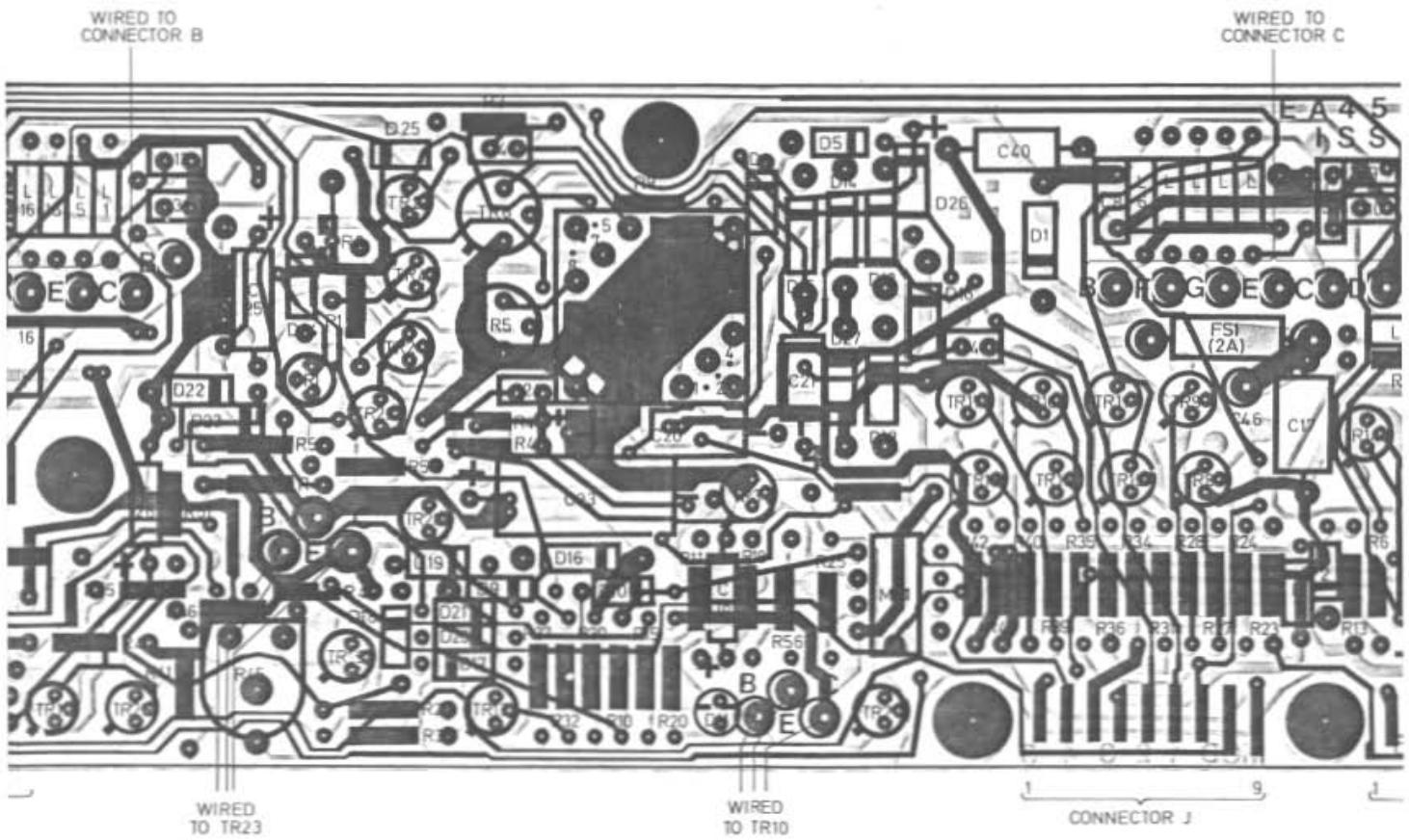
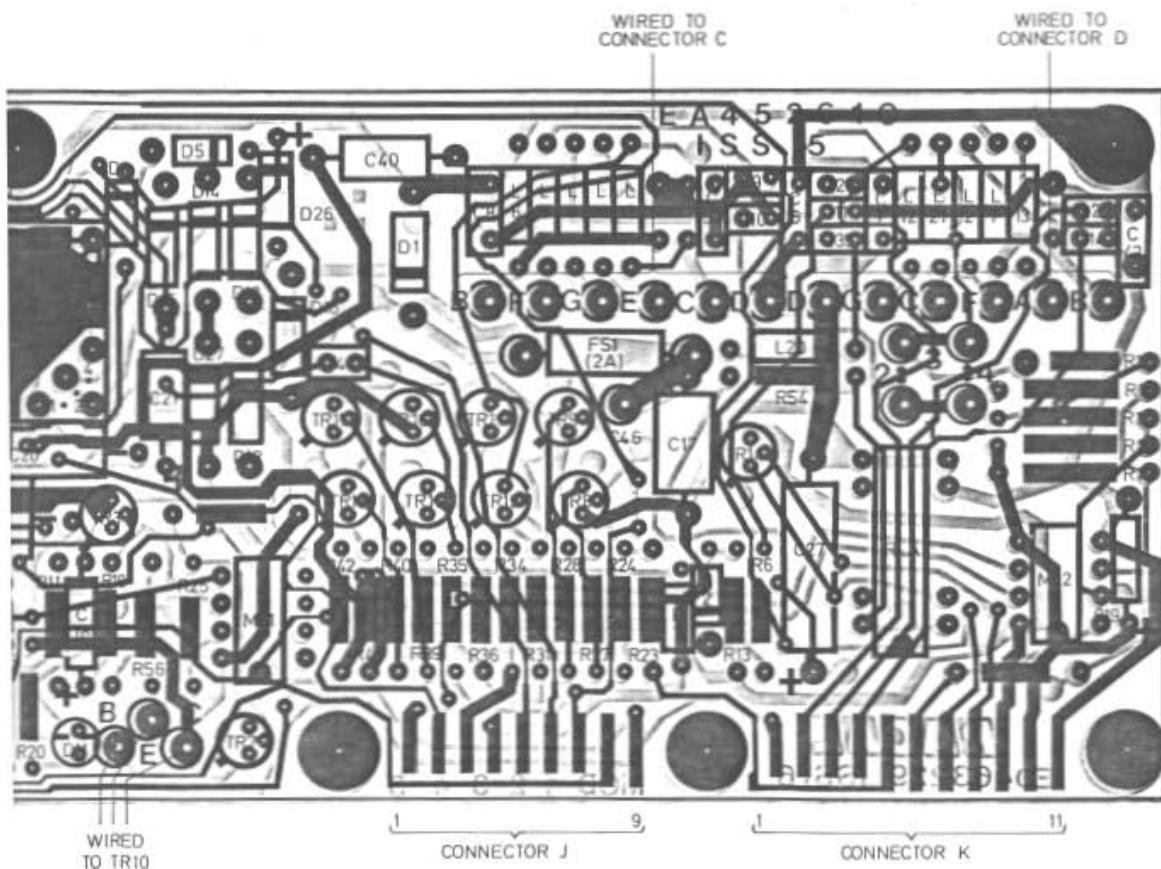


Fig.5.5.1 Power Board (452610) :Layout



:Layout



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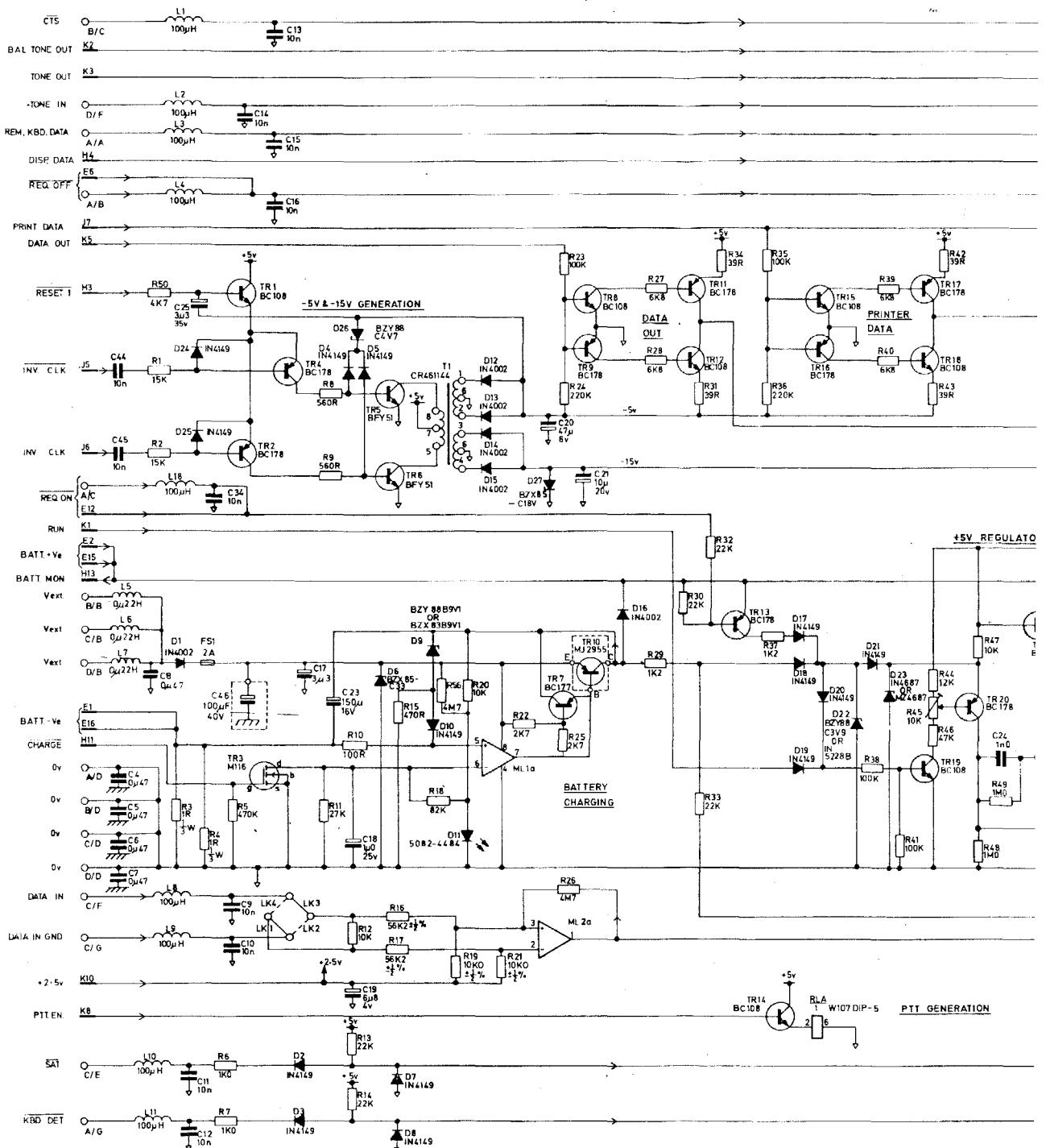
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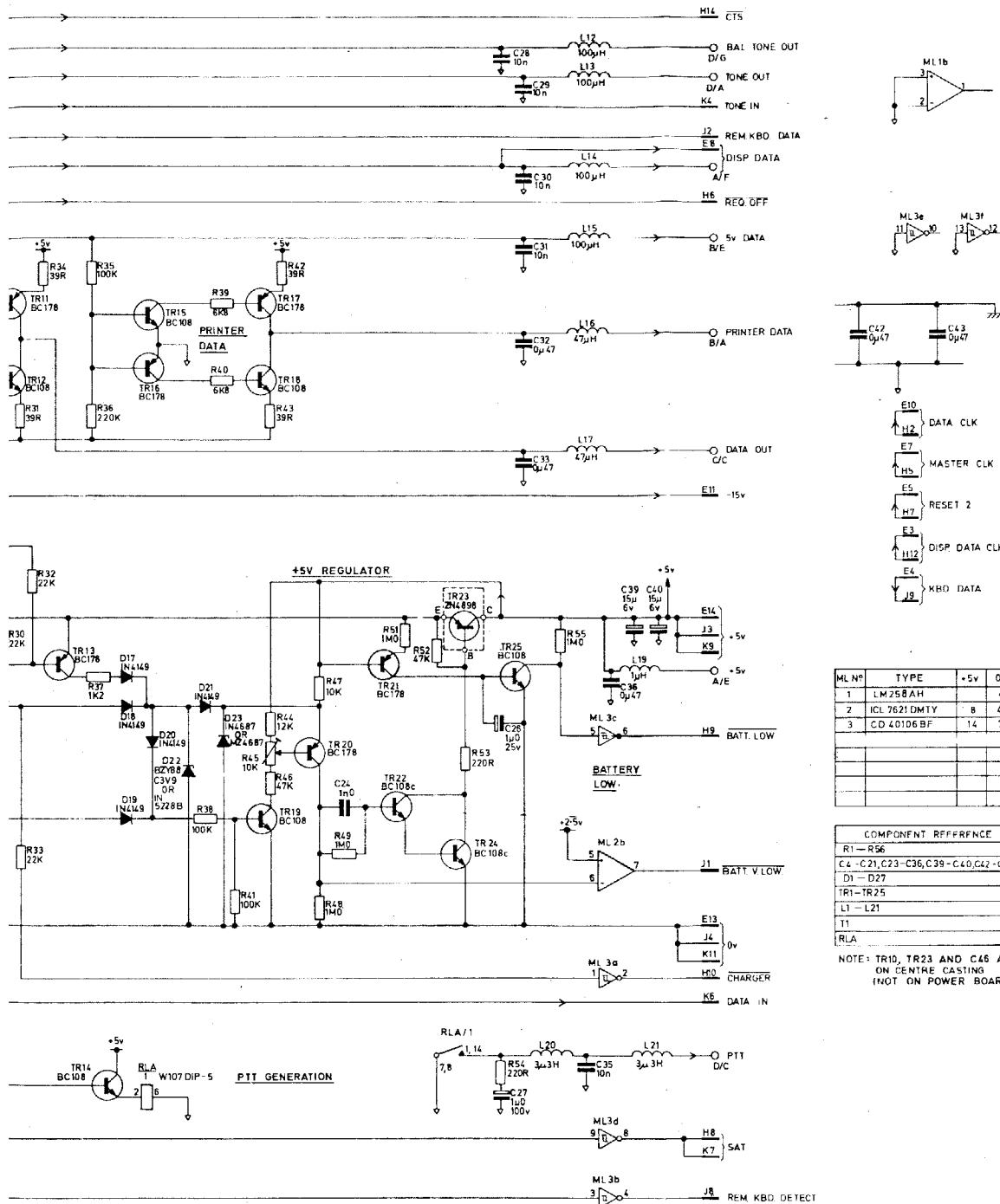
ISSUE 6/6/6, 4.81

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Power Board (452610): Circuit

Fig.5.5.2

CHAPTER 1

MAINTENANCE

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CHAPTER 1

MAINTENANCE

ROUTINE MAINTENANCE

1. The MA 4248 requires very little routine maintenance. It is sealed and should not be opened unless a fault is to be rectified.
 - (1) Visually check the unit and its associated cables for damage (e.g. cracks in casing, damaged connector pins, cuts in cables, loose connections, etc).
 - (2) Clean the unit using a lint-free cloth.
 - (3) Switch the unit on (or apply power, as applicable). It should display SELF TEST COMPLETE UNIT O.K. (If the unit displays LAST 5 CHAR GROUP INCOMPLETE, complete or erase the message as applicable, switch off, then on; the unit should respond with SELF TEST COMPLETE UNIT O.K.).
 - (4) If the unit is being operated on battery power and the POWER indicator flashes, charge the battery. This can be done by connecting the unit to the radio, or by using a battery charger (11 V minimum (including -ve ripple) to 32 V maximum (including +ve ripple) d.c., 1A). If the unit is using external power, the POWER indicator should be on when power is connected.

IDENTIFYING A FAULTY UNIT

2. The MA 4248 has a self-test facility which checks its main functions. When the unit is switched on (or power is applied, as applicable), it displays SELF TEST COMPLETE UNIT O.K. (or LAST 5 CHAR GROUP INCOMPLETE: See paragraph 1(3)); or, if a fault is detected, it displays an ERROR message.
3. If a unit does not fail the self test, but is not working correctly in a system, use it with different cables and different radio and printer, replacing the items one at a time. This establishes whether the fault is in the unit, the radio, the printer, or the cables.

FAULT FINDING

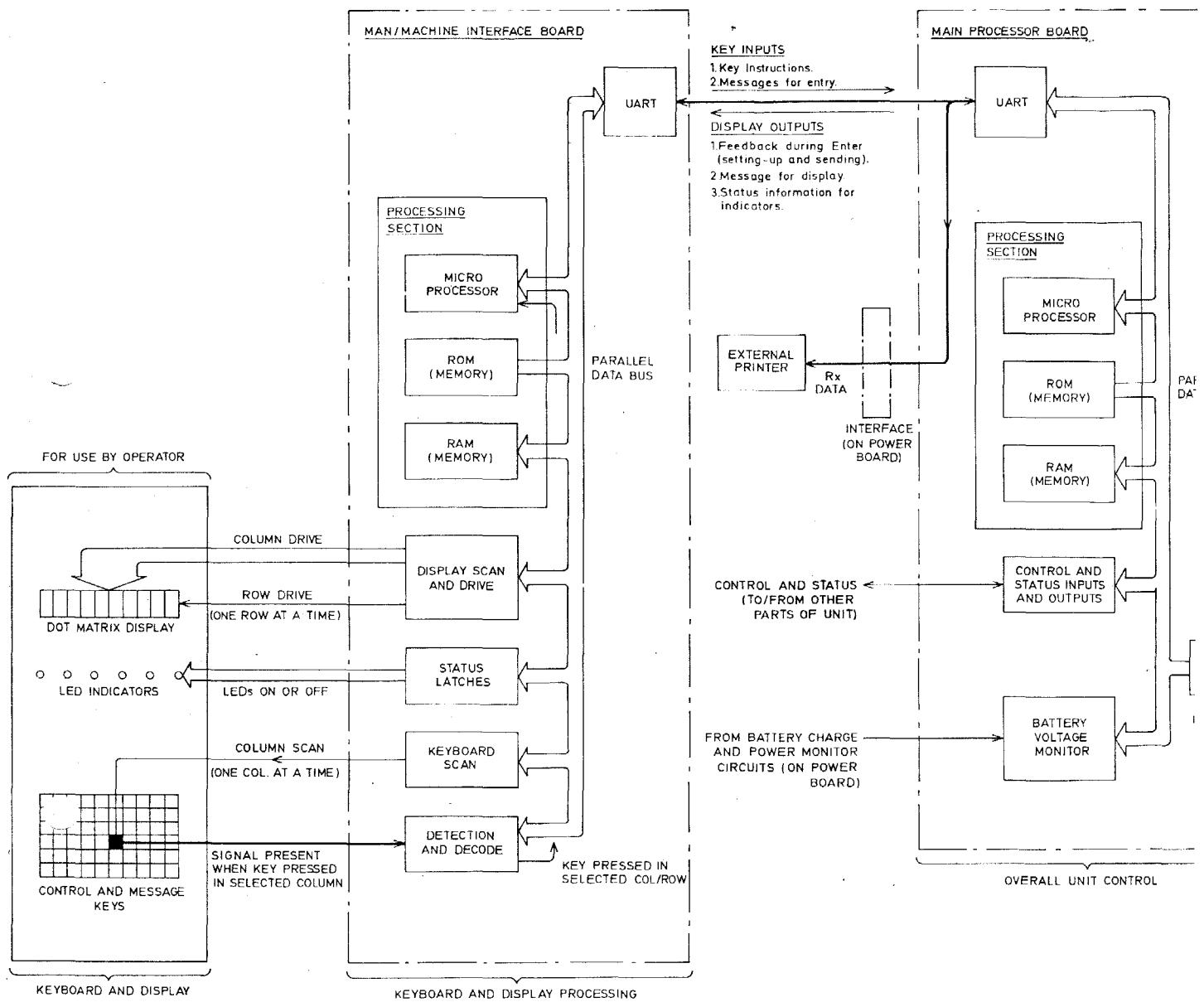
4. If an error message is displayed, or another fault occurs, fault rectification is by replacement of modules.
5. The faulty module can be identified by the error message (Table 1) or by operator observation during operation (Table 2).

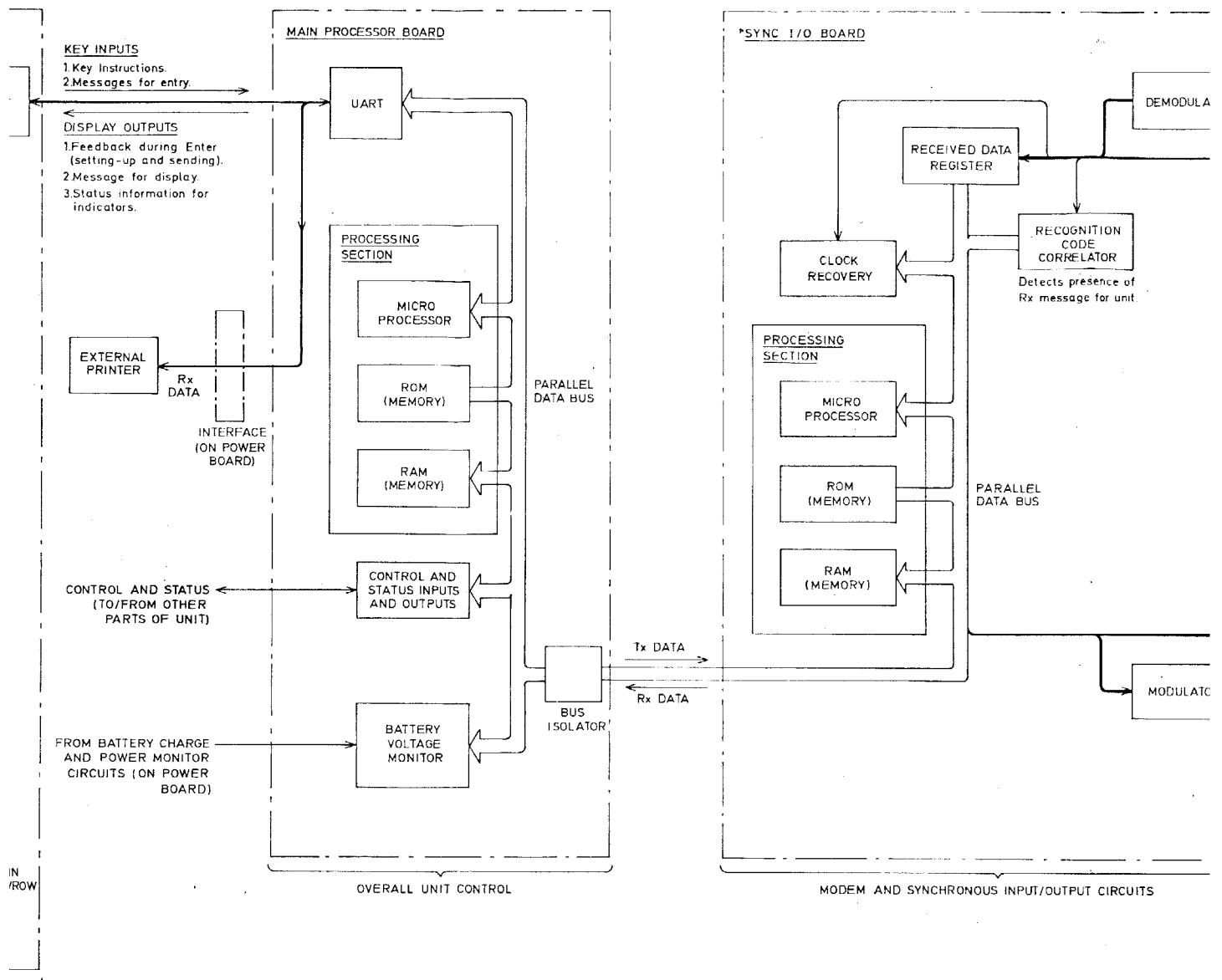
TABLE 1 DISPLAYED ERROR MESSAGES

Message	Meaning	Suspect (in order)
ERROR 1	Main processor module not running	(1) Main Processor Board Assembly (2) Man/Machine Interface Module Assembly (3) Sync I/O Board Assembly
ERROR 2	Main processor memory (RAM) fail	(1) Main Processor Board Assembly
ERROR 3	Main processor/MMI link fail	(1) Man/Machine Interface Module Assembly (2) Main Processor Board Assembly
ERROR 4	MMI memory fail	(1) Man/Machine Interface Module Assembly
ERROR 5	Sync I/O module not running	(1) Sync I/O Board Assembly (2) Main Processor Board Assembly
ERROR 6	Sync I/O memory fail	(1) Sync I/O Board Assembly (2) Main Processor Board Assembly

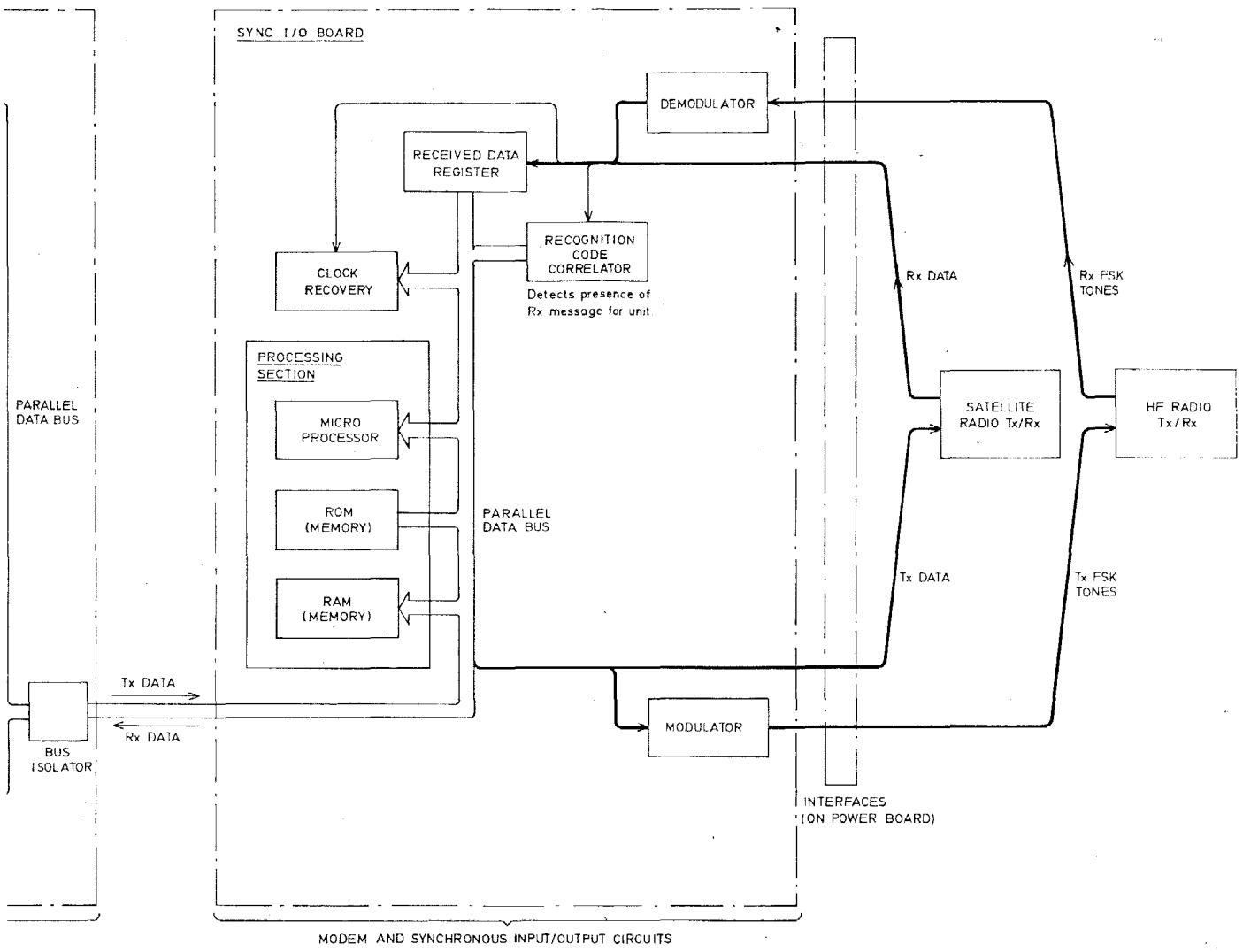
TABLE 2 OTHER FAULTS

Fault	Suspect (in order)
No message on display	(1) Man/Machine Interface Module Assembly (2) Power Module Assembly
No message on display and no LEDs on	(1) Main fuse (if using Vext) (2) Battery fuse (if using battery)
Display not working correctly (eg. Black marks or missing rows)	(1) Man/Machine Interface Module Assembly
Unit sending but not receiving	(1) Sync I/O Board Assembly (2) Power Module Assembly (3) Main Processor Board Assembly
Unit receiving but not sending	(1) Sync I/O Board Assembly (2) Main Processor Board Assembly (3) Power Module Assembly (4) Man/Machine Interface Module Assembly
Unit not responding to keyboard	(1) Man/Machine Interface Module Assembly (2) Main Processor Board Assembly (3) Power Module Assembly
Random pattern on display	(1) Man/Machine Interface Module Assembly (2) Main Processor Board Assembly



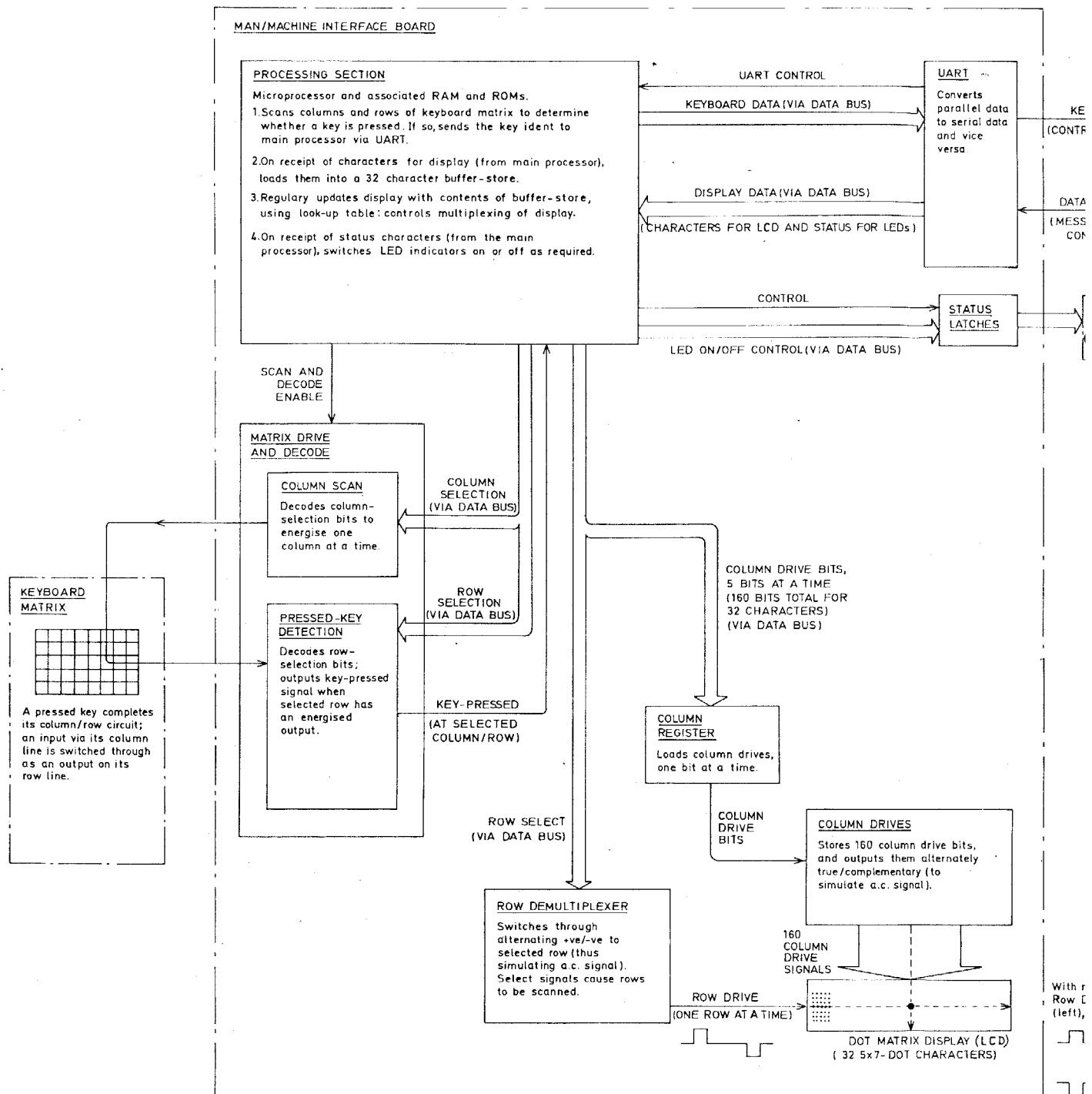


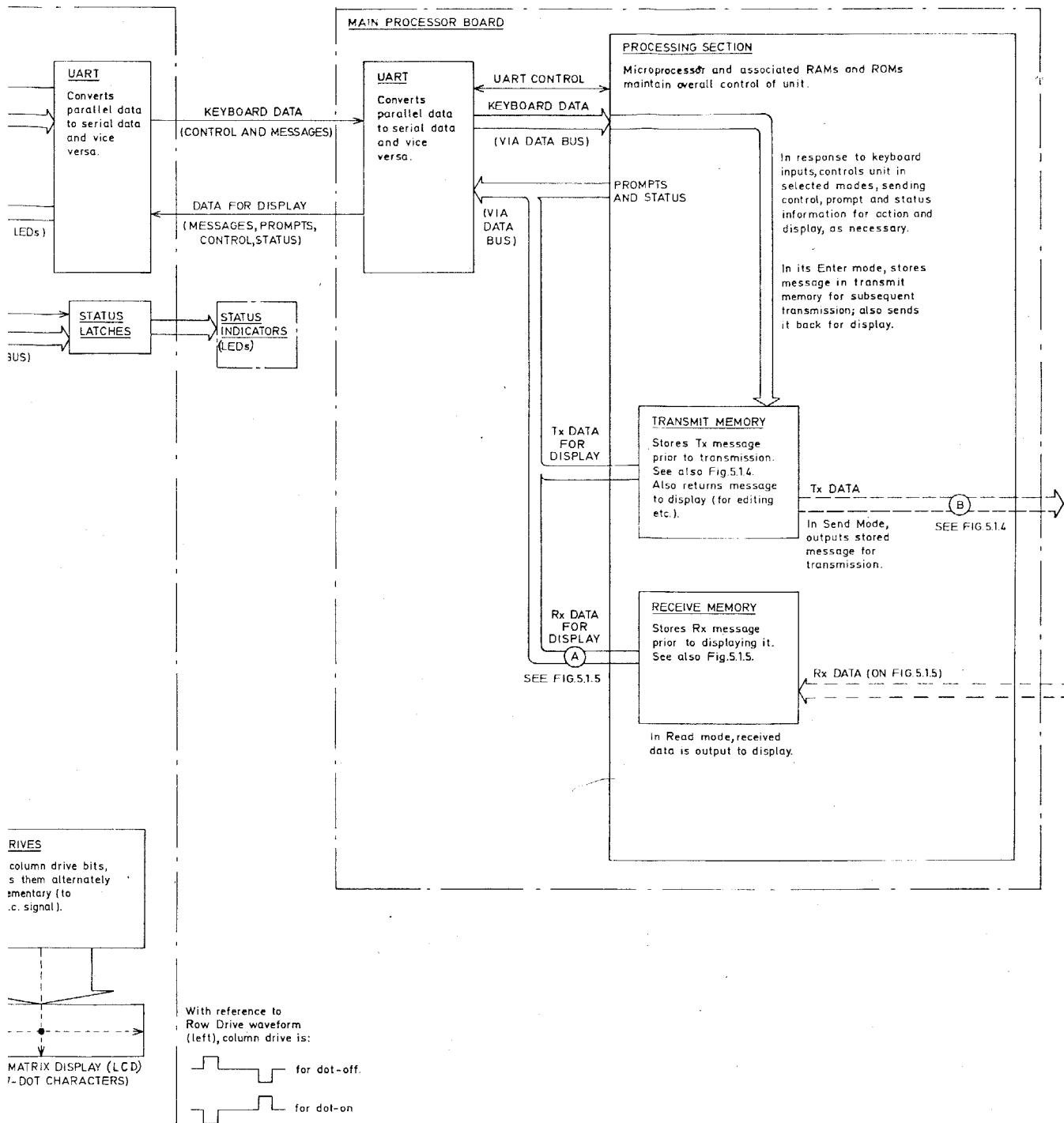
MA4248: Over
Showing Mair



MA4248: Overall Block Diagram
Showing Main Signal Paths

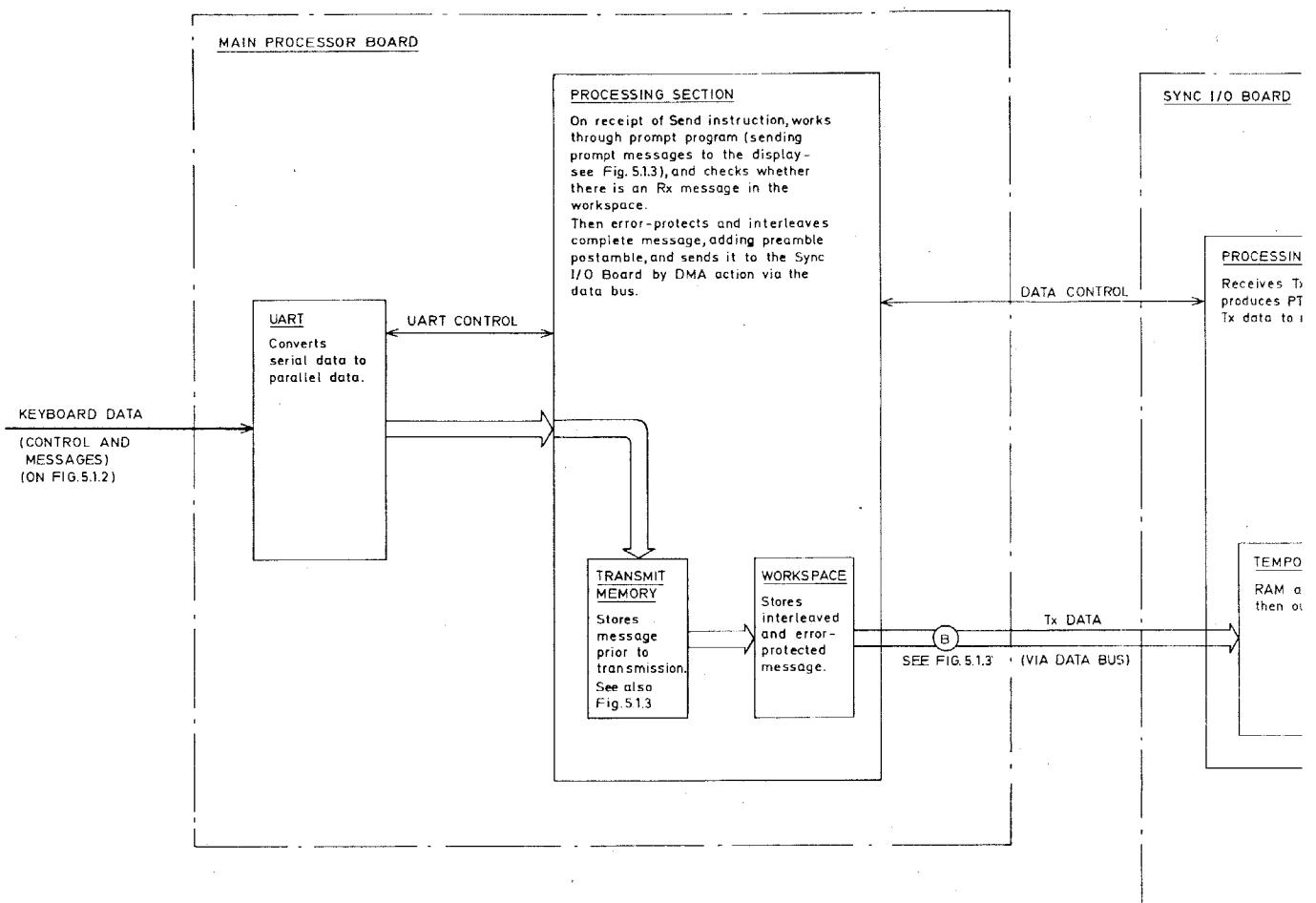
Fig.5.1.2

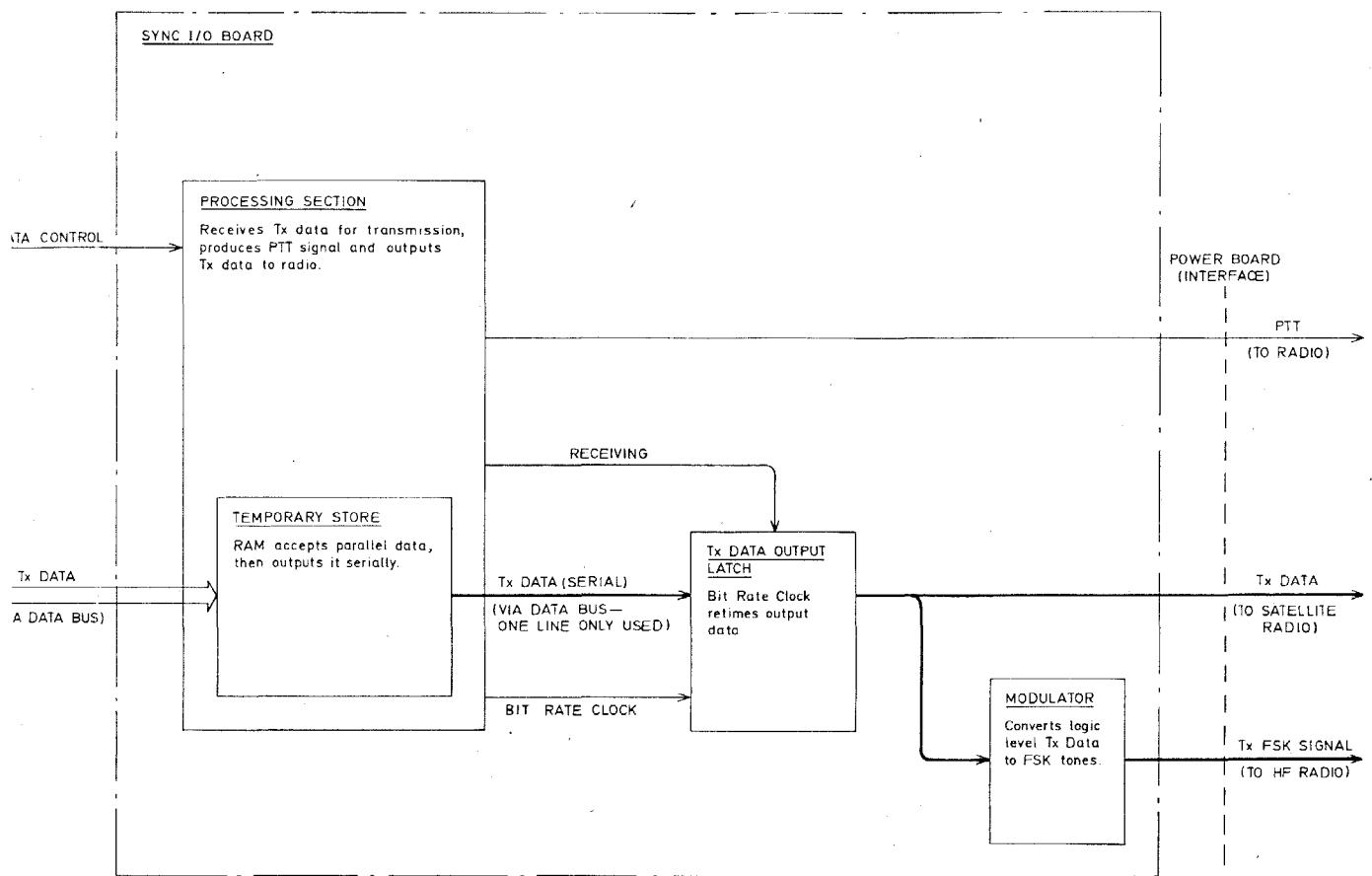




Keyboard and Display: Simplified Diagram

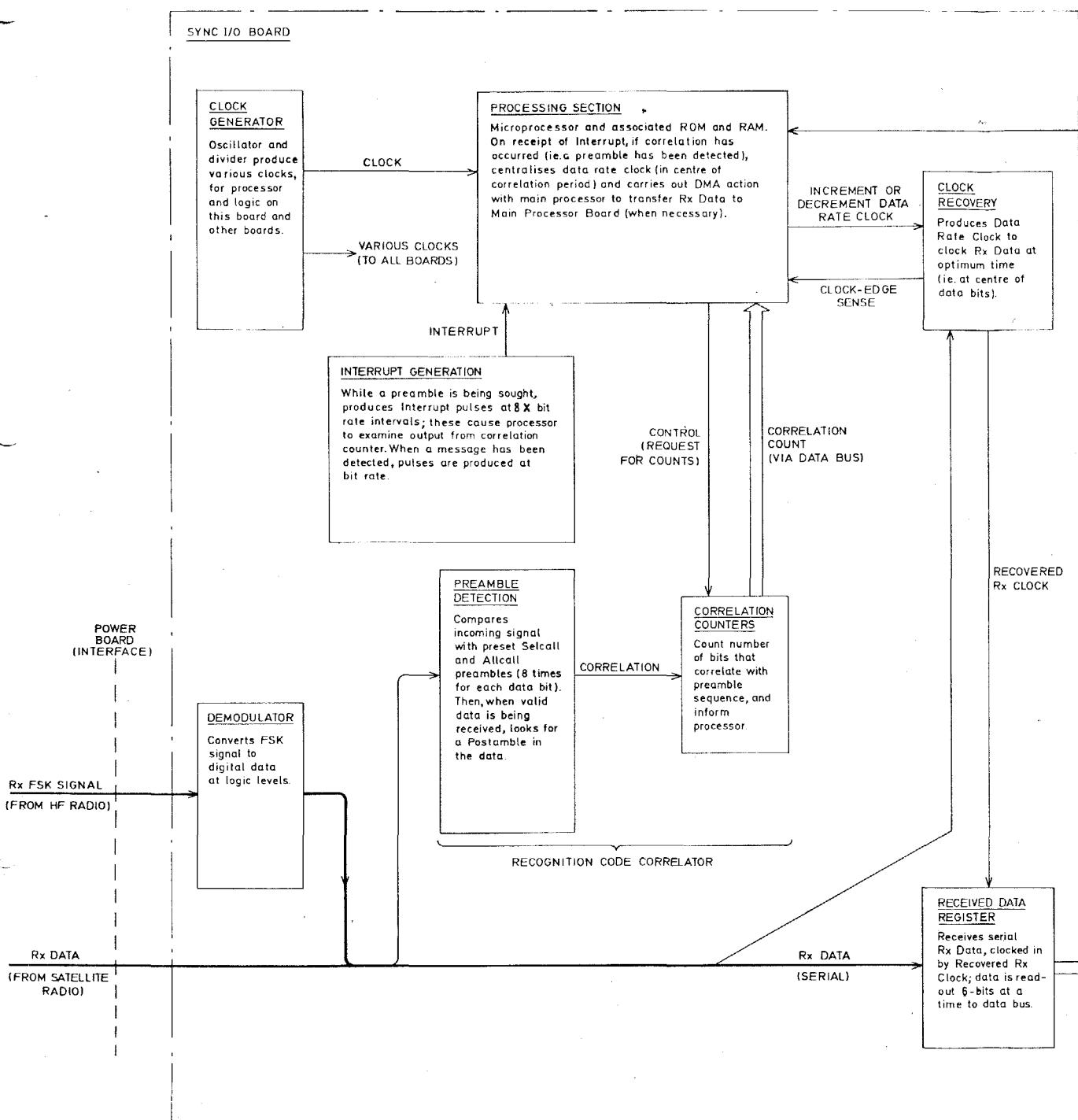
Fig. 5.1.3

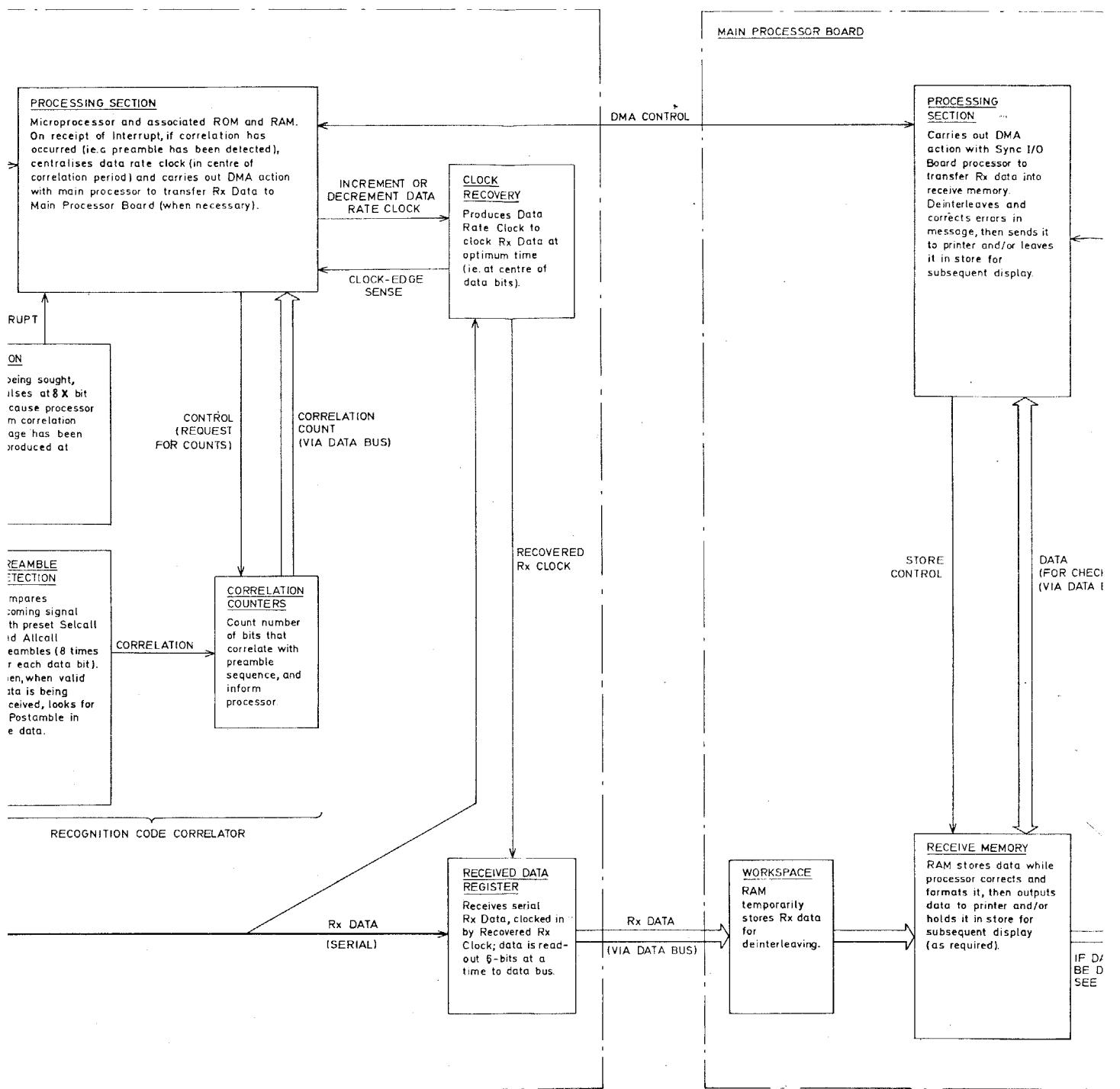




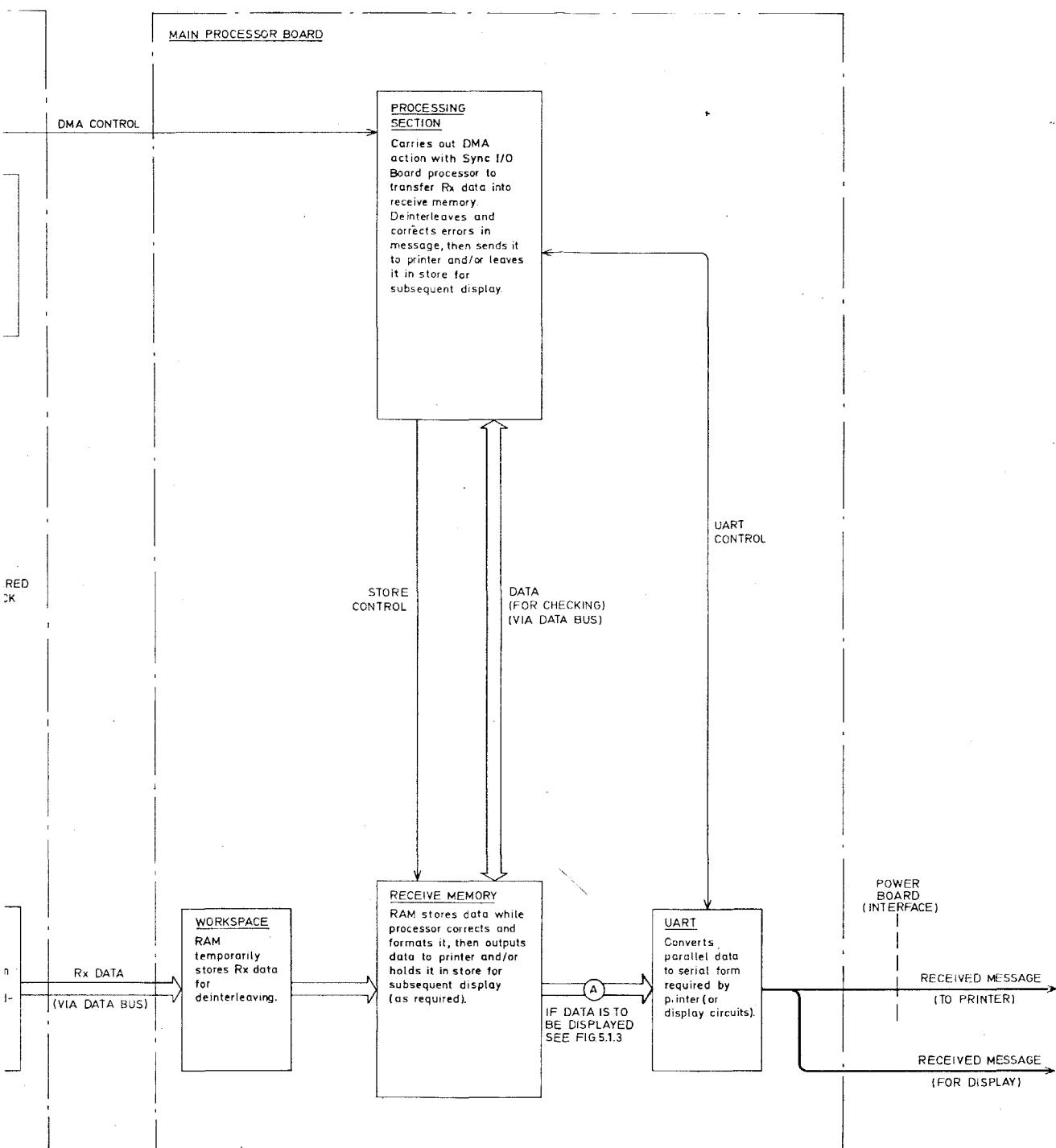
Sending Data:
Simplified Diagram

Fig. 5.1.4



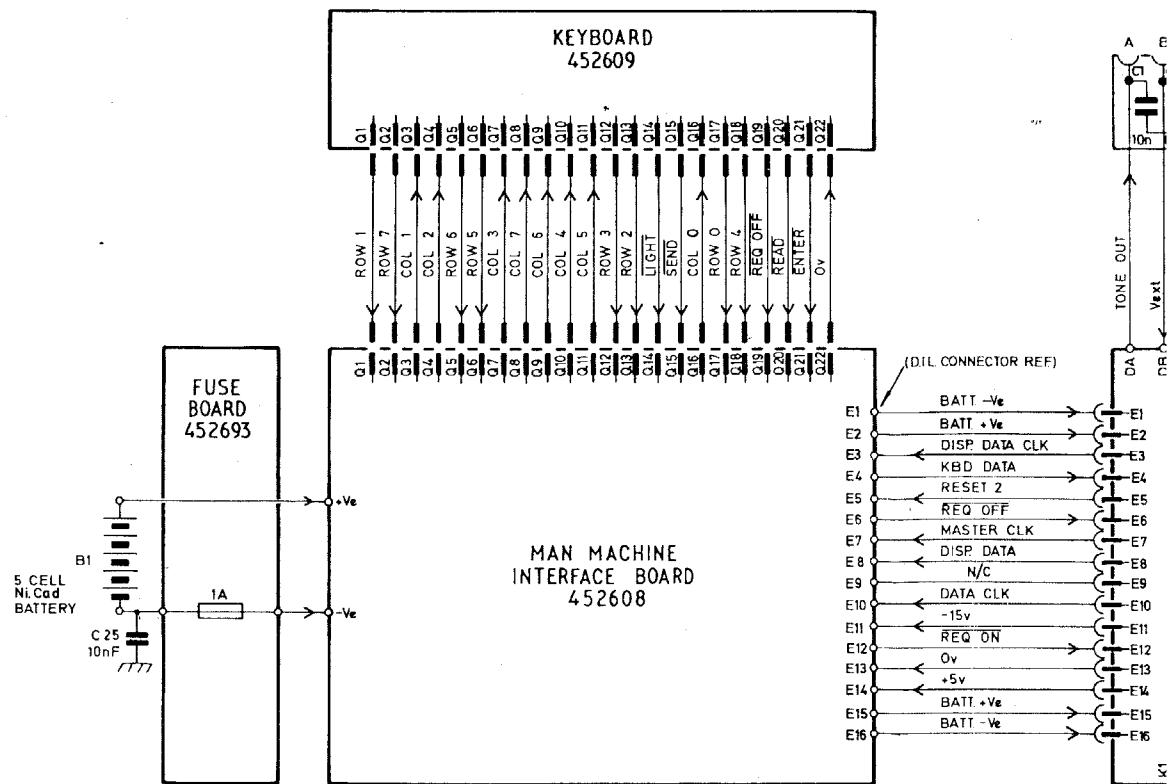


Receiving
Simpli

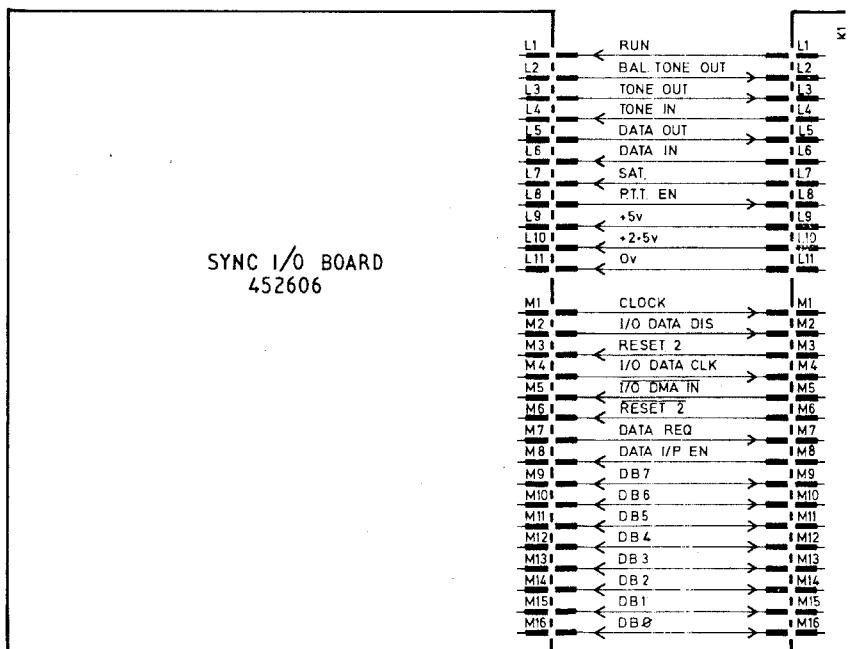


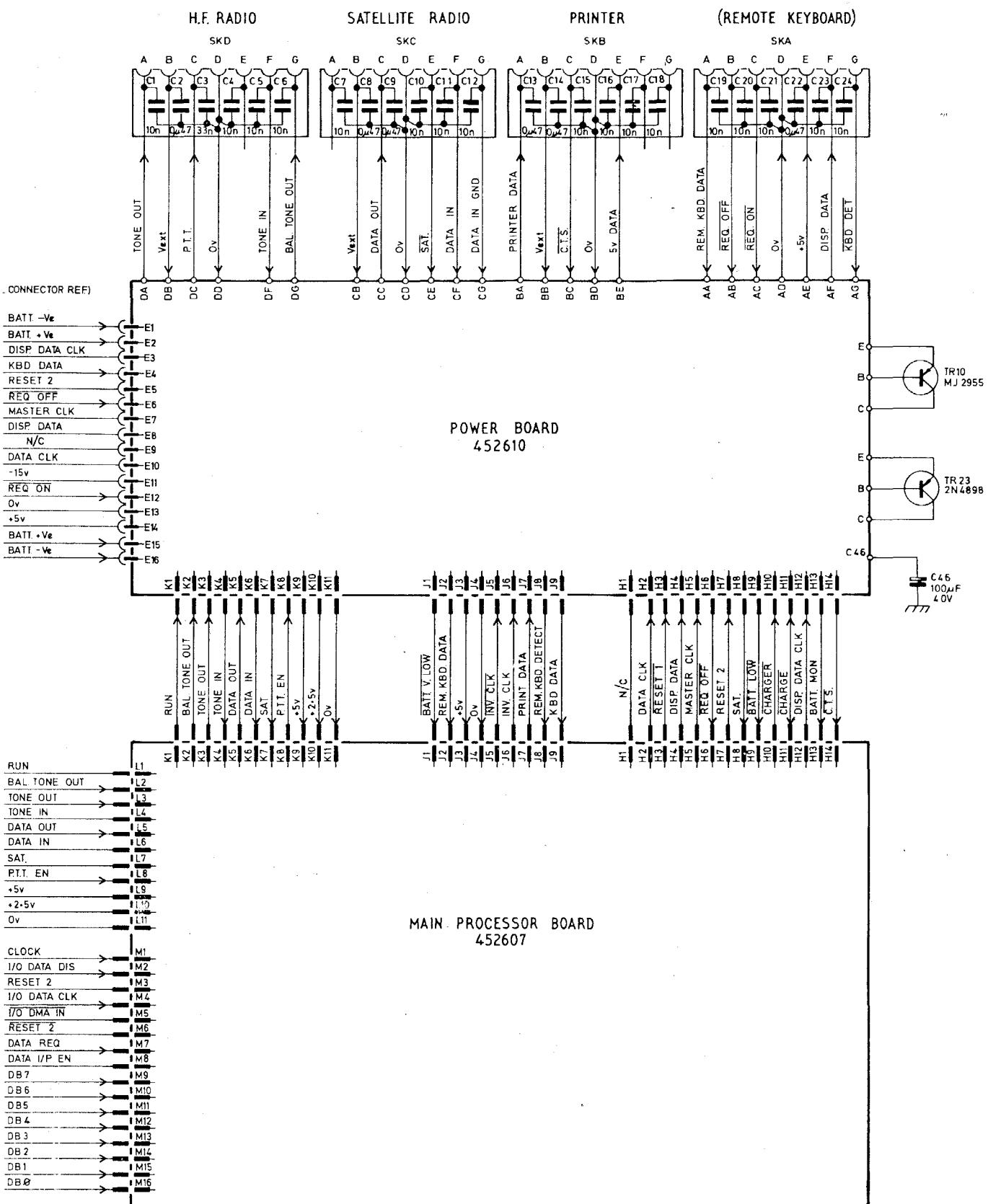
**Receiving Data:
Simplified Diagram**

Fig.5.1.5



CONNECTOR REF	DESCRIPTION
SKA	BULKHEAD 7 WAY SOCKET 62 GB-5016-10-7SF
SKB	BULKHEAD 7 WAY SOCKET 62 GB-5016-10-7SB
SKC	BULKHEAD 7 WAY SOCKET 62 GB-5016-10-7SE
SKD	BULKHEAD 7 WAY SOCKET 62 GB-5016-10-7SE
E	PLUG DIL 3M 3416-0000 STRAIN RELIEF 3M 344-B SOCKET 3M 3452-6000 HEADER PLUG 3M 3408-2202 POLARISERS 2 OFF 3M 3518
H	TECKNIT DS100 BR 461151
J	TECKNIT DS100 BR 461152
K	TECKNIT DS100 BR 461153
L	TECKNIT DS100 BR 461155
M	TECKNIT DS100 BR 461154
Q	TECKNIT DS100 2 OFF BR 461156





MA 4248: Interconnections

Fig 5.1.6

CHAPTER 2

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MAN/MACHINE INTERFACE BOARD - 452608

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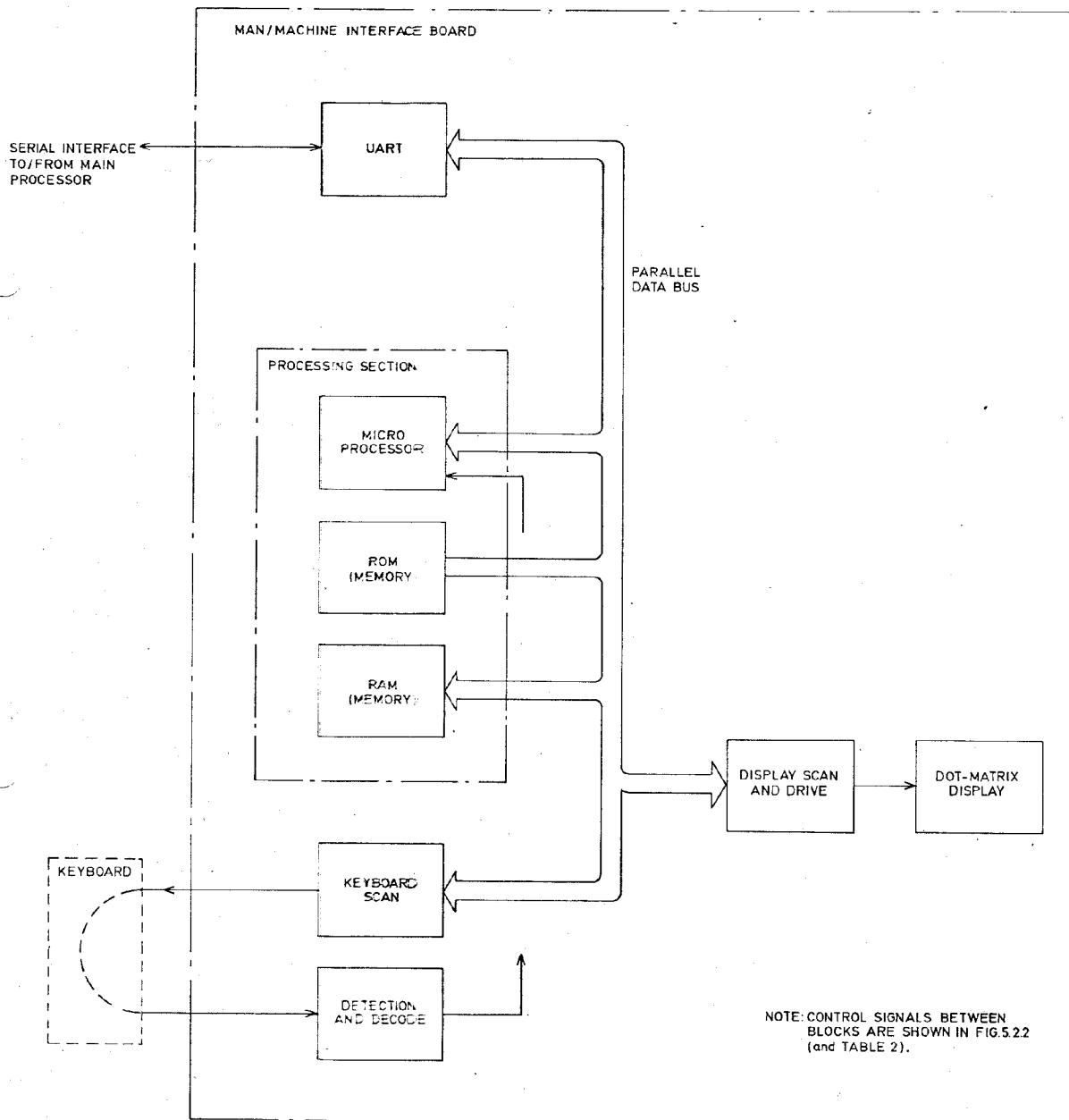


Fig.5.2.1

**Man/Machine Interface Board:
Simplified Block Diagram**

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CHAPTER 2

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MAN/MACHINE INTERFACE BOARD - 452608

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(AND KEYBOARD - 452609)

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GENERAL

1. The Man/Machine Interface Board 452608 provides keyboard and display control; the circuit is shown in Figure 5.2.7, the Keyboard 452609 circuit is shown in Figure 5.2.8. The Man/Machine Interface Board contains the following functions:
 - (1) Microprocessor, which controls the keyboard scan, display drive and serial interface with other boards.
 - (2) Control program for the board's operation (in ROM).
 - (3) Display character 'look-up' memory (in ROM).
 - (4) Working storage for the processor during execution of routines (in RAM).
 - (5) Keyboard matrix scan and pressed-key detection circuits (standard keyboard plus function keys).
 - (6) Voltage generator and drivers for the dot-matrix display.
 - (7) Interface between microprocessor and the microprocessor on the Main Processor Board (UART).
 - (8) Status indicator (LED) and backlight drivers.

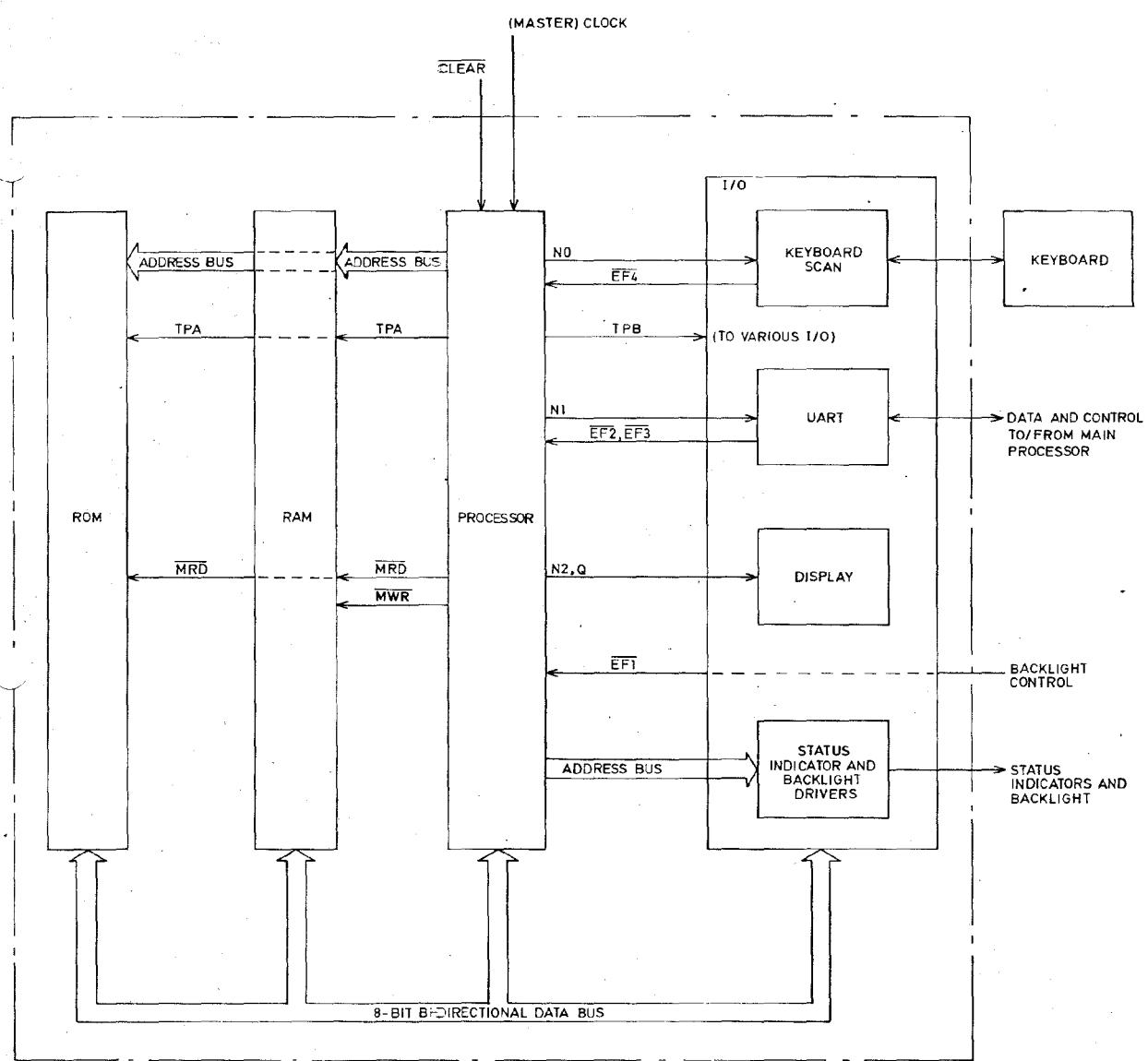


Fig.5.2.2 Simplified Block Diagram of Processing Section used on Man/Machine Interface Board

THE PROCESSING SECTION

Brief Description of Processor

2. Microprocessor ML9 is an RCA CDP1802 eight-bit register-orientated central processing unit which includes all of the circuits required for fetching, interpreting and executing instructions that have been stored in associated memories; it also produces control signals for, and accepts control signals from, external devices.
3. The basic timing signal for the microprocessor is Ck at pin 1, which enters the board as Master Clk via connector pin E7. The microprocessor works in eight-clock-cycle operations, using eight Master Clock cycles to fetch, eight cycles to execute an instruction, etc. At eight-clock-cycle intervals, it produces TPA pulses, then, later in the sequence, TPB pulses. These pulses are used as basic timing signals for the memory and the associated I/O (input/output) circuits on the board.
4. While the Master Clock pulses are present, the microprocessor works through its program, which is held in its associated memory, 1k x 8 bits ROM, ML10. The processor addresses a part of the memory, using the address lines A0 to A7 and the information stored in the addressed part of the memory is fed back to the processor via the bi-directional eight-bit data bus, D0 to D7. The processor then processes and outputs the information according to the requirements of information previously fetched from store and according to any received control signals.
5. The processor uses 16-bit (hexadecimal) multiplexed addressing: it outputs the higher-order byte, A8 to A15, first (timed by TPA), then the lower-order byte, A0 to A7. The addresses used for the various parts of the circuit are shown in the memory map, Table 1.

TABLE 1 - MEMORY MAP (MAN/MACHINE INTERFACE BOARD)

Address	Device
0000 to 03FF (0 to 1023)	ROM (ML10)
0400 to 0403 (1024 to 1027)	Status latches (ML19 & ML26)
0800 to 081F (2048 to 2079)	RAM (ML2)
0820 to 083F (2080 to 2111)	RAM (ML3)

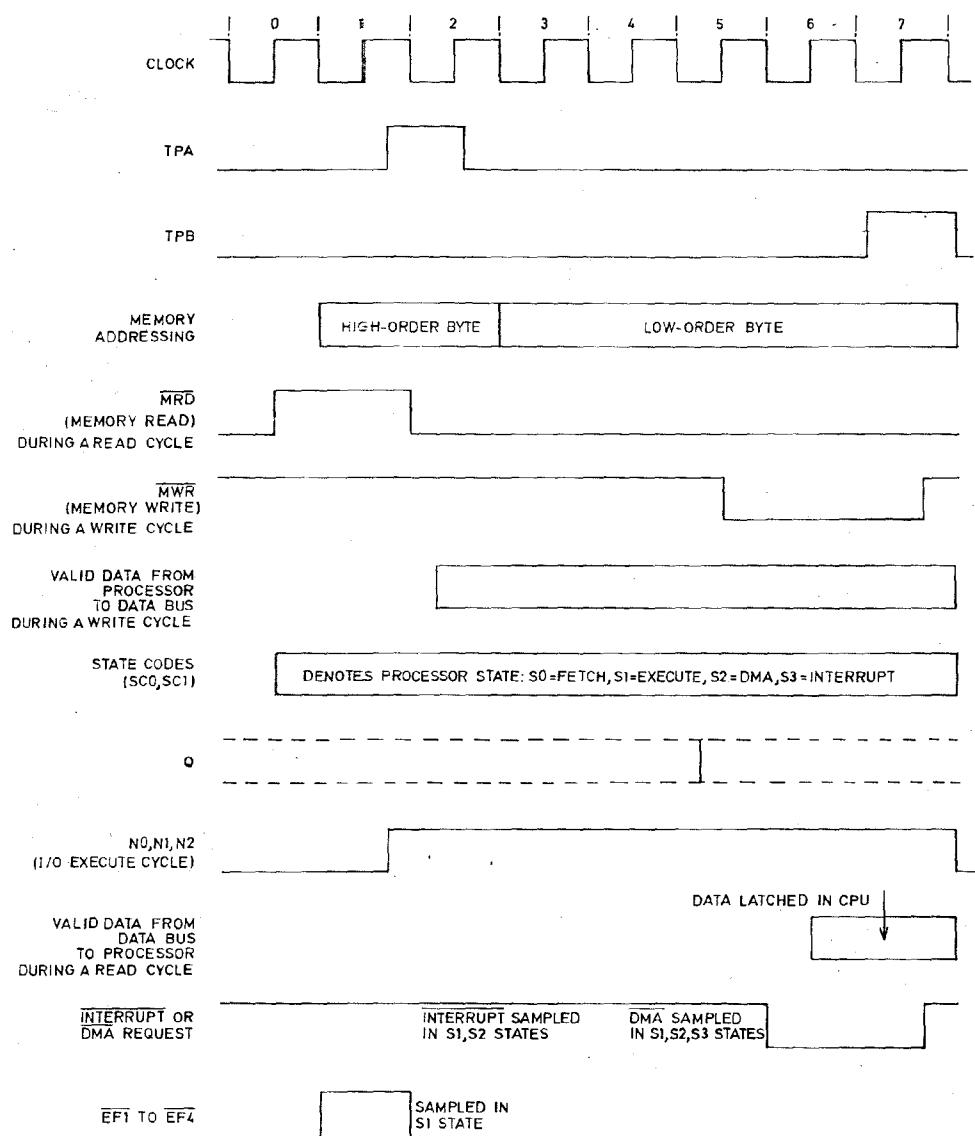


Fig.5.2.3 Processor: Simplified Timing Diagram

6. External flag signals received on its EF1 to EF4 inputs enable the processor to monitor external events and execute particular parts of the program as necessary. The processor uses its N0 to N2 outputs and its Q output to control other devices. These control signals are described with the parts of the circuit to which they relate, as listed in Table 2.

TABLE 2 - DIRECT COMMAND SIGNALS TO/FROM THE MICROPROCESSOR

Signal	Use	Description in Handbook
<u>Inputs</u>		
EF1	Backlight switch pressed.	Paragraph 35
EF2	UART ready to accept data for transmission.	Paragraph 12
EF3	UART has received data.	Paragraph 10
EF4	Key pressed.	Paragraph 16
<u>Outputs</u>		
N0	Data on bus is key address (during keyboard scan).	Paragraph 14
N1	Data on bus is for or from UART (ie.to/from external processor), depending on the state of MRD.	Paragraphs 10 & 12
N2	Data on bus is for alpha-numeric display.	Paragraph 22
Q	Switches row drive voltage to display.	Paragraph 28

Program Store

7. The microprocessor program is stored in 1k x 8 bits ROM (read-only memory) ML10. (ML10 also stores the look-up table for the display: see Paragraph 22.) The low-going edge of TPA from pin 34 of the processor clocks bistables ML4 and thus latches the high-order address, bits A8 to A11 of the address lines; if bits 10 and 11 are low, the output from OR gate ML5 to the CSI input (pin 20) of ML10 selects the ROM. (The output from the gate remains low until after the next TPA pulse.) When MRD from pin 7 of the processor goes low later in the processor's cycle, CS2 (pin 18) goes low and allows the contents of the currently addressed part of the ROM to be read out onto the eight parallel data bus lines.

Working Store

8. Two 32 x 8 bit RAMs (random-access memories), ML2 and ML3 are used by the processor for storing display information. The RAMs are addressed by the processor in a similar manner to the ROM (Paragraph 7): address bit 9 is low and bits 11 and 13 are high to select ML3, bit 11 is high and 13 is low for ML2. A RAM is enabled by low CS and MRD or MWR inputs. The CS input (pin 15) is low for the duration of the selecting address on the address lines. The selected RAM writes data (eight bits) from the parallel data bus into the addressed location when MWR at pin 17 is low; when MRD at pin 16 is low, data is read out to the data bus.

SERIAL INTERFACE TO/FROM MAIN PROCESSOR VIA UART

9. Serial data transfer between processor ML9 and other boards is via UART (universal asynchronous receiver/transmitter) ML11. Serial data (Disp Data) enters the board via connector pin E8 and goes to the RRI input, pin 20, of the UART; the associated clock, Data Clk, enters via E10 and goes to RRC (pin 17) and TRC (pin 40) to time both receive and transmit operations in the UART. Reset 2, which enters the board via connector pin E5, goes to MR (Master Reset), pin 21, of the UART; when MR is high it initialises the internal registers and resets the status lines.

Receiving from the Serial Interface

10. A data character consists of a low Start bit, seven data bits and a high Stop bit. When the UART has received a complete character (ie. half-way through the Stop bit), it transfers the character to its receive buffer register and makes DR (Data Received), from pin 19, high. This informs the processor (via EF3) that the UART has data to transfer. On detecting this, the processor performs an input instruction which makes N1 high, so that at the next MWR high pulse from the processor, both inputs to NAND gate ML6b are high. The resulting low RRD (Receiver Register Disable) signal at pin 4 of the UART causes the UART to output the data bits via RBRO to 7 (pins 12 to 5) onto the parallel data bus. Simultaneously, the low DRR (Data Received Reset) signal at pin 18 resets the DR signal low.
11. The input instruction transfers the character from the UART via the data bus, into the RAM where it remains until the processor is ready to use it (eg. in the next display drive routine). If the character was a status character, the program outputs the appropriate data to set and reset the LEDs (Paragraph 37).

Sending via the Serial Interface

12. When the UART is free to send a character, the TBRE (Transmitter Buffer Register Empty) signal from pin 22 of the UART is high. This goes to the processor's EF2 input. To send data via the serial interface, the processor (after checking that its EF2 input is high) performs an OUT 2 instruction while addressing the RAM location that contains the data to be sent. NAND gate ML6a provides the latching TBRL (Transmitter Buffer Register Load) signal to pin 23 of the UART: this signal is the timing pulse TPB gated with the MRD and N1 signals from the processor; the data is latched from the parallel data bus into the UART via TBRO to 7 (pins 26 to 33) when the TBRL signal returns from low to high.
13. The UART automatically adds Start and Stop bits and clocks the data out serially, via pin 25, at a rate of one data bit per sixteen Data Clk pulses. The data leaves the board as Kbd Data via connector pin E4 (at 1800 bauds). The UART makes TBRE high as soon as the data has been transferred from its buffer register to its transmitter register (ie data is being sent); the UART is then ready to accept more parallel data.

KEYBOARD OPERATION

14. The keyboard is arranged as part of an 8×8 matrix. The processor scans the matrix by outputting each 6-bit key address in turn (3 bits for row address, 3 bits for column address) to demultiplexers ML17 and ML8. The demultiplexers are selected during the Output 1 (keyboard address) instruction: the high NO output (pin 19) from the processor is inverted by inverter ML18e to remove the inhibit signals from the demultiplexers (pin 6).
15. Demultiplexer ML8 applies +5 V from its common input (pin 3) to the addressed column output line. If a key in that column is pressed, the +5 V is fed back to ML17 on the key's row line; if the pressed key is in the row that is currently being addressed, the +5 V is switched through ML17's common output, pin 3, as a Key Pressed signal.
16. The high NO signal from the processor gates the high-going edge of TPB through AND gate ML12c to clock the Key Pressed signal through bistable ML13a (If the key is not pressed, the input to the bistable is held low by 0 V via R19). The Q output (pin 1) from the bistable goes to the processor as EF4. Following the output instruction, the processor checks the EF4 input to determine whether the addressed key was pressed.

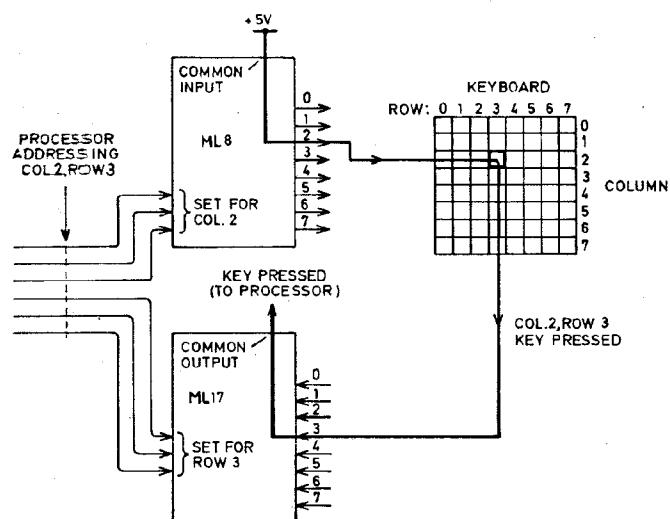


Fig.5.2.4 Pressed-Key Detection: Simplified Diagram

17. The three mode keys: ENTER, READ and SEND, when pressed, make contact closure to 0 V. When the ENTER key is pressed, the 0 V Enter signal at connector pin Q21 makes the A input (pin 11) of switch ML1 low (via diode D21). This connects the Col 0 line (pin 2) to the Row 4 line (pin 3), therefore the low Enter signal simulates a pressed key at the Col 0, Row 4 address. Likewise, Read (connector pin Q20) goes to the B input (pin 10) of ML1, and connects pin 5 to pin 3, simulating a pressed key at the Col 6, Row 4 address; Send (connector pin Q15) goes to the C input of ML1, and connects pin 12 to pin 3, simulating Col 7, Row 4.
18. When one of the mode keys, ENTER, READ or SEND, is pressed, the Req On signal, which leaves the board via connector pin E12, is made low (via diodes D3, D2, D1). This signal goes to the Power Board to initiate unit power-up.

DISPLAY CONTROL

Liquid Crystal Display

19. The 32-character display is a liquid crystal 7 x 5 dot matrix type. To turn-on a dot, an a.c. voltage is applied between the dot's row and column lines.
20. The seven display rows are multiplexed: an a.c. signal is applied to each row in turn. Each of the 160 columns has its own a.c. signal, and this is made in-phase with the row signal for a dot-off condition, out-of-phase for a dot-on condition. (See the bottom two items in Figure 5.2.5.) For a particular dot, the in-phase signals make an a.c. voltage (between the row and column) that is below the dot's turn-on threshold, the out-of-phase signals cause an a.c. voltage above the threshold.

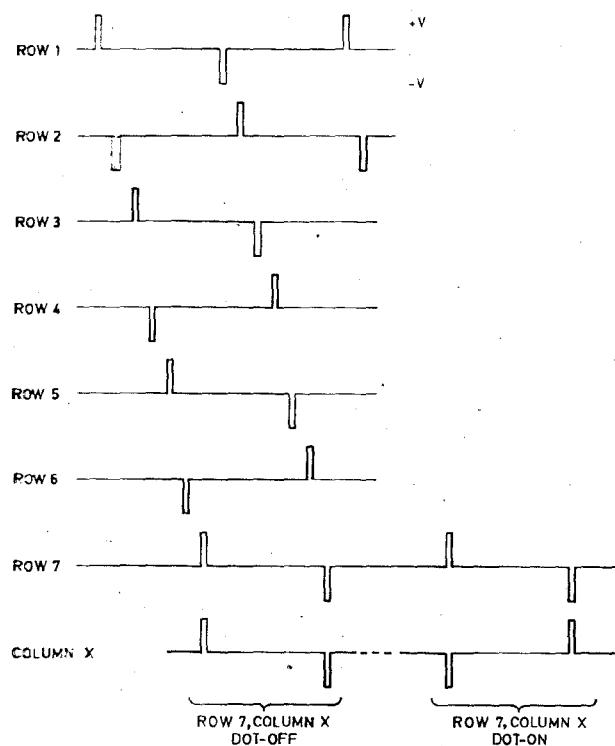


Fig.5.2.5 LCD Drive Inputs: Simplified Timing Diagram

Driving the Display

21. To drive the display, the processor sends to the column drives the data that is applicable to a particular row: it then drives that row. New column drive data is sent as each row is driven in turn.
22. The processor obtains the complete 32 characters of column data from a look-up table in the ROM; it temporarily stores the data in the RAM. The processor then outputs a 5-bit column character, using an Output 4 instruction which sets the N2 line high. N2 high sets the column register ML25 for a parallel load operation (pin 9 high), and N2 gates TPB via AND gate ML12a to load the five column-character bits into the register. The high output from AND gate ML12a also latches the three bits of row-number data through the row latches, ML24.
23. The 5-clock-group counter ML7 counts Disp Data Clk pulses, which enter the board via connector pin E3. When the display-output-latching signal (from AND gate ML12a) is removed from the counters input (pin 15), the counter starts counting. Bistable ML13b is set on receipt of the first count, thus allowing subsequent pulses via AND gate ML12c and OR gate ML5a to clock the five bits of column data serially out from the column register, ML25. At the sixth count, the 5-clock-group counter inhibits itself and resets its associated bistable, thus terminating the clock pulses to ML25.
24. The five column bits go via switch ML20c (which acts as a level shifter), to display drive ML29 where they are clocked-in serially via pin 2 by the same 5-clock group that clocked them out from the column register. (The clock pulses to pin 39 of all display drive registers also go via a level shifter, ML20b.)
25. The display drivers, ML29, ML30, ML31, ML32, ML33 are 32-bit static shift registers with true/complement outputs; connected serially they form a 160-bit register. Display data is loaded in serially, five bits at a time until the column drive data for a complete 32-character row is stored.
26. To produce a.c. signals across the display, the processor outputs a status bit which is latched through to the Q1 output (pin 7) of ML19. This goes to the True/Complementary control inputs of the column drives. When the T/C input (pin 1) is low, the column bits are output in their true states, when the T/C input is high, the column bits are output in inverted states. The Q1 output also goes to switch ML20a where it switches either +ve or -ve drive through to the common input (pin 3) of row demultiplexer ML23. Each time a block of row data is output to the display drives the sense of the Q1 output is reversed. Because the number of rows scanned is odd (seven), on successive scans the sense of the control line is reversed for any particular row, thus producing an over-all a.c. waveform. The changing T/C inputs to the column drives achieve the same effect for the column signals. See Figure 5.2.5.
27. The positive and negative voltage levels used by the LCD and drives are produced by the display drive voltage generator (Paragraph 31); all control and data signals to these devices are converted to the required levels by level shifters (digitally-controlled analogue switches) ML20, ML27.

28. While the column data is being loaded into the display drive shift registers ML29 to ML33, the processor inhibits the row drive by making its Q output (pin 4) low. While the input to pin 11 of switch ML27b is high (this is set by the processor, as described in Paragraph 37), the Q signal goes via the switch and, inverted by inverter ML18d to high, inhibits the row demultiplexer. The output lines from the row demultiplexer to the display are pulled-up to mid-rail voltage (via RML2), thus ensuring that there is no d.c. across the LCD. The Q output from the processor is made high, when the column data has been loaded, to enable the selected row output.
29. To accommodate certain types of LCD, if link LK1 is fitted, the processor is able to remove all drive voltages from the LCD by setting the Q6 (pin 15) output from ML26 low. This goes to switch ML27a where it switches the outputs of column voltage generators ML14 and ML16 to mid-rail. The low Q6 output also goes to switch ML27b to force an inhibit on the row demultiplexer ML23 (regardless of the level of the Q signal from the processor), so the row drives to the LCD are pulled-up to mid-rail voltage (via RML2) and there is no voltage across the LCD.
30. If link LK2 is fitted instead of LK1, the display columns are permanently driven, except when Reset 2, which enters the board via connector pin E5, is high. Reset 2 high makes the output from exclusive OR gate ML34a low, thus causing switch ML27a to remove the column drive voltages (as in Paragraph 29). The low ML34a output also goes via switch ML27b and inverter ML18d to inhibit the row demultiplexer outputs (as in Paragraph 29).

DISPLAY DRIVE VOLTAGE GENERATION

31. The drive voltages used by the LCD display are generated by the circuits consisting of ML28, ML14, ML15 and ML16, and TR1, TR2, with their associated components. Voltage V_M is the mid-point between +5 V and - V_c which is a temperature compensated reference voltage. V_{DR} and V_{SR} are generated symmetrically about V_M .
32. Reference voltage - V_c is generated by the temperature compensated reference generator circuit using ML28. Variations in temperature are sensed by four diodes D4, D5, D6 and D7, connected between the +5 V rail and the non-inverting input of operational amplifier, ML28. Temperature compensation is of the order of 70 mV/ $^{\circ}C$. Initial setting-up of - V_c is by potentiometer R8.
33. Voltage - V_c is used as the negative voltage rail and +5 V as the positive rail for a resistor network (R10 to R13) that provides the inputs for the V_{DR} , V_M and V_{SR} drive circuits. Each drive circuit consists of an operational amplifier, with extra drive provided for the V_{DR} and V_{SR} rails by transistors TR1 and TR2 respectively.
34. Switch ML27a, when closed, shorts-out resistors R11 and R12 and causes the V_{DR} , V_{SR} rail generators to go to the mid-rail voltage, V_M .

BACKLIGHT OPERATION

35. When the LIGHT key on the keyboard is pressed, the Light signal, which enters the board via connector pin Q14, goes low. This signal, inverted by inverter ML18a, goes to the EFI input (pin 24) of the processor. The processor, on sensing that the LIGHT key has been pressed, latches a high bit through the D0 input of status latch ML19, (it 'writes' via the data bus, to the address allocated to ML19 in the memory map (Table 1)), making the Q0 output high and the Q0 output low; these outputs enable oscillator ML21, ML22, TR4, TR5, which produces a 60 V r.m.s., 400 Hz (approximately) sinewave via transformer T1 to drive the backlight.
36. The Q0 output of ML19 is also routed to the base of transistor TR3 where it is used to control the brightness of the status LEDs. Current for these indicators is provided via emitter follower TR3. The transistor is held switched-on by the base bias provided by resistor R21 to 0 V; when the Q0 output of ML19 goes high it increases the base voltage of TR3 and therefore the emitter voltage, thus reducing the amount of current through an activated LED. Consequently, the brightness of the LED is reduced.

LED INDICATORS

37. The LED indicators D15 to 19 are controlled by the output of status latch ML26. The processor sends the appropriate LED status to ML26 by 'writing' (via the data bus) to the address allocated to ML26 in the memory map (Table 1). An LED is on when its associated ML26 output is high. The POWER LED, D20 is driven by a combination of the Charge (Q2) and Batt Lo (Q3) outputs from status latch ML19. The POWER LED has three possible states, as follows:
 - (1) ON: when the MA 4248 is connected to an external supply, V_{EXT} and is charging.
 - (2) OFF: when the MA 4248 is not connected to V_{EXT} and a battery low condition does not exist, or V_{EXT} is connected but charging is not occurring (eg. battery has fully charged; no battery fitted).
 - (3) FLASHING: when the MA 4248 is not connected to V_{EXT} and a battery-low condition exists.
38. When the battery is in a state of low charge, Batt Lo (Q3) is low, and if Charge (Q2) is high (not charging) the output of AND gate ML12d is low. With D13 reverse-biased at the same time as D4, the oscillator formed by ML18f, R22 and C10 runs and causes the POWER LED to flash at approximately 2 Hz.
39. When the unit is connected to a V_{EXT} supply and the unit is charging, the Charge (Q2) output from ML19 is low, which holds the input of ML18f low (regardless of the state of Q3). The high output from ML18f makes the POWER LED on. The termination of charging causes Q2 to go high and reverse-bias D13. With Q2 high and Q3 high (battery not low), the output of ML12d is high, D14 is forward biased and the input to ML18f is held high. As a result the POWER LED is off.

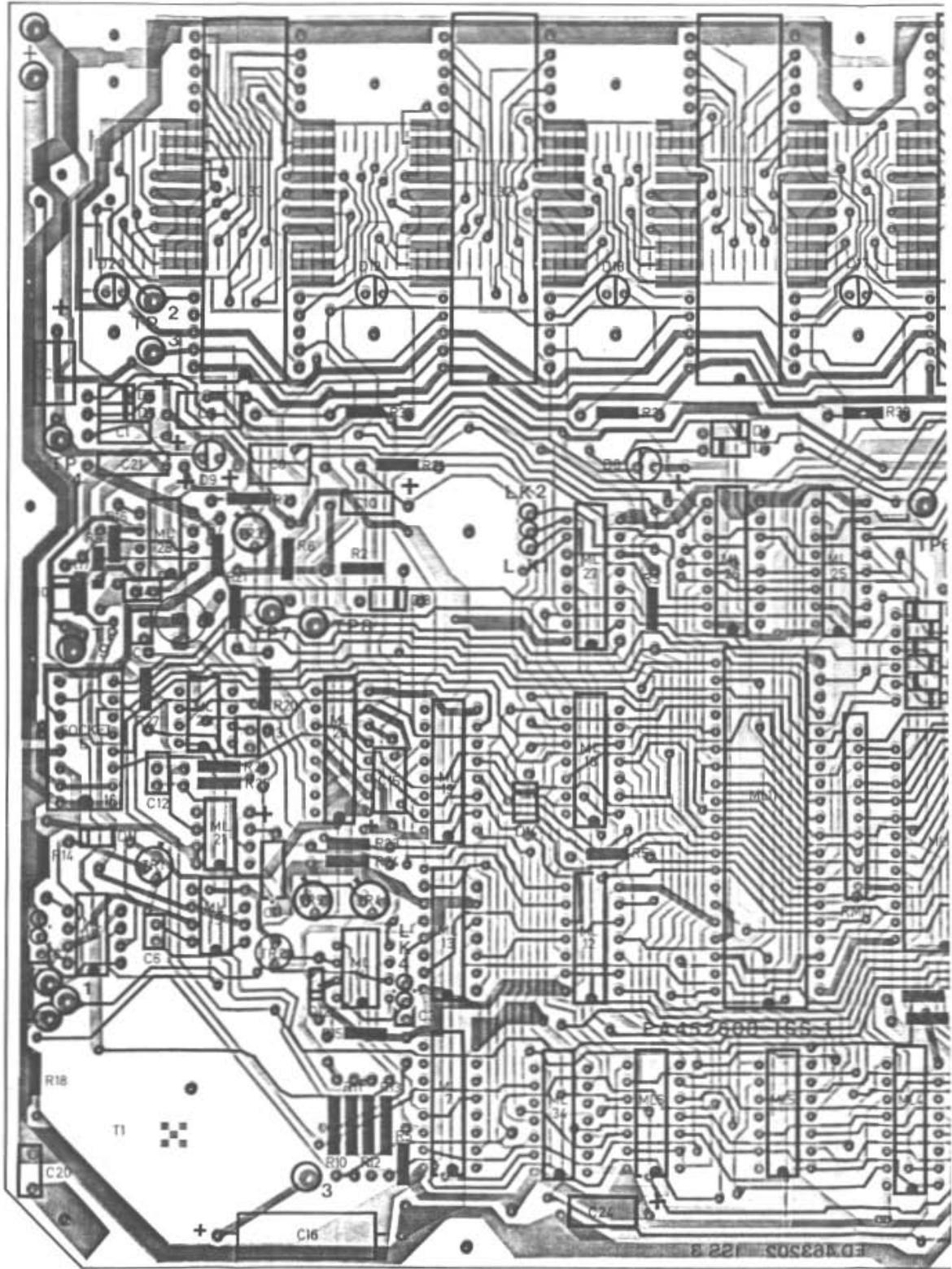
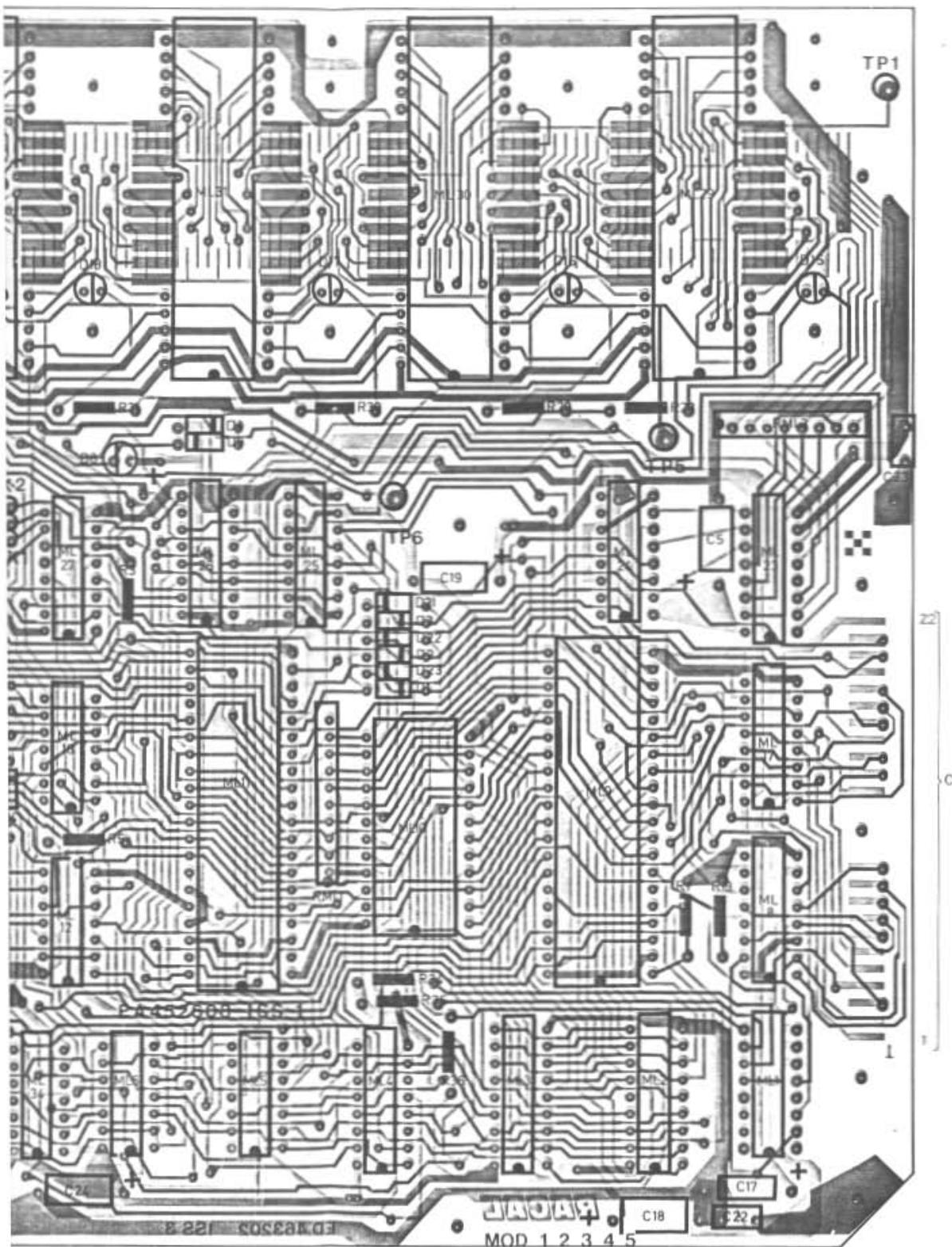
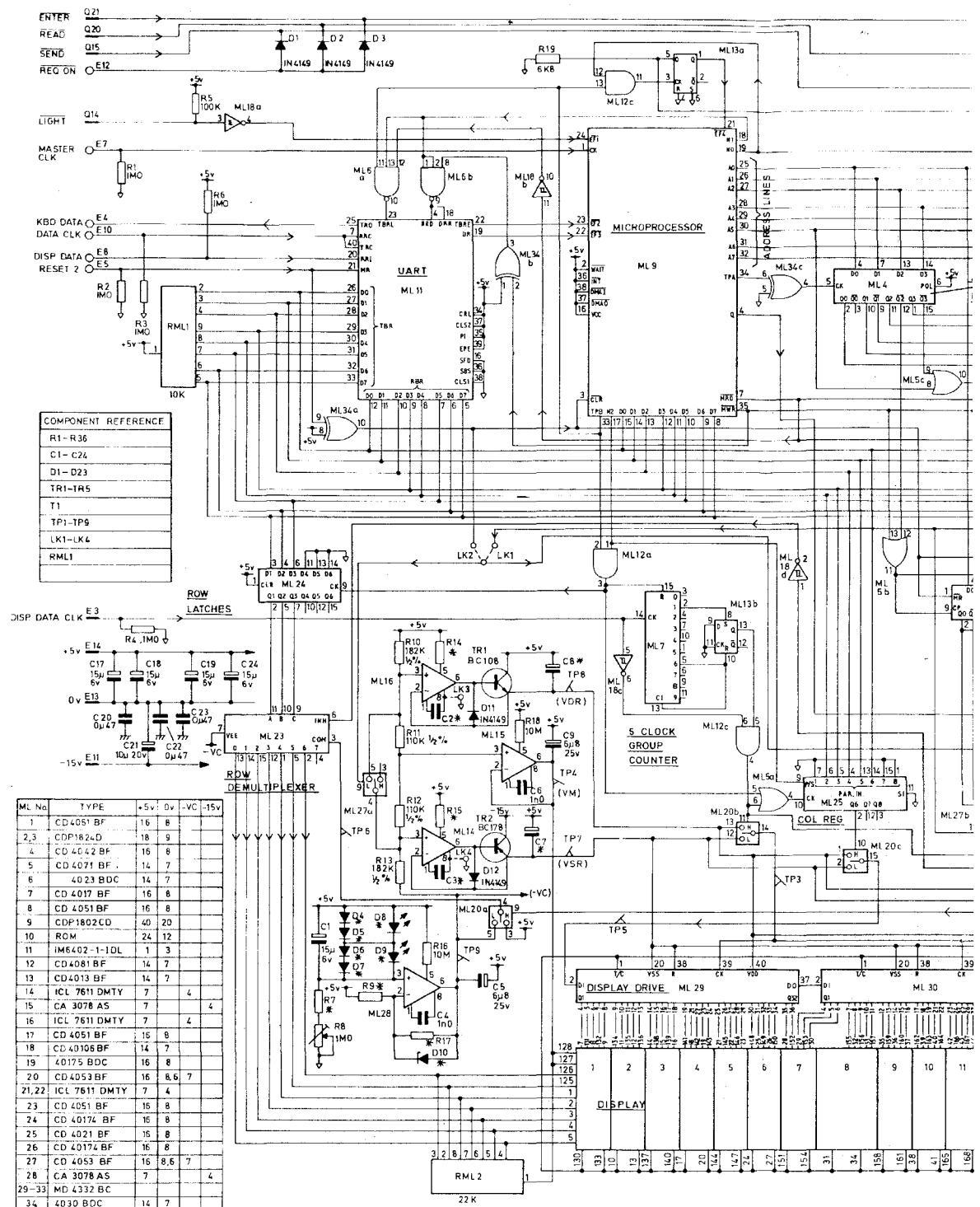


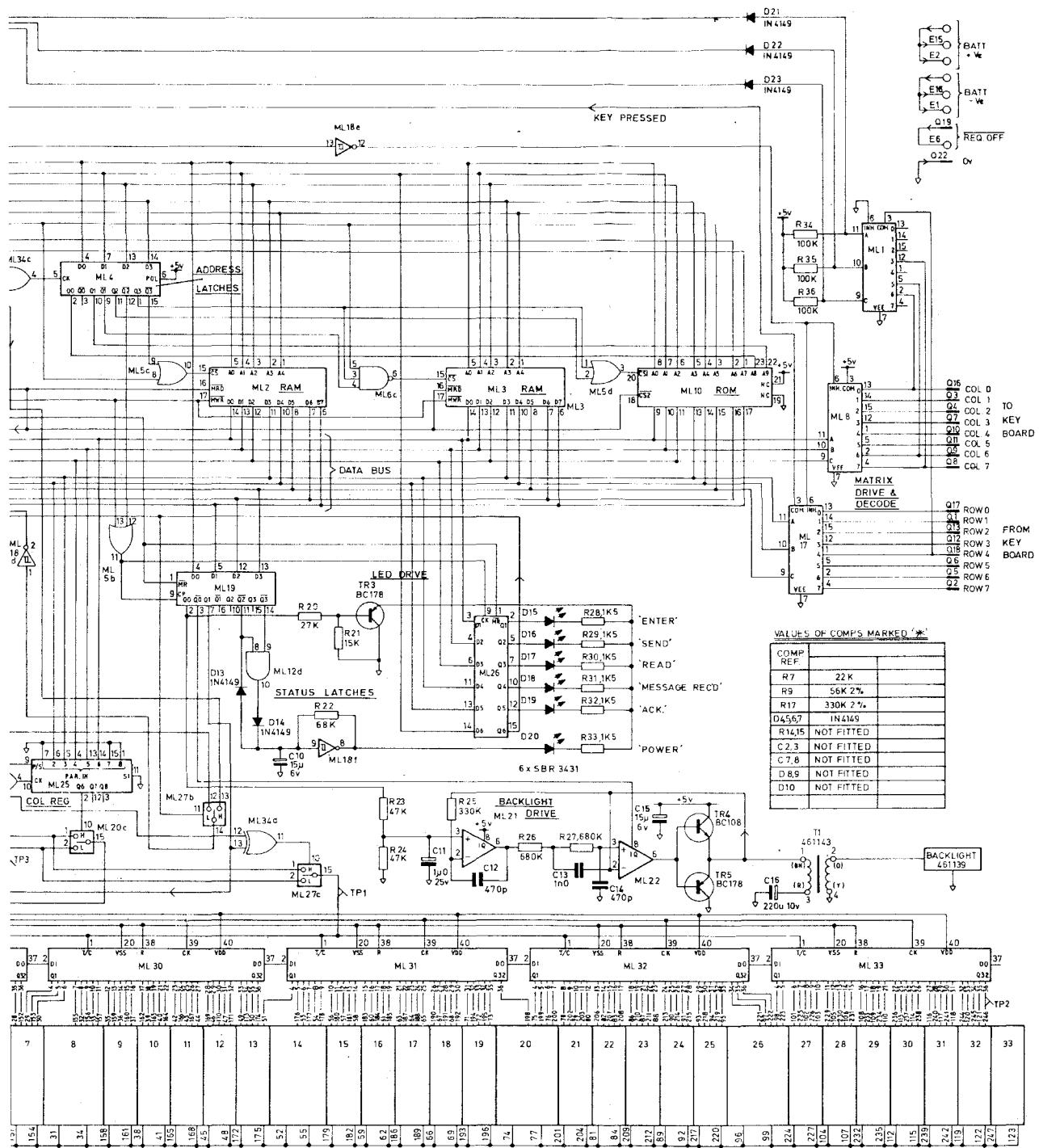
Fig.5.2.6 Man/Machine Interface Board (452608): Layout



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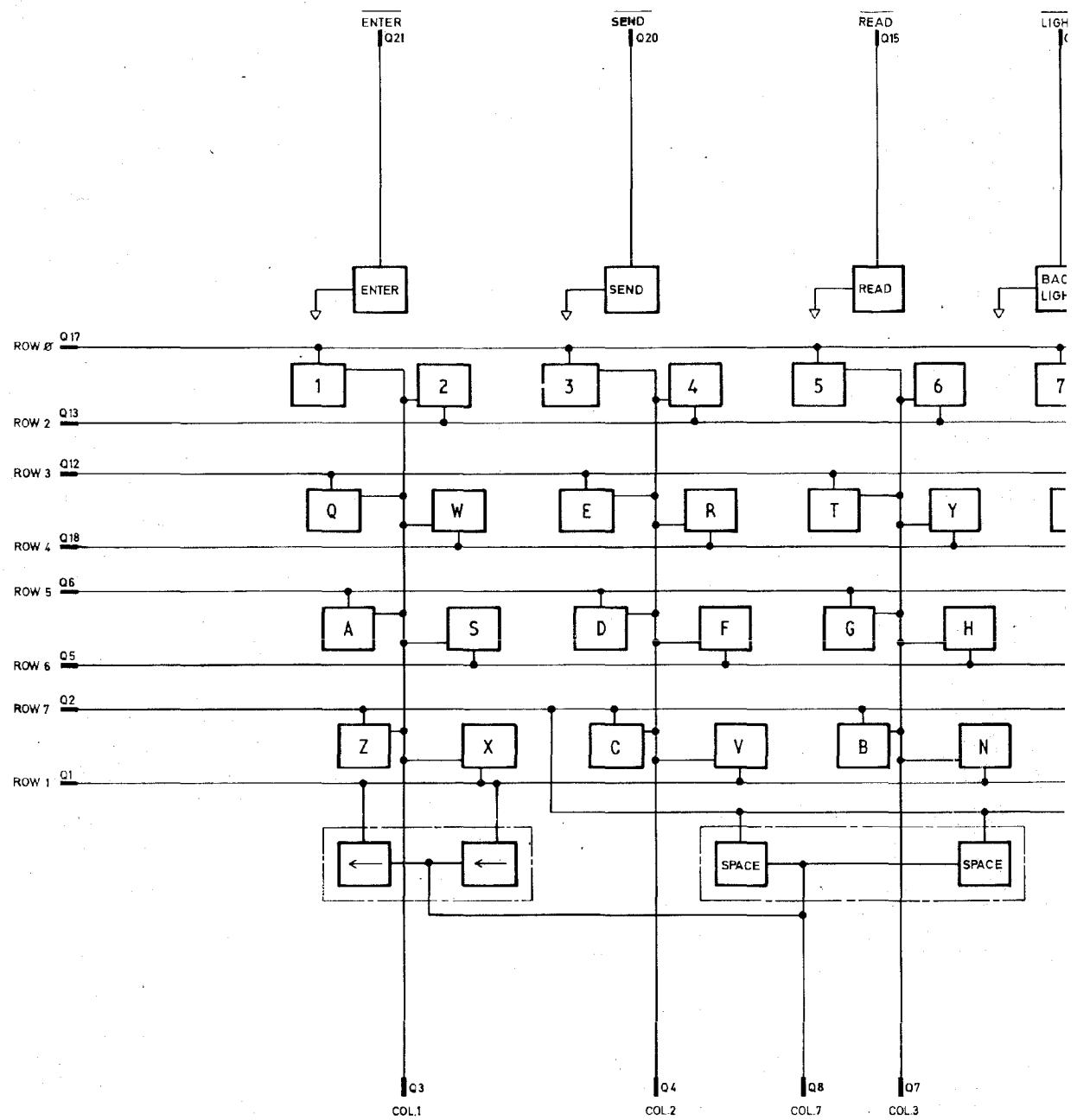
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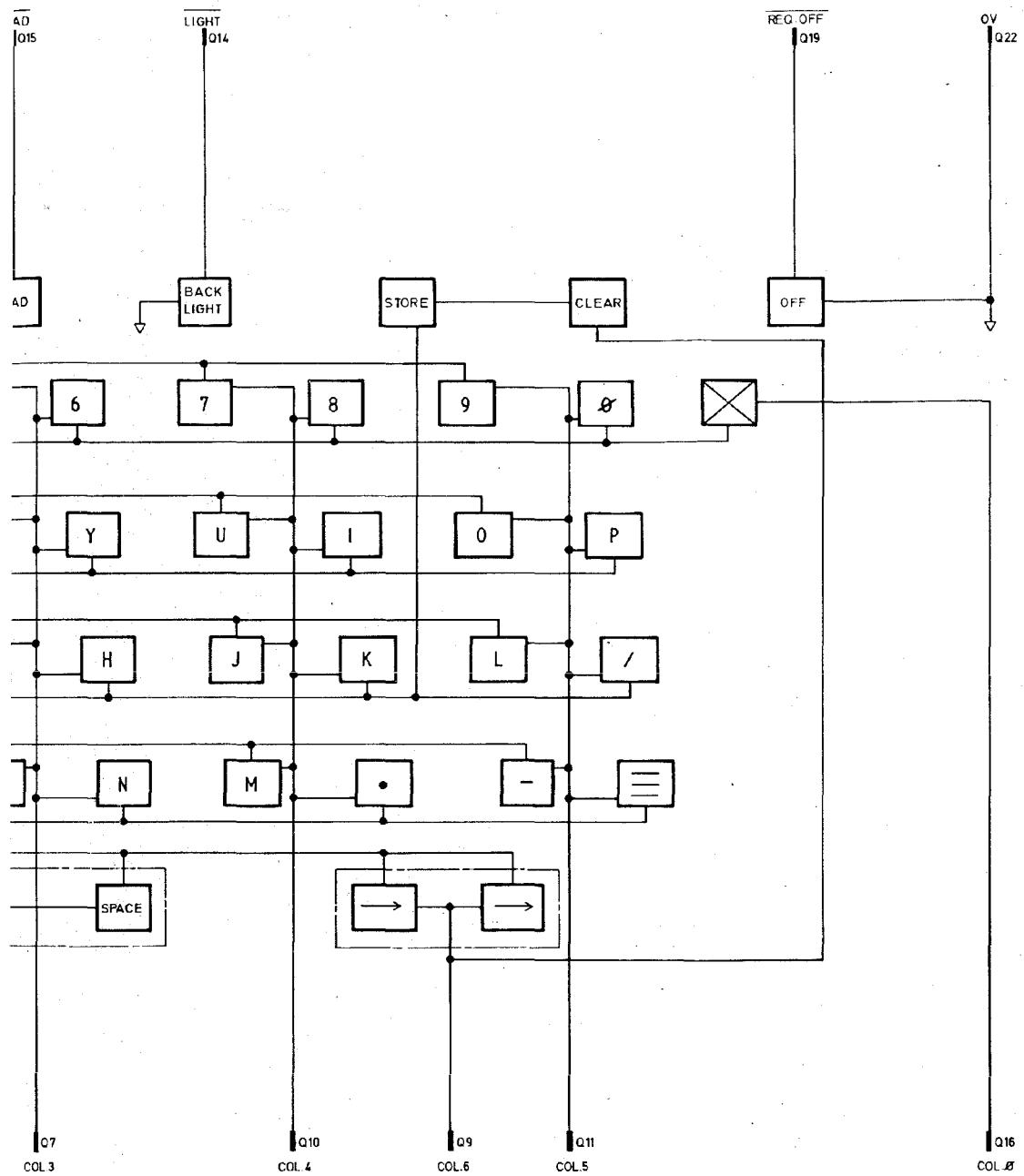




Man/Machine Interface Board(452608):Circuit

Fig.5.2.7





Keyboard (452609): Circuit

Fig.5.2.8

CHAPTER 3

SYNCHRONOUS INPUT/OUTPUT BOARD - 452606

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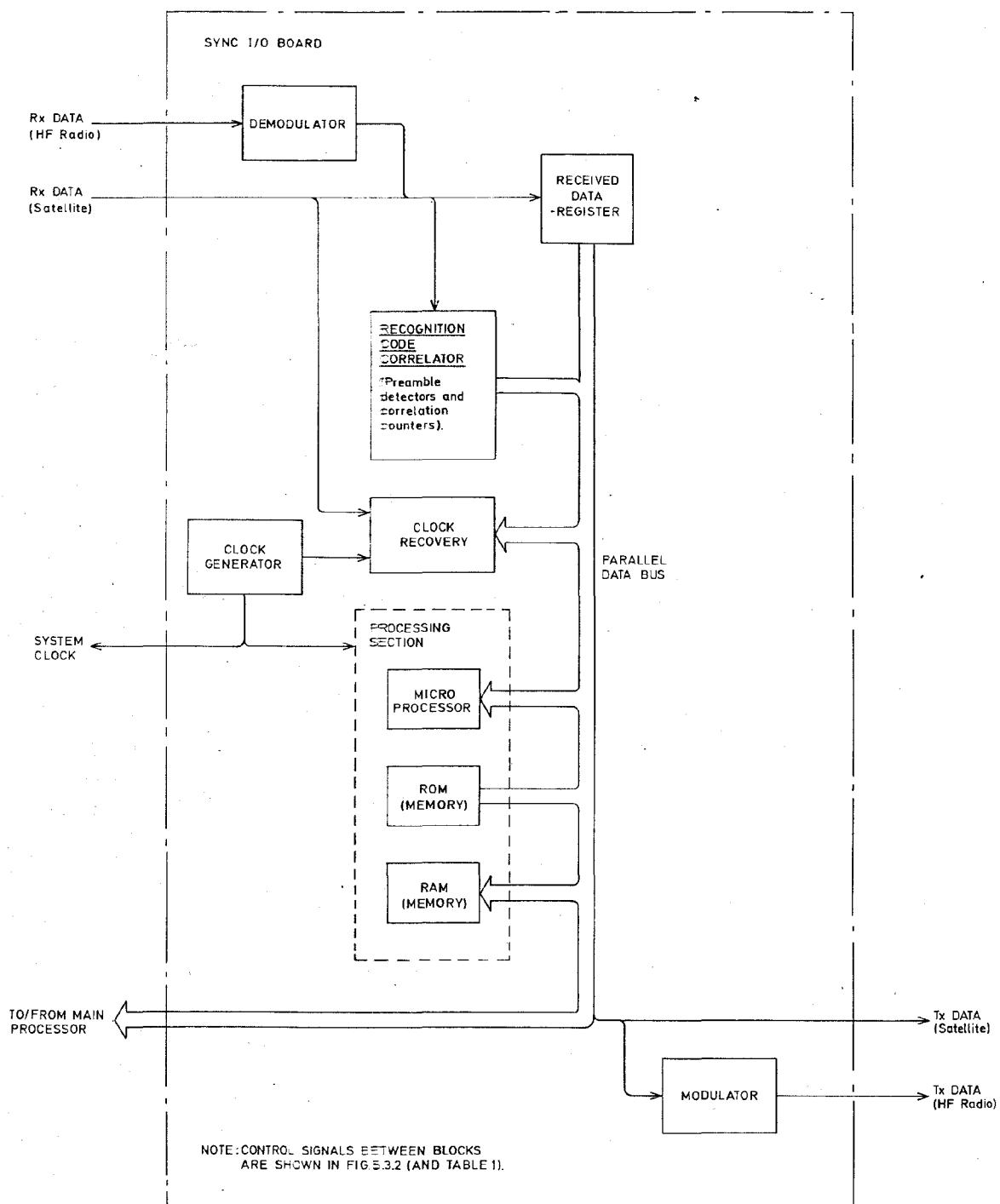


Fig.5.3.1

Sync I/O Board:
Simplified Block Diagram

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CHAPTER 3

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SYNCHRONOUS INPUT/OUTPUT BOARD - 452606

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GENERAL

1. The Synchronous Input/Output Board 452606 provides an interface between the main processor and the external communication system; the circuit is shown in Figure 5.3.5. The board contains the following functions:
 - (1) Microprocessor, which controls received message identification and acceptance, message transmission, and data transfer to/from the Main Processor Board.
 - (2) Clock generator, which produces all the clock signals required by the board.
 - (3) Working storage for the processor during execution of routines (in RAM).
 - (5) Recognition code correlator: preamble detectors and counters that detect presence of received message and establish bit-centre clocking.
 - (6) Clock recovery: continuous check that received data is being clocked at bit centre.
 - (7) Received data register, which accepts serial received data and outputs it as required to the microprocessor.
 - (8) Modem: FSK modulator and demodulator for HF radio use.

THE PROCESSING SECTION

Brief Description

2. Microprocessor ML32 is the same as the processor described in Chapter 2, but with some additional control inputs and outputs used, as shown in Figure 5.3.2 and Table 1.
3. The basic timing signal for the microprocessor is provided by crystal XL1, bit rate generator ML9 and associated components (Paragraph 4). The processor's program is stored in 1k ROM ML38 and the working store is 32 x 8-bit RAM ML37.

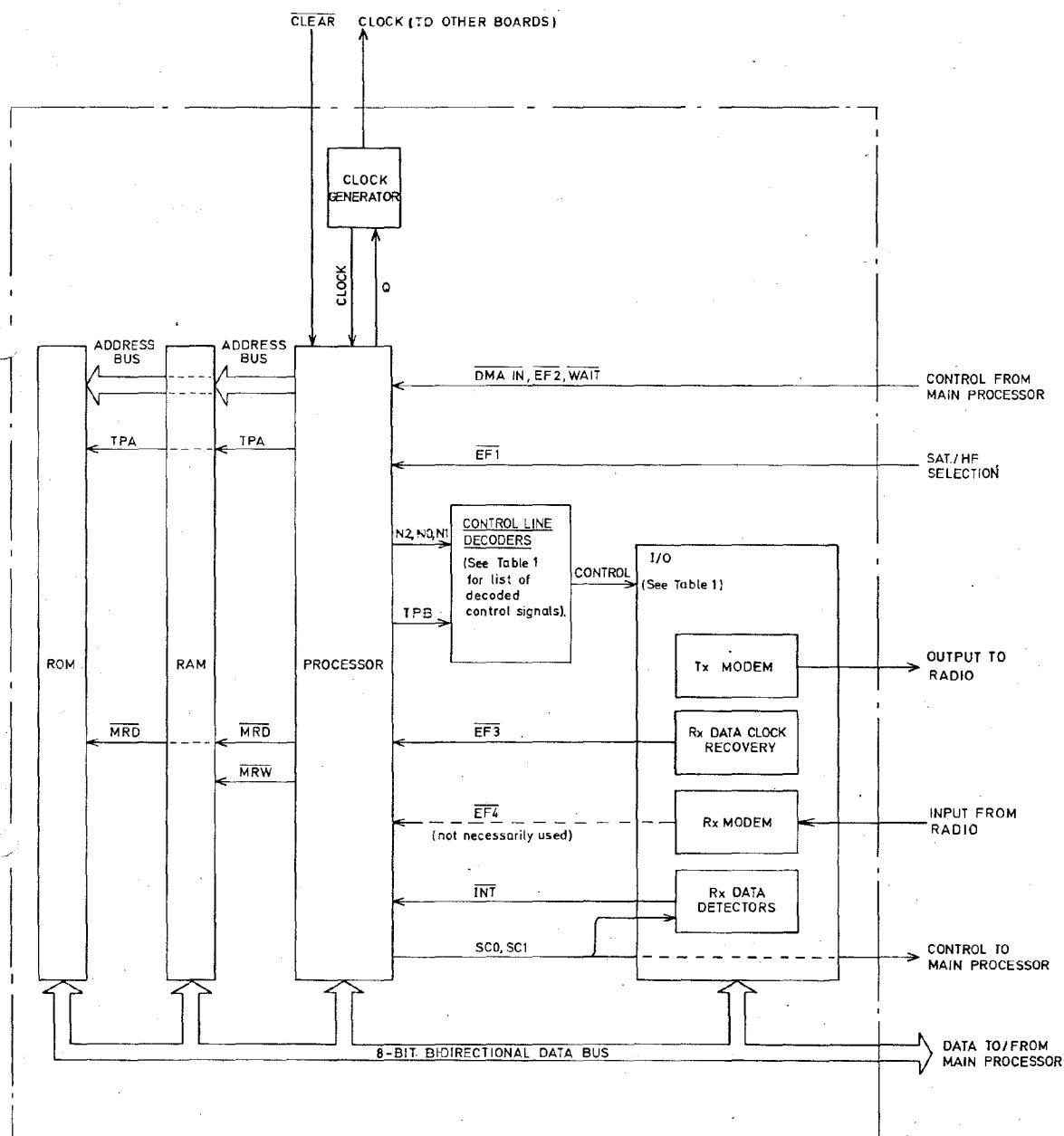


Fig.5.3.2 Simplified Block Diagram of Processing Section used on Sync I/O Board

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TABLE 1 DIRECT COMMAND SIGNALS TO/FROM THE MICROPROCESSOR

Signal	Use	Description In Handbook									
<u>Inputs</u>											
EF1	Selects satellite or HF radio operation.	Paragraph 10									
EF2	Data Input Enable: external device (off-board) ready for data via bus.	Paragraph 25									
EF3	Data rate clock (recovered from Rx Data).	Paragraph 21									
EF4	Data received (can be used to allow processor to monitor the received data).	Not used									
Int	Interrupts processor to inform it that the board has correlator data for the processor	Paragraph 16									
DMA In	Direct Memory Access control line to store data from the Main Processor independantly of processor control.	Paragraph 28									
<table border="1"> <tr> <th>Clear</th> <th>Wait</th> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>			Clear	Wait	0	1	1	0	1	1	
Clear	Wait										
0	1										
1	0										
1	1										
<table border="1"> <tr> <th>SC0</th> <th>SC1</th> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>			SC0	SC1	0	1	1	1			
SC0	SC1										
0	1										
1	1										
<u>Outputs</u>											
<table border="1"> <tr> <td>Q</td> <td>In satellite operation, alters bit rate clock from 300 to 1200 baud.</td> <td>Paragraph 27</td> </tr> </table>			Q	In satellite operation, alters bit rate clock from 300 to 1200 baud.	Paragraph 27						
Q	In satellite operation, alters bit rate clock from 300 to 1200 baud.	Paragraph 27									
<table border="1"> <tr> <td>SC0</td> <td>SC1</td> <td></td> </tr> <tr> <td>0</td> <td>1</td> <td>Carrying out DMA action.</td> </tr> <tr> <td>1</td> <td>1</td> <td>During Interrupt cycle, resets interrupt-request logic.</td> </tr> </table>			SC0	SC1		0	1	Carrying out DMA action.	1	1	During Interrupt cycle, resets interrupt-request logic.
SC0	SC1										
0	1	Carrying out DMA action.									
1	1	During Interrupt cycle, resets interrupt-request logic.									

TABLE 1 (Cont'd)

Signal	Use			Description In Handbook
<u>ML30 decoded outputs</u>				
Instruction	N2	N0	N1	
Output 1	0 0	0 0	0 1	Not used Output to Postamble register (loading)
Output 2	0	1	0	Output TX data via ML20a
Output 3	0	1	1	Output to status register ML34
Output 4	1	0	0	Output to Allcall and Selcall registers (loading)
Output 5	1	0	1	Output to load count into ML16 to centre clock on Rx data
Output 6	1	1	0	Strobe to load clock-centering count into ML15
Output 7	1	1	1	Output to main processor
<u>ML31 decoded outputs</u>				
Instruction	N2	N0	N1	
Input 1	0 0	0 0	0 1	Not used Input Allcall/Postamble correlation counter value
Input 4	0 0 1	1 1	0 1	Not used Not used Input Selcall correlation counter value
Input 5	1	0	1	Input received data register contents, and clock data edges for clock-recovery purposes
	1	1	0	Not used
	1	1	1	Not used

TIMING GENERATOR

4. Basic timing signals are produced by 2.4576 MHz crystal oscillator XL1 which, with bit rate generator ML9, produces the various clock signals used by the board. The 2.4576 MHz output from pin 9 of the bit rate generator goes to the clock input (pin 1) of processor ML32, and it leaves the board as Clock via connector pin M1. The Q0 output from pin 1 of ML9 is a clock at 1.2288 MHz, used by the data detection circuits when sampling at sixteen times the data rate.
5. The Z output from pin 10 of the bit rate generator is 8 x Bit Rate Clock, used by the preamble correlators and clock recovery circuit. The Z output varies according to the bit rate selected by the S0, S1, S2, S3 inputs (pins 14, 13, 12, 11 respectively). The basic bit rate is set for 266 baud (HF radio; the Sat signal to S1 is low), or 300 baud (satellite; Sat high); the processor can set the rate to 1200 baud (Q low) for high-speed satellite communication (Paragraph 27). (The Z output is 16 x the bit rate selected; because an 8 x bit rate signal is required, the bit rate selection inputs S0, S1, S2, S3 are set to select half the required bit rate).

LOADING SELCALL & ALLCALL PREAMBLES AND POSTAMBLER

6. The Selcall preamble is stored in 64-bit shift register ML23c, the Allcall preamble in ML23b, and the Postamble in ML23a. To load the Selcall preamble into ML23c, the processor outputs a status character to ML34 with an Output 3 instruction (N0, N1 high and N2 low and hence ML30 pin 7 high). The status character latched into ML34 has bit 1 set high to signal a correlation load status. This sets ML34 pin 5 (Q2) high; the high output goes to switch ML12c where it switches the data bus bit 0 line through to shift register ML23c. The processor then outputs the Selcall bits on the data bus bit 0 line, one bit at a time using an Output 4 instruction (N2 high)), and clocks them into the register by using the Q1 (pin 14) output from control line decoder ML30 as a clocking signal via switch ML12a.
7. The Allcall preamble is loaded at the same time as the Selcall preamble; the Allcall bits are placed on the data bus bit 1 line.
8. The Postamble is loaded in a similar manner (to Paragraph 6), the processor performing an Output 1 instruction (N0 high); the data bus bit 0 line is used for the Postamble bits, which are clocked into ML23a by the Q2 (pin 2) output of the control line decoder.
9. When the registers have been loaded (i.e. load signals are removed from the associated switches), the register outputs are fed back, via the switches, to their inputs.

MA 4248

MESSAGE ENTRY AND READ-OUT DEVICE (MEROD)

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PART 1 GENERAL

CHAPTER 1 GENERAL DESCRIPTION

PART 2 SPECIFICATION

CHAPTER 1 TECHNICAL SPECIFICATION

PART 3 INSTALLATION

CHAPTER 1 UNPACKING
CHAPTER 2 OPTION SETTING
CHAPTER 3 INTERFACE

PART 4 OPERATION

CHAPTER 1 CONTROLS AND INDICATORS
CHAPTER 2 OPERATING INSTRUCTIONS

PART 5 TECHNICAL DESCRIPTION

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CHAPTER 2 MAN/MACHINE INTERFACE BOARD (and Keyboard)
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CHAPTER 4 MAIN PROCESSOR BOARD
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PART 6 MAINTENANCE

CHAPTER 1 MAINTENANCE
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MA 4248

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CHAPTER 1

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GENERAL DESCRIPTION

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ILLUSTRATIONS

Fig. No.

- 1.1.1 MA 4248: General View
- 1.1.2 MA 4248: Construction

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End of Chapter



Fig.1.1.1

MA 4248: General View

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The MA 4248 Message Entry and Read-Out Device (MEROD) is a portable message terminal, with alpha-numeric keyboard and display, which can be connected to either an HF radio link or a digital radio link. It uses burst transmissions, to reduce transmission time compared with normal voice transmissions, and a built-in error-protection facility increases communications reliability.

OPERATION

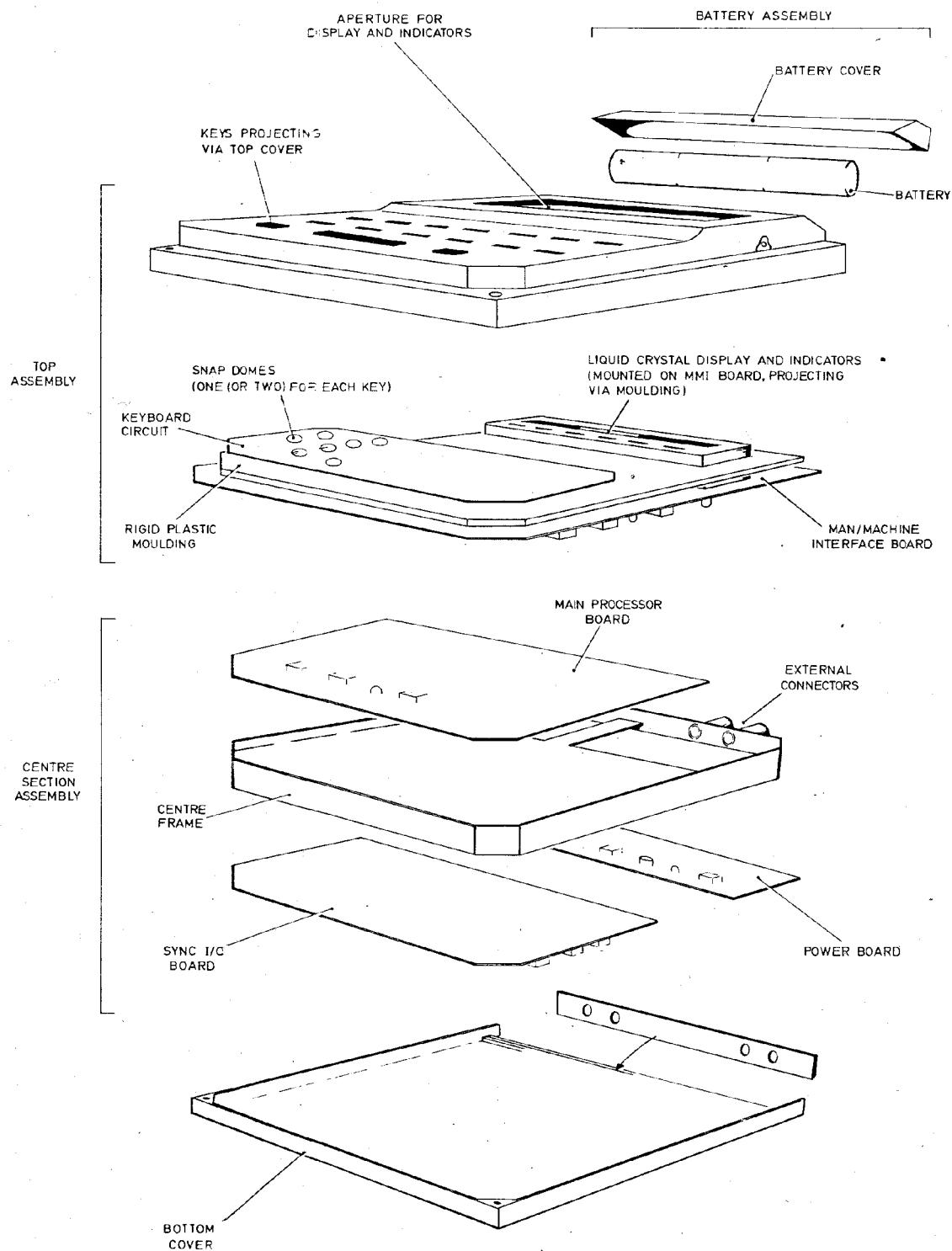
2. The operator enters a message of up to 1000 characters via the standard full-size keyboard. During entry, the message is displayed on the liquid crystal dot-matrix display, and it is stored until required for transmission. The unit has a full editing capability and the message may be entered in either free-format or fixed-format. In fixed format preparation, the message is entered, part at a time, in response to a series of prompts or titles that automatically appear on the display. The prompts are not sent with the data: the receiver inserts any that are required.
3. The operator selects the address of the equipment that is to receive the message (the message may be addressed to one particular receiver or all receivers in a network), and presses a key to send the message. The equipment automatically adds a synchronising preamble and postamble (for use by receiving equipment), and converts the data to the required form for transmission. If working with an HF radio, the MA 4248 uses a built-in FSK modem so the unit can be plugged directly into the handset socket of the radio. If operating with a digital radio, the unit sends and receives digital data (for details, see the Specification, Part 2, Chapter 1).
and messages transmitted
4. Received messages (i.e. messages addressed to the particular unit) can be printed on an external printer. The received messages may be stored in the unit (up to eight messages can be stored provided the total length does not exceed 2000 characters); an indicator informs the operator when a message has been received: the operator can then read the stored message on the display. The unit can be set to automatically erase messages after printing.

5. Various operating options may be selected by the operator. Using the keyboard, in response to prompts on the display, the operator selects:
 - (1) High or low speed operation over digital links.
 - (2) Store and print received messages, or print-only.
 - (3) Free-format or fixed-format message entry.
 - (4) Accept or mask received messages that contain residual errors.
 - (5) The address of the unit.
 - (6) The address to which a message is to be sent.
 6. For details of the accept or mask received errors option, see Part 5, Chapter 1, Paragraph 18.
 7. The internal working of the unit is described in the Principles of Operation, Part 5, Chapter 1.
- CONSTRUCTION
8. The MA 4248 is housed in a rectangular alloy casting, which is sealed and should not be opened during normal operations. Operator's controls (standard keyboard plus function keys) and indicators (alpha-numeric display plus status indicators) are on the top of the unit; external connections are via three of four sockets on the rear of the unit (one for HF radio, one for satellite radio, one for printer (the other is not used)).
 9. Logic components (mainly CMOS) are mounted on four printed circuit boards. Three boards have microprocessors which control the specific functions that the boards perform; thick film hybrids are used for the modem section. From top to bottom the unit consists of: top cover assembly, centre section assembly, and base cover; the battery assembly is fitted at the rear of the top cover. (See Figure 1.1.2).
 10. The top cover has apertures through which the keys and display panel project. The keys are raised parts of a flexible keysheet moulding: when a key is pressed it bears down on a snap dome on the Keyboard circuit. (See Figure 1.1.2). The Keyboard circuit is mounted on a rigid plastic moulding, below which is mounted the Man/Machine Interface Board with its component side facing downwards. The Man/Machine Interface Board scans the keyboard to detect pressed keys, and drives the display (and indicators). The liquid crystal (LCD) and indicators are mounted on the upper side of the Man/Machine Interface Board and project up via apertures in the plastic moulding.
 11. Connections between the two printed circuit boards are via elastomeric connectors located in apertures in the plastic moulding; when the two boards are secure in situ, the contacts in the flexible connectors press on to the appropriate connection pads on the boards. The Man/Machine Interface Board also has a flat ribbon cable connection to the Power Board. This connects the top assembly to the centre section: the cable is sufficiently long for the two parts to be separated for maintenance purposes.

12. The centre section has the Main Processor Board (which controls the overall functioning of the unit) mounted in the top part of the frame, with components facing upwards. The lower part of the centre section is occupied by the Synchronous Input/Output Board (which converts logic signals to/from the form used by the external equipment), and the Power Board (which distributes power and converts the levels of signals to/from the external equipment). The Sync I/O Board is at the front of the section, with component facing downwards; the Power Board is at the rear, with components facing upwards (through cut-outs in the frame).
13. Connections between the boards on the centre section are made via elastomeric connectors (through the frame). In addition, the Power Board has a connector for the ribbon cable from the top assembly (para. 11); and soldered wire connections to the battery-charge transistors mounted on the frame and to the external connectors, which are fixed to the rear of the frame (with RF decoupling capacitors fitted directly to the earthed rings of the connectors).
14. The top cover fits over the top of the centre section, the bottom of the centre section fits inside the base cover. The unit is sealed by combined RF and weather gaskets between the top cover and centre section, and the centre section and base. A hole in the side of the top cover allows testing of the seal to be carried out. (In normal operation, the hole is sealed by a screw).

CONNECTION TO SYSTEM

15. A single plug-in cable connects the MA 4248 to the handset connector of an HF radio or the data connector of a satellite/digital input radio. If a printer is used, a single plug-in cable connects it to the unit. The cables are supplied to suit the particular system used.
16. Power is provided from the radio, if it has a suitable external supply output, via the single cable that connects the radio to the MA 4248; or it can be supplied from another source via the HF radio socket or satellite radio socket that is not already being used to carry signals between the unit and the radio; or it is provided by the battery in the unit. When an external supply is used the internal battery is automatically charged; when the internal battery is used for operation, battery charging is necessary whenever the POWER indicator flashes.



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MA4248 : Construction

Fig.1.1.2

CHAPTER 1

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TECHNICAL SPECIFICATION

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CHAPTER 1

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TECHNICAL SPECIFICATION

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GENERAL

1. (1) Message Preparation Off-line, with full editing.
- (2) Transmission High-speed synchronous data.
- (3) Selective addressing Up to 63 individually-addressed units, and one general-broadcast address.

OPERATOR'S INTERFACE

2. (1) Message entry Conventional QWERTY keyboard.
- (2) Controls Seven mode and control keys.
- (3) Display 32-character, single-row, dot-matrix liquid crystal display. It displays:
 - (a) Prompts (instructions & warnings) to operator.
 - (b) Message entered into transmit store.
 - (c) Received messages (unless print-only has been selected and printer is connected).
- (4) Status indicators Six LEDs.

MESSAGE STORE

3. (1) Transmit store One message, up to 1000 characters.
- (2) Receive store Up to 8 messages, provided the total does not exceed 2000 characters.

SELECTIVE ADDRESSING

4. Up to 63 individually-addressed units and one Allcall (broadcast) address. Unit's own address and destinations of messages are entered via the keyboard.

TRANSMISSION FORMAT

5. (1) Each message consists of (a) Phase reversals.
(b) Preamble.
(c) Message.
(d) Postamble.
- (2) Phase reversals Allow for transmitter start-up and receiver AGC.
- (3) Preamble Pseudo random sequence dependent upon the address to which the message is transmitted. Probability of correct recognition: 98% in a 1-in-12 error rate.
- (4) Message Up to 1000 six-bit characters plus error-correction code parity bits. Message bits interleaved to message depth to randomise effects of burst errors.
- (5) Postamble 64 bit pseudo-random sequence.

ERROR CORRECTION

6. Message protected by a powerful forward error correcting algorithm. Probability of correct reception of a 1000-character message in a 1-in-100 error rate is 99.64%. Error detection gives a probability of 99.98% that all residual errors will be detected irrespective of error conditions.

FORMAT AND INTERFACE FOR HF RADIO

- 7.
- | | |
|-----------------------|--|
| (1) Phase reversals | 0.5 or 1.0 seconds duration, depending on preset option (internal link). |
| (2) Message preamble | 64 bits. |
| (3) Transmission rate | 266 baud. |
| (4) Information rate | 160 baud. |
| (5) Modulation | Wide-shift FSK (frequency shift keying), 1303 Hz, 2100 Hz. |
| (6) Demodulation | Tones detected independently to achieve in-band diversity. |
| (7) Tone output level | 2.5 mV or 25 mV rms from 50 ohms, selected by preset option (internal). Balanced or unbalanced output. |
| (8) Tone input level | 10 mV to 2 V rms into 56 kohms. Unbalanced. |
| (9) PTT | Contact-closure to ground. Max in-rush current 450 mA. Max open-contact voltage 100 V. |

FORMAT AND INTERFACE FOR SLOW-SPEED SATELLITE/DIGITAL RADIO

- 8.
- | | |
|---------------------------------|--|
| (1) Phase reversals | 2.1 seconds duration. |
| (2) Message preamble | 82 bits. |
| (3) Transmission rate | 300 baud. |
| (4) Information rate | 180 baud. |
| (5) Data output levels | MIL STD 188-114, unbalanced, current-limited at 40mA. |
| (6) Data input levels | MIL STD 188-114, balanced or unbalanced. |
| (7) Satellite/digital selection | Ground Sat pin on connector (22 kohm input impedance). (Otherwise HF is selected). |
| (8) Receive data sense | Unit detects inverted data and automatically corrects it. |
| (9) Receive data rate | Unit automatically detects high or low speed operation independently of transmit speed selected. |

FORMAT AND INTERFACE FOR HIGH-SPEED SATELLITE/DIGITAL RADIO

- | | |
|---------------------------------|--|
| (1) Phase reversals | 0.5 second duration. |
| (2) Message preamble | 64 bits at 300 baud followed by 64 bits at 1200 baud. |
| (3) Transmission rate | 1200 baud. |
| (4) Information rate | 730 baud. |
| (5) Data output levels | MIL STD 188-114, unbalanced, current-limited at 40mA. |
| (6) Data input levels | MIL STD 188-114, balanced or unbalanced. |
| (7) Satellite/digital selection | Ground Sat pin on connector (22 kohm input impedance). (Otherwise HF is selected). |
| (8) Receive data sense | Unit detects inverted data and automatically corrects it. |
| (9) Receive data rate | Unit automatically detects high or low speed operation independently of transmit speed selected. |

FORMAT AND INTERFACE FOR PRINTER

- | | | |
|-----|-------------------------|---|
| 10. | (1) Data output format | Asynchronous 5-bit ITA 2 code (Baudot). |
| | (2) Data output rate | Selected by preset option (internal links). (See Table 3 in Part 5, Chapter 4 for typical list of rates). |
| | (3) Output levels | MIL STD 188-14, current-limited to 40mA; or 5 V CMOS (for use with MA 4233 Printer), max current 0.5mA. |
| | (4) Clear-To-Send | Ground to request data (22 kohm input impedance). |
| | (5) Mark/Space polarity | Output data can be inverted (preset option: wire link). |

POWER REQUIREMENTS

11. (1) Battery not fitted 11 V (d.c. - peak ripple) minimum,
 32 V (d.c. + peak ripple) maximum,
 200mA maximum.

(2) Battery fitted As (1) when battery fully charged.

(3) Battery charging As (1), but 1A pulsed.

MECHANICAL SPECIFICATION

- | | | |
|-----|-----------------|---|
| 12. | (1) Enclosure | Sealed, fully-immersible, RFI screened, light-weight cast-alloy case. |
| | (2) Dimensions: | Height
Width
Depth |
| | | 64 mm.
230 mm.
230 mm. |
| | (3) Weight | 3.25 kg (including main battery). |

ENVIRONMENTAL SPECIFICATION

13. (1) Operating temperature range -20⁰C to +55⁰C.
(2) Storage temperature -40 to +55⁰C
(3) Vibration MIL STD 810C requirements for loose and secure cargo.
(4) EMI MIL STD 461A requirements for ground-based terminals.
(5) Sealing MIL STD 810C requirements for ground and airborne equipment in respect of humidity, altitude, rain, immersion.

CHAPTER 1

UNPACKING

CONTENTS

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MA 4248

Part 3
Chapter 1
Contents

CHAPTER 1

=====

UNPACKING

=====

GENERAL

1. The MA 4248 is supplied in a polystyrene shock-resistant transit package.
 - (1) Remove the unit from the transit package.
 - (2) Inspect the unit for possible damage caused during shipment.
 - (3) Check that the contents of the transit package are complete as detailed on the packing slip/advice note.
 - (4) Before installation, check that the details of the preset option links are correct for the system (see Chapter 2).

CHAPTER 2

=====

OPTION SETTING

=====

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CHAPTER 2

OPTION SETTING

GENERAL

1. A number of wire links inside the unit allow it to be configured to suit the requirements of a particular system. The links are set, during manufacture, to the user's requirements. The version number, shown on the rear of the unit, further defines the equipment, and details are given in an appendix (as necessary).

OPTIONS

2. The links that are concerned with preset user options are on stand-off pins. Their uses are listed in Paragraphs 3, 4 and 5.

When Used with HF Radio

3.
 - (1) Phase reversals at the start of a message may be 0.5 second duration, with link LK4 fitted on the Main Processor Board; or 1.0 second duration with no link. (Part 5, Chapter 4, Paragraph 23).
 - (2) Demodulation of the FSK signal from the radio uses a fixed-reference when link LK2 is fitted on the Sync I/O Board; it uses an adaptive threshold when there is no link. (Part 5, Chapter 3, Paragraph 37).
 - (3) The output level of the FSK tone to the radio is 25 mV when R13 and R14 on the Sync I/O Board are 270 ohms; the level is 2.5 mV when the resistors are 2k7 ohms. (Part 5, Chapter 3, Paragraph 33).

When Used with Satellite/Digital-Input Radio

4.
 - (1) Inverted data is sent to the satellite/digital-input radio when LK1 on the Sync I/O Board is present; true data (i.e. uninverted) is sent when there is no link. (Part 5, Chapter 3, Paragraph 30).

When Used with Printer

5.
 - (1) The speed of the data output to the printer is set by a combination of links LK10, LK11, LK12, LK13 on the Main Processor Board. See Table 3 in Part 5, Chapter 4 for the various speeds and link settings.
 - (2) True data (i.e. uninverted) is sent to the printer when link LK2 on the Main Processor Board is present; inverted data is sent when link LK3 is present instead. (Part 5, Chapter 4, Paragraph 39).
 - (3) A parity bit is added by the UART to the data output to the printer when link LK6 on the Main Processor Board is present; when link LK7 is present instead, the UART does not use parity. (Part 5, Chapter 4, Paragraph 41).

OTHER LINKS

6. Other links shown in the circuit diagrams do not concern the user.

CHAPTER 3

INTERFACE

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Fig. No.

3.3.1 MA 4248: Rear Connectors

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MA 4248

Part 3
Chapter 3
Contents

CHAPTER 3

=====

INTERFACE

=====

GENERAL

1. The functions of the 'pins' (socket-contacts) in the three connectors SKB, SKC, SKD on the rear of the MA 4248 are shown in Tables 1, 2, 3; the fourth connectors, SKA, is not used.

TABLE 1 FUNCTIONS OF PINS IN SKB, PRINTER CONNECTOR

Function	Pin	Notes
Printer Data	A	Data to printer; data rate selected by internal links, MIL STD 188-114 levels. Current-limited at 40 mA.
5 V Data	E	Data, as for pin A, but at 5 V CMOS levels, 0.5 mA max current (e.g. for an MA 4233 Miniature Printer).
CTS	C	Clear to send, grounded by printer when ready to receive data. 22 kohm input impedance.
V ext	B	External supply 11 to 32 V (d.c. + ripple) max; approx. 200 mA when unit is operating (1 A for charging if battery is fitted).
0 V	D	Ground.

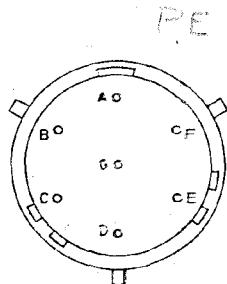
TABLE 2 FUNCTIONS OF PINS IN SKC, SATELLITE/DIGITAL - INPUT RADIO CONNECTOR

Function	Pin	Notes
Data Out	C	Data to radio, at 300 or 1200 baud.
Data In	F	Data from radio, at MIL STD 188-114 levels.
Data In Gnd	G	Balanced data input; grounded for unbalanced operation.
Sat	E	Grounded to set unit for operation through this connector (i.e. SKC). 22 kohm input impedance.
V ext	B	External supply; same as in Table 1.
0 V	D	Ground.

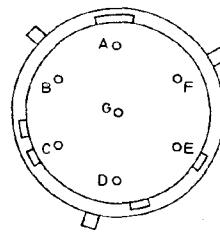
TABLE 3 FUNCTIONS OF PINS IN SKD, HF RADIO CONNECTOR

Function	Pin	Notes
Tone Out	A	FSK signal to radio, 2.5 mV or 25 mV rms (set internally) from 50 ohms.
Bal Tone Out	G	Inverted Tone Out signal. Grounded for unbalanced operation.
PTT	C	Contact closure to ground when transmitting. Maximum inrush current 450 mA, maximum open-circuit voltage 100 V.
Tone In	F	10 mV to 2 V rms input from radio, input impedance 56k ohms.
V ext	B	External supply; same as in Table 1.
0 V	D	Ground.

*cable
452838*



SKC: SATELLITE RADIO
SKD: HF RADIO



SKB: PRINTER

Cable 452743

Fig.3.3.1 MA4248: Rear Connectors

CHAPTER 1

CONTROLS AND INDICATORS

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Fig. 4.1.1

MA 4248 : Controls and Indicators

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CHAPTER 1

CONTROLS AND INDICATORS

GENERAL

1. The MA 4248 is controlled by a 51-key keyboard with an associated 32-character display. Six LED indicators provide status information. The functions of the controls and indicators are listed in Tables 1 and 2.

TABLE 1 CONTROL FUNCTIONS

Control	Function
39 alpha-numeric and punctuation keys	Used to enter messages into the transmit memory, and to select formats and addresses.
☒ (delete key)	Causes the character appearing over the cursor line to be deleted (when unit is in applicable mode).
≡ (new-line key)	Actions a selection (as called-for by prompts on the display). Can be used in free-format text as carriage-return line-feed to printer.
Space bar	Inserts a space into the part of the message indicated by the cursor point (when unit is in applicable mode).
← (left key) → (right key)	Permit a displayed message to be scrolled left or right across the display. A momentary depression of either key causes the message to be stepped by one character position; when a key is held down the message is block-scrolled 12 characters every two seconds.
ENTER key	Selects the Enter mode to allow unit set-up, or allows access to the transmit memory (to allow message entry). Also, switches-on the MA 4248 if external power is not connected (if battery is fitted).

SEND key	Selects the Send mode. Causes the instruction SELECT ADDRESS to appear on the display to prime the operator to enter the address of the unit that is to receive the message. Also, switches-on the MA 4248 if external power is not connected (if battery is fitted).
READ key	Allows access to the read memory. The first depression of the key causes the first 32 characters of the first received message to appear on the display. Subsequent depressions of the key cause subsequent messages to be displayed. Also, switches-on the MA 4248 if external power is not connected (if battery is fitted).
STORE key } CLEAR key }	Pressed simultaneously to clear a displayed message from the memory.
OFF key	Switches-off the unit (if an external power supply is not connected).
LIGHT key	Activates the display backlight. The light remains on for 10 seconds after the last keyboard entry. When the display backlight is on, the status LEDs are dimmed (to prevent dazzling).
32-Character display	Allows inspection of the messages in the memory, provides editing facility using the cursor (^—), and displays prompts and status information.

TABLE 2 STATUS INDICATOR FUNCTIONS

Indicator	Function
ENTER	Unit is in the Enter mode, and the operator has access to the transmit memory.
SEND	Unit is in the Send Mode.
READ	Unit is in the Read Mode, and the operator has access to the receive memory.
MSG RCD	A received message has been entered into the receive memory.
ACK	Not used.
POWER	If battery is fitted: Flashes when battery is in low state of charge; on continuously while battery is charging. If battery is not fitted: On when external power is connected.

CHAPTER 2

OPERATING INSTRUCTIONS

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CHAPTER 2

OPERATING INSTRUCTIONS

SWITCHING-ON

1. Connect external power to the MA 4248, or, if a battery is fitted, press one of the ENTER, SEND or READ keys. The unit responds with SELF TEST COMPLETE UNIT O.K., or, if the self-test routine has failed, the unit provides an error indication, as shown in Table 1. (If the unit displays LAST 5 CHAR GROUP INCOMPLETE, complete or erase the message in the transmit store as applicable (Paragraph 15), switch off, then on. The unit should respond with SELF TEST COMPLETE UNIT O.K.).

TABLE 1 MA 4248 SELF-TEST ERROR MESSAGES

Message	Meaning
ERROR 1	Main Processor module not running
ERROR 2	Main Processor memory (RAM) fail
ERROR 3	Main Processor/MMI link failure
ERROR 4	MMI memory failure
ERROR 5	Sync I/O module not running
ERROR 6	Sync I/O memory fail

SETTING-UP OPERATIONAL OPTIONS

2. Press ENTER
The unit displays
SELECT FORMAT: \emptyset \gg \equiv
Press \emptyset
The unit displays
SELECT FORMAT: \emptyset \gg \equiv
Press \equiv

Note: Ensure MA 4233 is switched on otherwise Format \emptyset will be incomplete.
3. The unit enters the set-up mode, displaying either
LOW SPEED \equiv OR HIGH=1
or
HIGH SPEED \equiv OR LOW=0

(1) If the required satellite/digital radio operating speed is shown at the left of the display, press \equiv
(2) If the required speed is not shown at the left, press the character that is shown at the right of the display (i.e. 1 or \emptyset as applicable), then press \equiv
(Note that the unit looks for only the characters that are specified (i.e. displayed); any other character that may be pressed is ignored).

(7)

The unit displays either

ASC II PRINTER = OR BAUDOT

If the required mode = Ø

(5)

The unit displays either

AUTO ACK = OR NO ACK Ø

If the required mode - -

ONCE ONLY

6. The unit displays either
STORE & PRINT OR PRINT ONLY=1
or
PRINT ONLY OR STORE & PRINT=0

- (1) If the required mode is shown at the left, press \equiv
- (2) If the required mode is not shown at the left, press the character that is shown at the right of the display, then press \equiv

7. The unit displays either
RX ERROR MASK OR ACCEPT=0
or
RX ERROR ACCEPT OR MASK=1

The unit may be set to either accept messages that contain remaining uncorrectable errors (these messages are preceded by a letter E), or to mask the errors with Qs (thirteen of them) inserted in place of each uncorrectable block. (See Part 5, Chapter 1, Paragraph 18).

- (1) If the required mode is shown at the left, press \equiv
- (2) If the required mode is not at the left, press the character that is shown at the right, then press \equiv

8. The unit displays either
UNIT ADDRESS = NN OR \blacksquare
Where N is an octal digit (i.e. 0 to 7).

- (1) If the unit address is correct, press \equiv
- (2) To change the last digit of the address, press \blacksquare , press the new digit, then press \equiv
- (3) To change the complete address, press \blacksquare \blacksquare , enter the new address, then press \equiv

Setting-up is complete; the unit returns to displaying the satellite operating speed (Paragraph 3). To exit from the set-up mode, press one of the ENTER, READ, SEND or OFF keys as applicable.

ENTERING A FREE-FORMAT MESSAGE

8. Press ENTER
The unit displays
SELECT FORMAT:_ 0>2, \equiv
Press 1
The unit displays
SELECT FORMAT:1 0>2, \equiv
Press \equiv
9. (1) If the transmit store is empty, the unit displays
ENTER MESSAGE
(2) If a free-format message is already in store, the unit displays the last 20 characters of this message.
(3) If a non free-format message is already in store, the unit displays
CLEAR TRANSMIT MEMORY?

10. To erase a message from the store, press the STORE and CLEAR keys simultaneously.
11. Enter the message. The characters appear on the display, to the left of the cursor position A.
12. The message can be moved left or right past the cursor: to move the message left, press the \leftarrow key; to move the message right, press the \rightarrow key. If one of these keys is held pressed, the message is block-scrolled at a rate of 12 characters every 2 seconds; this allows fast reviewing of the message.
13. To edit (alter) a message, set the character to be changed over the flat part of the cursor, press \blacksquare , then press the new character required.
14. To exit from this mode press one of the ENTER, READ, SEND or OFF keys.

ENTERING A 5-CHARACTER-GROUP MESSAGE

15. Press ENTER
The unit displays
SELECT FORMAT: _ $\theta > 2, \equiv$
Press 2
The unit displays
SELECT FORMAT: 2 $\theta > 2, \equiv$
Press \equiv
16. (1) If the transmit store is empty, the unit displays
ENTER 5 CHARACTER GROUPS.
(2) If a 5-character-group message is already in store, the unit displays the last 3 blocks of the message.
(3) If a non 5-character-group message is already in store,
the unit displays
CLEAR TRANSMIT MEMORY? ✓
17. To erase a message from the store, press the STORE and CLEAR keys simultaneously.
18. Enter the message, five characters at a time. Only the 26 alphabet and 10 numeric characters can be used. After each group of five characters, press the Space Bar (to enable another group to be entered). The characters appear on the display, to the left of the cursor position A. Exit from this mode is possible only when the last group is complete. (If the unit is switched off then on, it displays LAST 5 CHAR GROUP INCOMPLETE if the last group was not completed).
19. The message can be moved left or right past the cursor: to move the message left, press the \leftarrow key; to move the message right, press the \rightarrow key. The message moves one character position for each depression of the \leftarrow or \rightarrow key.
20. To edit (alter) a message, set the character to be changed over the flat part of the cursor, then press the new character required. (Additionally, the last character of a message may be deleted, if it is over the cursor line, by pressing \blacksquare).

SENDING A MESSAGE

21. Press SEND

The unit displays

SELECT ADDRESS: **00>77,≡**

Enter the address of the unit to which the message
is to be sent; for general broadcast enter 00.

The unit displays

SELECT ADDRESS: NN **00>77≡**

To send the message, press ≡

The unit displays

MESSAGE BEING TRANSMITTED

When the message has been sent, the unit displays

MESSAGE TRANSMITTED

22. If, when ≡ is pressed to send the message,
the unit displays

MESSAGE BEING PROCESSED

the unit is receiving a message and therefore
is unable to transmit.

CLEARING A MESSAGE FROM THE TRANSMIT MEMORY

23. Display the end of the message, as described in Paragraph 8 (for a free-format message) or Paragraph 15 (for a 5-character-group message).

Press the STORE and CLEAR keys simultaneously.

The unit displays

TRANSMIT MEMORY CLEARED

RECEIVING A MESSAGE

24. While the unit is switched-on, it automatically accepts any messages that are addressed to it, and all general-broadcast messages. When a complete message has been received, the unit displays

MESSAGE BEING PROCESSED

for a short time while it carries out error-correction and outputs the message to a printer (if one is connected). During this period the unit does not respond to any inputs from the keyboard or radio.

25. When processing is complete, the unit displays

RECEIVED MESSAGE IN MEMORY

MSS REC'D

and the (MESSAGE RECEIVED) indicator is on.

Any keyboard operations started before the unit began to process the received message can now be continued.

26. The unit can receive and store up to eight messages providing the total length does not exceed 2000 characters.

READING A RECEIVED MESSAGE

27. When a message is received, it is automatically printed, if a printer is connected. In the Print-Only mode, the message is not stored. In the Store and Print mode, the message is printed and stored, and the MESSAGE RECEIVED indicator is turned-on to inform the operator that a message is available for read-out on the display. In either mode, if no printer is connected, the received message is stored and the MESSAGE RECEIVED indicator is turned-on.
(If no messages in Rx Memory) - NO MESSAGES IN RX MEMORY
28. Press READ: the unit displays the first 32 characters of the first message in the memory. The message may be stepped left or right by the \leftarrow or \rightarrow key respectively; if one of these keys is held pressed, the message is block-scrolled at a rate of 12 characters every 2 seconds.
29. To read the next message, press READ: the unit displays the first 32 characters of the second message. Step or block scroll to read the message; press READ for the third message; continue until all messages (up to 8) have been read. When all messages have been read from the memory the unit displays
NO MORE MESSAGES IN READ MEMORY
(To read the first message again, press READ).

CLEARING A MESSAGE FROM THE RECEIVE MEMORY

30. Display the message, as described in Paragraphs 28 and 29.
Press STORE and CLEAR simultaneously.
The unit erases the message then displays the first 32 characters of the next message. To erase the displayed message, press STORE and CLEAR simultaneously, whereupon the next message is displayed. (The messages are moved up through the memory to fill the gap left by the cleared message). Continue as necessary, or until the unit displays
RECEIVE MEMORY CLEARED
which shows that the complete memory is cleared.

DISPLAY BACKLIGHT

31. To switch-on the display backlight, press LIGHT. The backlight remains on while keys are being pressed; it turns-off automatically when no keys have been pressed for 10 seconds. The status indicators are dimmed while the backlight is on (to prevent dazzling).

SWITCHING-OFF

32. (1) If an external power supply is connected:
Disconnect the external supply
This is the only way the unit can be switched-off when using the external supply.
32. (2) If the unit is operating from internal battery power:
Press OFF
33. Operating mode information, and messages held in the transmit and receive stores, are retained for at least 22 days when the unit is switched off.

CHAPTER 1

PRINCIPLES OF OPERATION

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ILLUSTRATIONS

Fig. No.

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- 5.1.6 MA 4248: Interconnections

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End of Chapter

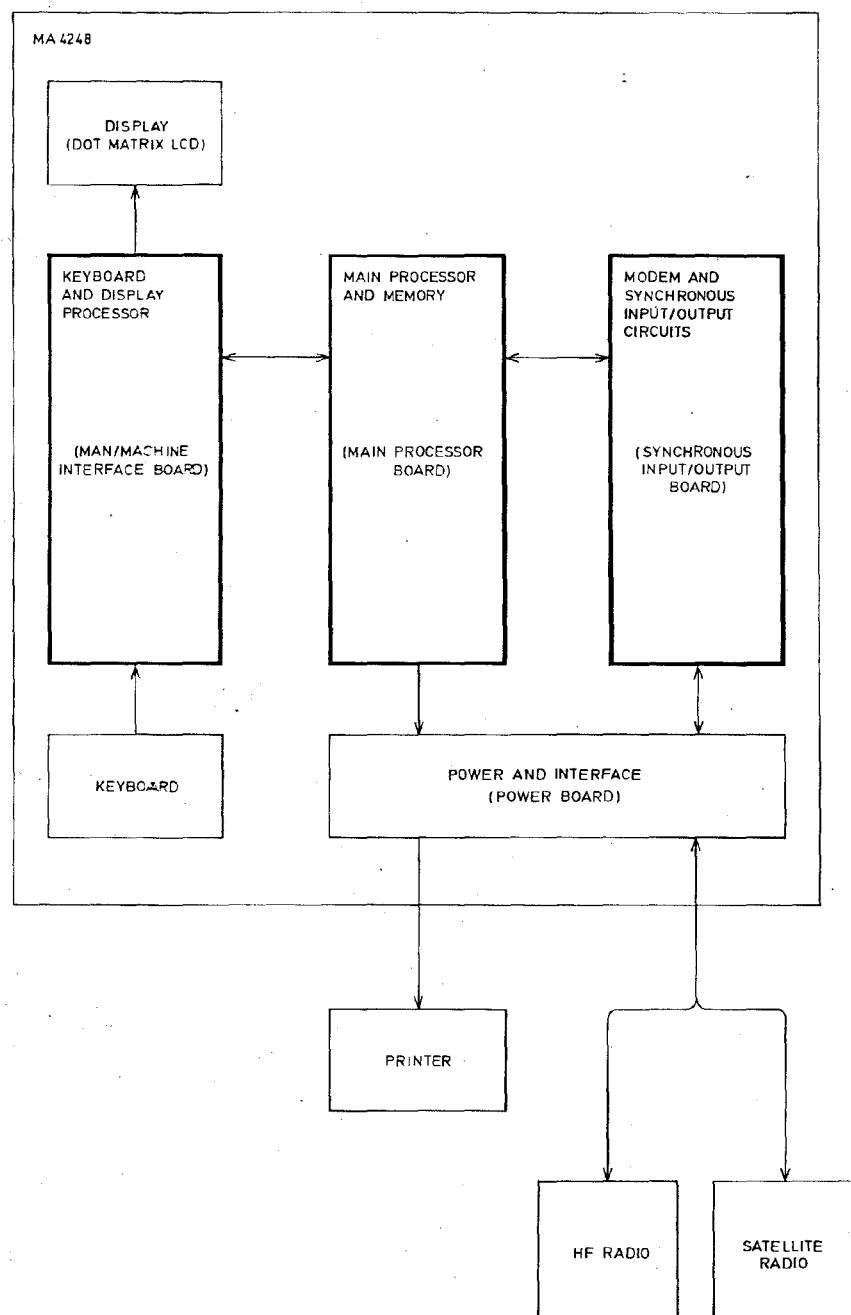


Fig.5.1.1

MA4248: Block Diagram

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CHAPTER 1

PRINCIPLES OF OPERATION

GENERAL

1. The MA 4248 consists of three main modules; each module has specific functions, and each has a microprocessor which controls the functions. The three main functions are shown in Figure 5.1.1. Details of interconnections between the modules are shown in Figure. 5.1.6.
2. Each microprocessor has a control program, stored in a read-only memory (ROM), and temporary storage space in a random-access memory (RAM). Each processor works through its program, processing information from its peripheral services (i.e. the other functions on its board) according to the instructions in the program and according to commands received from external sources (e.g. other microprocessor, or keyboard, etc). It moves data round the board via a common data bus (i.e. a shared set of lines). See Figure 5.1.2.
3. Overall control and coordination of the internal functions of the unit are provided by the microprocessor on the Main Processor Board, which also stores messages-for-transmission in a transmit memory and received-messages in a receive memory (parts of RAM). The main processor organises interleaving, and error protection/correction; also it provides prompts and status indications for the operator.
4. The unit operates in four basic operating modes:
 - (1) Enter. The keyboard is used to enter commands from the operator, and messages for storage in the transmit memory (i.e. for subsequent transmission when Send mode is selected). Keyboard inputs also set the various operating options into the main processor program; the operator presses keys in response to prompts provided on the display.
 - (2) Send. The unit formats the message from the transmit memory and outputs it to a radio transmitter.
 - (3) Receive. Occurs automatically when a message is received via the radio. The message goes to a printer and/or it is stored in the receive memory until the operator selects Read mode to view the message on the display.
 - (4) Read. The unit displays a message that has been stored in the receive memory.

Each mode of operation involves one or more of the following main functions:

- (1) Operator inputs via the KEYBOARD. (Figure 5.1.3).
- (2) DISPLAY outputs to the operator. (Figure 5.1.3).
- (3) SENDING messages to a radio transmitter. (Figure 5.1.4).
- (4) RECEIVING messages from a radio receiver. (Figure 5.1.5).

KEYBOARD

8. Messages for transmission and commands from the operator to the main processor are entered via the keyboard. The processor on the Man/Machine Interface Board scans (i.e. addresses in turn) the columns and rows of the keyboard to detect a pressed key: when a key is pressed it completes its column/row circuit and the processor recognises that the currently-addressed key is pressed. (See Figure 5.1.3).

9. The processor transfers the character denoted by the pressed key to the main processor via a serial interface controlled by a universal asynchronous receiver/transmitter (UART). If the character is a command, the main processor goes to the appropriate part of its program and carries out the relevant instructions (e.g. during option-setting, the processor sets conditions for the selected option and causes the next set of options to be displayed). If the character is part of a message for transmission, the main processor stores it in the transmit memory (where it remains until the operator initiates a Send operation). The transmit memory can hold 1000 characters; the processor sends a transmit-memory-full message to the display when the store is full.

DISPLAY

10. The display is used in most modes of operation:

- (1) At switch-on, the unit performs self-test routines and displays the result.
- (2) During option-setting, the unit displays prompts to the operator.
- (3) While a message that is to be transmitted is being entered, the unit displays the message for editing purposes.
- (4) Prior to sending a message to the radio transmitter, the unit displays a prompt which asks for the address to which the message is to be sent.
- (5) After a message has been received from the radio receiver (to indicate that a message has been stored).
- (6) The contents of the transmit memory and receive memory can be displayed for reading and erasure purposes.

11. According to the operating mode, the main processor extracts from its memory the appropriate data for display, and sends it via the serial interface to the processor on the Man/Machine Interface Board. (See Figure 5.1.3). The Man/Machine processor converts the data to display-column-drive bits, using a look-up table that is stored in part of its ROM.
12. The liquid-crystal dot-matrix display has thirty-two 5 x 7 characters: there are 160 (32 x 5) columns to be driven, and seven rows. The processor loads a set of column-drive bits into the column drives, then drives a row; it then loads another set of drive bits and drives the next row; as the rows are scanned (driven in turn), the pattern of column-drive outputs makes dots on or off as required to display the characters.

SENDING

13. To transmit a message, the operator selects the Send mode and enters the required address: 00 for a general broadcast, or the two-digit octal address of a particular receiving unit. (01 to 77 can be used; 8 and 9 may not be used). The main processor extracts the message from the transmit memory, formats the message, adds a preamble (either an Allcall or a Selcall preamble, depending on the address selected), and transfers the message by direct memory access (DMA) action via the parallel data bus to the Sync I/O Board. (See Figure 5.1.5). At the end of the message, the main processor adds a 64-bit Postamble.
14. Provided the unit is not receiving at this time, the processor on the Sync I/O Board sends a PTT signal to the radio transmitter, then outputs the data serially to the transmitter: either direct, to a satellite/digital radio; or via a modulator, to an HF radio. Data for an HF radio is converted to FSK tones (1303 Hz and 2100 Hz) by a modulator on the Sync I/O Board. If data is being received at this time, the processor warns the operator and does not send the message.

RECEIVING

15. The unit can receive messages at any time, except when the unit is actually transmitting a message, or decoding and printing on receipt of a message; receiving takes priority over all other modes (e.g. entering, editing, reading). The received signal from an HF radio is first demodulated: the FSK tones (1303 Hz and 2100 Hz) are detected independently and a corresponding digital output is produced. This Rx Data signal, or an Rx Data signal direct from a satellite radio (as applicable) goes to the recognition code correlator circuit, which looks for preambles in the incoming data. (See Figure 5.1.5).
16. The unit has 64-bit Allcall and Selcall preambles (and postamble) stored in registers. The recognition code correlator samples the received data at eight-times the data bit rate and stores the samples in eight different 64-bit stores. The contents of these stores are compared with the preambles and the number of correlations is counted. The processor on the Sync I/O Board examines the correlation counts and if a count is more than 54 (from the 64 samples examined) a preamble has been detected. This is repeated until no further successful correlations occur (theoretically there can be eight correlations), then the processor sets the bit rate clock to the centre of the data bit period by locating it one-bit from the mid-point of the correlations.

Having established the presence of a message and recovered the clock, the processor transfers the data that follows the preamble to the main processor, which corrects and formats it. The main processor then sends the data to the printer via a UART, and/or stores it in the receive memory (for subsequent display on the dot-matrix display), as required by the preset options selected by the operator during the original set-up operation.

Uncorrectable Errors

18. Uncorrectable errors are either accepted or masked, as required by the operator when selecting options, as follows:

- (1) RX ERROR ACCEPT mode: if any errors in the message are uncorrectable, the message is prefixed with the letter E.

For example: **E03 MESSAGE**
error indicator  address of sending unit

The actual error in the message may be apparent in the display/print-out, or it may not be apparent, so any message preceded by E must be suspect.

- (2) RX ERROR MASK mode: if an error is uncorrectable, the complete block of thirteen characters that contains the error is replaced by thirteen Qs.

POWER

19. Power is from either an external source or an internal battery, which takes over when external power is removed. When external power is present the battery is charged (if necessary) under the control of the main processor. Charging, regulation and voltage-low-detection circuits are on the Power Board. The battery level is monitored by a circuit on the Main Processor Board: an A/D converter produces a digital representation of the level which is read at regular intervals by the main processor.

INTERFACES

20. Signals between the unit and external equipment go via interface circuits, on the Power Board, which convert levels and provide buffering/decoupling as required.