OpenROAD – Driving Open EDA Innovation for Industrial Applications

Novel Integrated Electronics (NINE) Labs
Indian Institute of Technology Guwahati

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Jan 18, 2024

https://theopenroadproject.org

www.precisioninno.com

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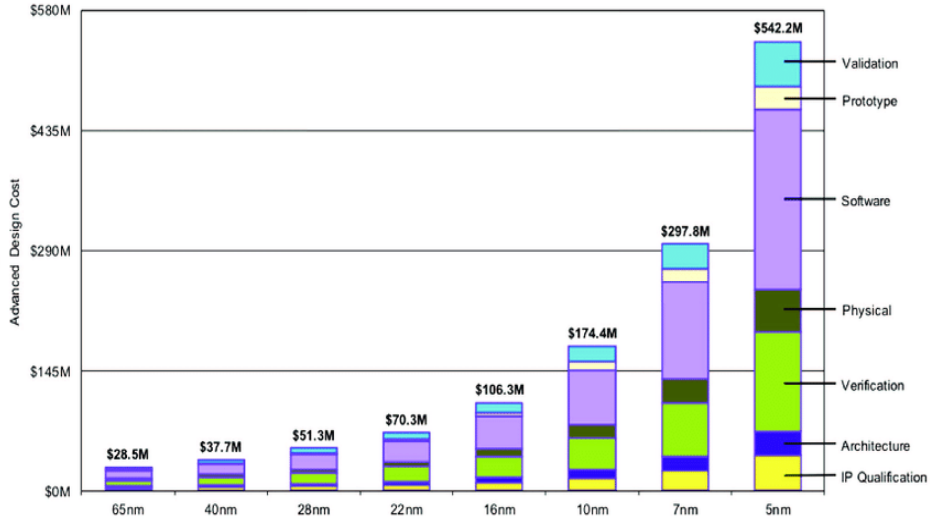
OpenROAD

Democratize IC Design and Lower Costs of IC design

- Mission: Democratize IC Design, Lower costs and Boost Innovation at Scale
- OpenROAD was funded by DARPA in 2018 within the Electronics Resurgence Initiative- ERI
  - UCSD is the prime with other universities and industry collaborators
  - University Collaboration: University of Michigan, University Minnesota, ASU
  - Early Industry partners: Arm, Qualcomm
  - **Precision Innovations** is the key Industrial developer of OpenROAD providing ongoing development, customer support and outreach
- Google is a major sponsor for OpenROAD and has supported several open MPW shuttles

OpenROAD : Low cost and Rapid Innovation

- **Directly attack the crises of hardware design and Innovation**
  - Chip design costs > 19x over the past 2 decades
  - Software development and licensing costs dominate overall design costs
- **Break down barriers:** cost, access, expertise, risk
  - Schedule: RTL-to-GDS in 24 hours
  - Expertise: No-human-in-loop, autonomous
  - Cost: permissive open source (**runs in 24 hours**)



Design software costs dominate total cost of design
source SIA

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About Precision Innovations

Company/Team Overview

- Principal industrial developer and integrator of the OpenROAD RTL to GDS ASIC/SoC Development solution
- Founded 2019
- Electronic Design Automation (EDA) veterans – 10 employees / contractors
- HQ – San Diego, CA.

History

- DARPA award for OpenROAD
- Key customers – Google and Intel
- Partners - Siemens and GlobalFoundries

Technology Overview

- OpenROAD is an EDA solution for hardware implementation of ASIC and SoC chips
- Proven (600+ tapeouts), open source, physical design solution.
- Used on designs down to 12nm
- Core competency: RTL-to-GDS EDA flows leveraging AI/ML for design space exploration and automated design implementation
- AI based Autotuner to maximize results
- Fast estimation / new design feasibility analysis
- Professional Support Solutions available.

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Making OpenROAD ready for the Indutry

- **For design SoC and ASIC design teams, who value time to market and who are not on the bleeding edge nodes, OpenROAD provides an open source, no-human-in-the-loop, 24-hour chip place and route solution**

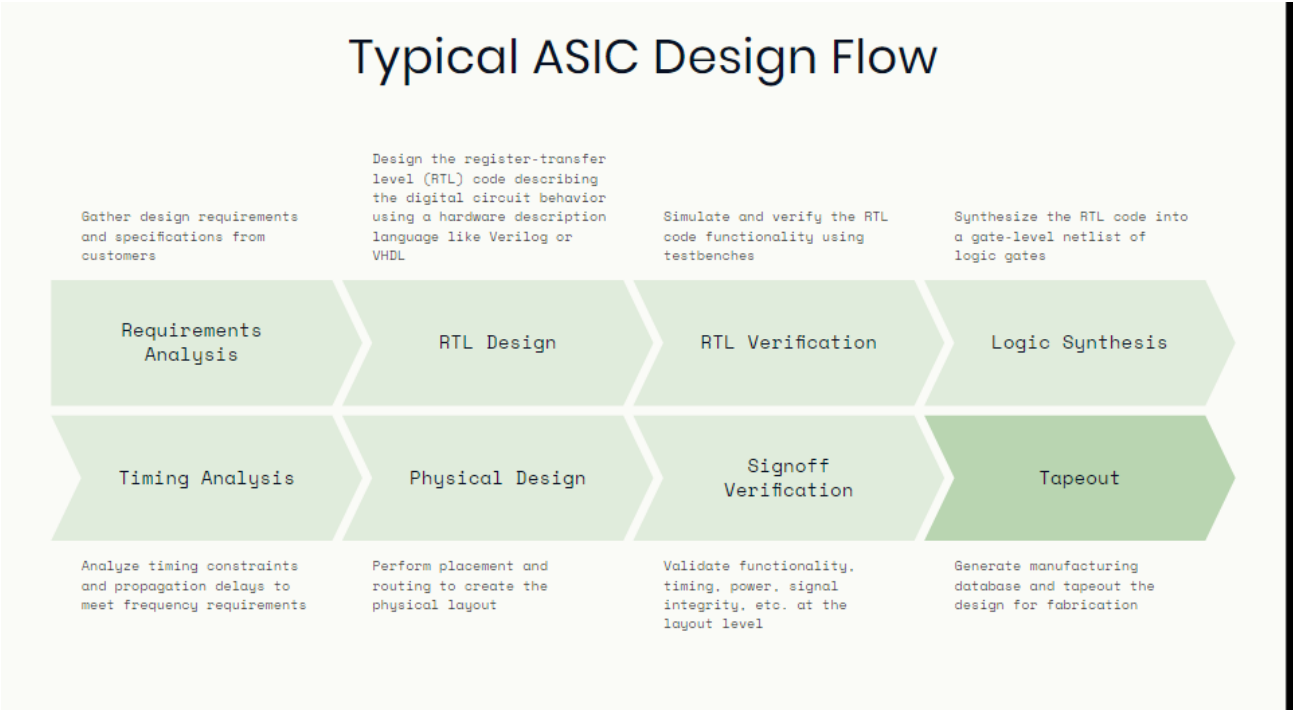
- **Unlike proprietary EDA who are focused on the bleeding edge and on designs where maximum PPA is required, regardless of the cost of tools or engineering effort, OpenROAD, provide a low cost, out of the box, push button RTL to tapeout flow**

Precision Innovations makes OpenROAD industry-ready : Build tools, native flow, test and support services

- IP design houses are building test chips with OpenROAD
- Others are interested in architecture exploration, productivity enhancements … Google, Ascenium
  - Users tell us the ASAP 7 nm is within 15% of commercial PPA and 5X faster!
- Expert tool and design services support down to 12nm for complete flow, down to 3nm for estimation

HOW IS ASIC DESIGN DONE TODAY?

- **Very sophisticated tools with 1000's of commands**
- **Tool supplier focus: performance, power, area**
- **Large teams of expert users, many manual steps**
  - **Challenges during handoff, too many iterations**
  - **Lack of tools for early design exploration**
- **Long project schedules with very little opportunity to enhance productivity and reduce design turnaround time**
- **Significant project risks**
  - Most of the design work is post-layout optimization which significantly increases risk



Source: Gen AI

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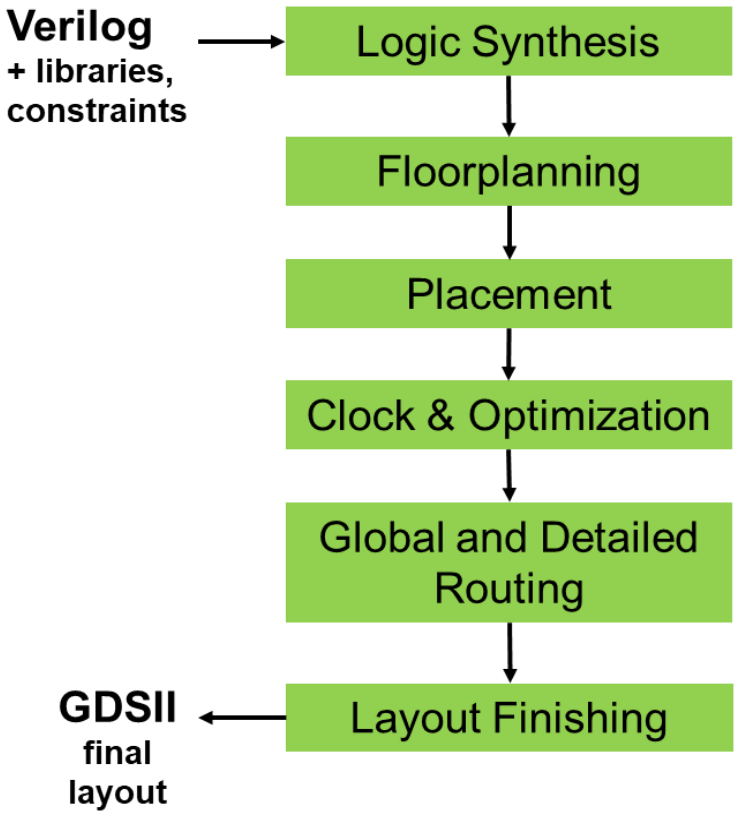
OpenROAD

OpenROAD for low-cost, easy-to-use ASIC design

- Autonomous RTL-to-GDS implementation flow
  - < 24 hrs, no-human-in-the loop
- Manufacturable layout
  - Proven on commercial PDKs from 180nm to 12nm
  - Support for private and public PDKS
- Complements commercial EDA and semiconductor ecosystem partner flows
  - Openlane-Efabless, Silicon Compiler Systems, DATC, Bazel
  - Easy handoff for Physical verification and signoff



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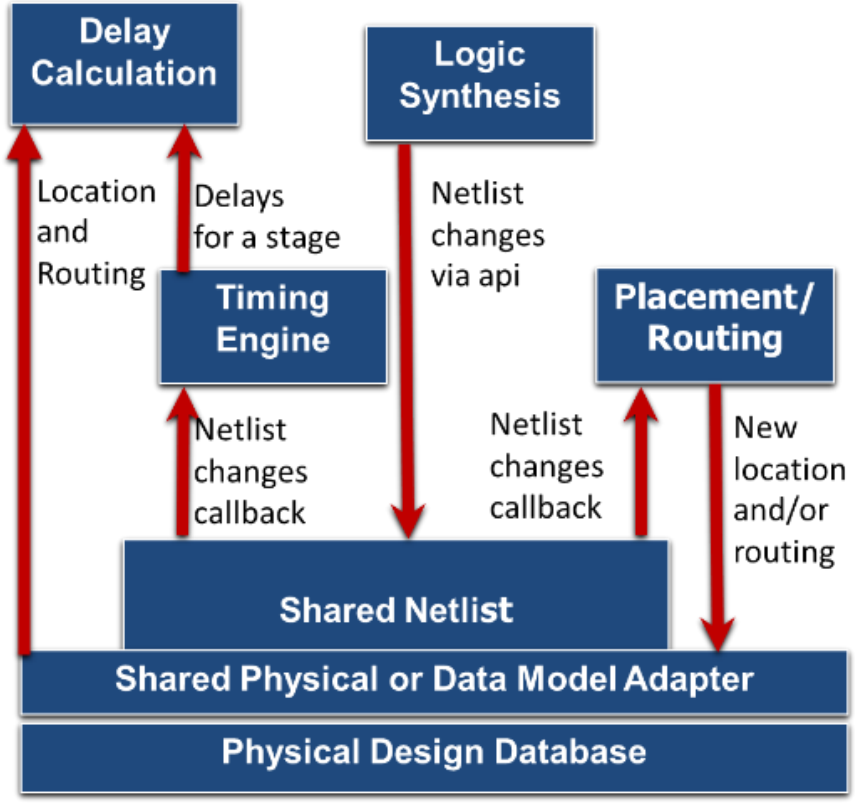
OpenROAD

Scalable Architecture for Industrial Applications

- Shared Netlist, Data model in memory
  - Communicates in real-time across key design stages - Synthesis, Placement, Routing, Optimization and Analysis (Timing, Congestion etc.)
  - Integrated, Common database ODB
  - Integrated Timing engine – OpenSTA
    - Timing, switching power
    - Common GUI – for analysis, visualization and API support
- Benefit: Important for modern PnR tools for speed and efficiency
  - Enables thousands of device sizing or incremental moves/sec
  - No need to stream design data files into multiple tools during design and optimization
- Support for distributed, parallel processing across for computational efficiency and productivity
  - COPILOT – manages key task distribution during design partitioning and routing



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OpenROAD

Interoperable Open-source and Commercial flows

- Free, No-licensing, Unlimited tool runs, Does not lock you in
  - Industry Standard tools, flows and data formats
  - Supports modern software architecture for development, problem reporting, fixes
- You can use other commercial EDA tools inter-operably with OpenROAD
  - Mix-and-match with other EDA and open-source tools
    - Use for early design exploration and a good pnR netlist before final production in commercial tool flows
  - Examples
    - Support for a DC netlist for PnR
    - PrimeTime for Static timing verification
    - Simulation in Verilog, SPICE etc.
  - Signoff flows with extraction and verification tools
    - E.g Calibre rule for extraction and DRC
- Examples of OpenROAD Commercial Flows today
  - Efabless – Efabless.com- OpenLane- ChipIgnite program
  - SiliconCompiler – SiliconCompiler.com - Use OpenROAD for ASIC design https://docs.siliconcompiler.com/en/stable/user_guide/installation.html#asic-demo
  - Google- Bazel interface on ORFS- used internally by hardware team

Practical for Applications on Mature nodes

- Mature nodes – 180nm- 22nm, Moore's law still applies
  - Planar CMOS, FinFets, EUV and materials enhancements
- Large number of applications are still developed in mid-range technologies– Industrial, Automotive, Consumer Electronics, and Legacy Systems for Computers
- **Time-to-Market, Reliability and Longevity are more important than PPA – Suitable for high-volume, low-cost design**
  - **RISC-V** based applications – IoT, e-toys, battery etc.
  - 180 nm- Sensor Systems-smoke alarms, Fitness Wearables, Battery Efficiency, motor drives
  - 130nm- Intel Pentium, microcontrollers, cable modem
  - 90nm – Pentium 4, Nvidia Graphics, IBM Power PC
  - 65nm –Processors, Advanced Graphics, WiFi
  - 12nm - Higher performance processing, AI chips
- Aligns with the core objectives and goals of the Government of India, Meity
  - **Indian Semiconductor Industry TAM: 55 billion by 2026,** more than 60% of which is driven by three industries: smartphones & wearables, automotive components, and computing & data storage **– source Deloitte report, 2023**
  - Natural fit with RISC-V based processors like Shakti, Vega
  - **Core Mandate of IITG under the leadership of Prof. Gaurav Trivedi**

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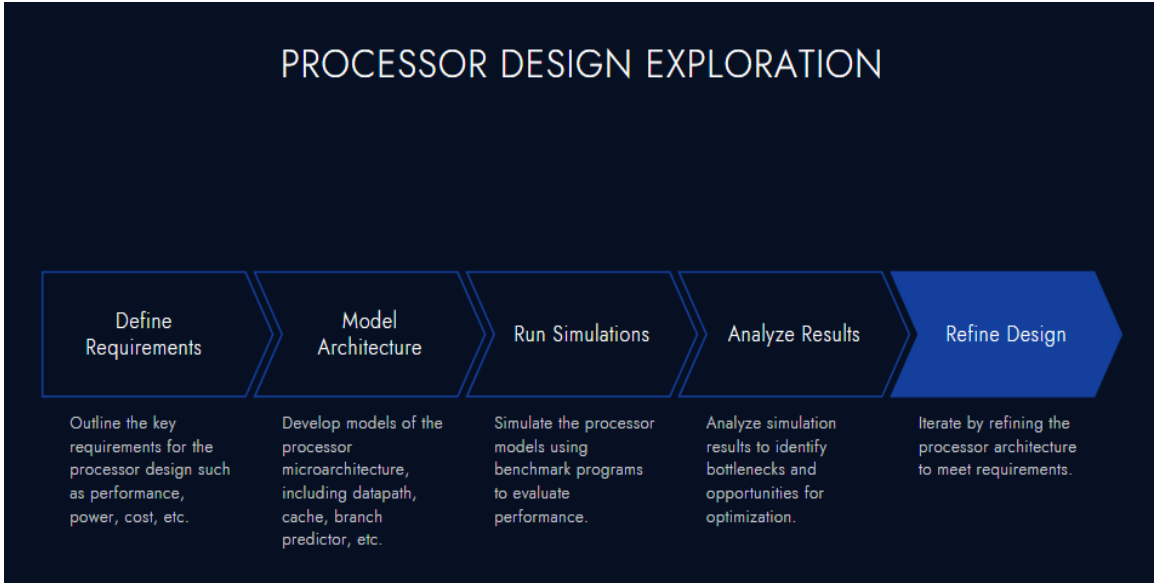
OpenROAD

OpenROAD Accelerates Design turnaround for advanced applications

- Processors, Hardware accelerators for HPC in Supercomputing, AI chips for datacenters, Healthcare etc. – mainly 7nm- 3nm
  - AI Chip market market projection
  - The global artificial intelligence chip market was valued at **$14.9 billion in 2022, and is projected to reach $383.7 billion by 2032, growing at a CAGR of 38.2% from 2023 to 2032** – source allied market research
- OpenROAD enables rapid design prototyping and proof-of-concept trials before production
  - Ascenium (Ascenium.com) uses OpenROAD for next gen Processor
  - Abacus designs next gen architectures for performance and power. They would like to use OpenROAD for architecture explorations and Proof-of-concepts.https://www.abacus-semi.com/blog.html#articleSix

Ascenium Uses OpenROAD for next gen General Processor

- Stringent design requirements for competitive edge
  - High performance, energy efficient
  - Faster compute engine for compiler blocks and efficient resource utilization in datacenter applications
  - Short time-to-market
  - Large designs with short turnaround
- OpenROAD provides key benefits
  - Explore multiple microarchitectures for the best PPA
  - Tightly placed large arrays of standard cells
  - Optimized clock-tree to minimize skew
  - Automatic macro-placement of large macros
  - Handling timing constraints across the design hierarchy
  - Better upfront design, fewer back-end iterations
  - Faster design convergence and signoff using commercial EDA



Source: Gen AI

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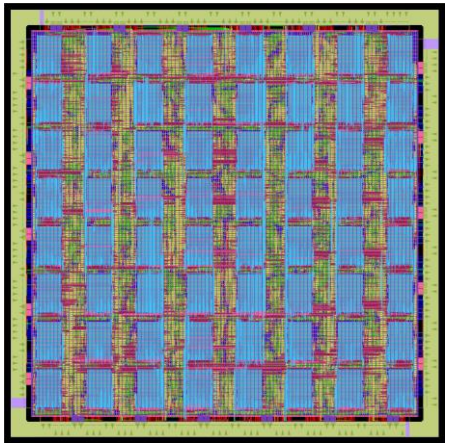
Some Key Customer Quotes

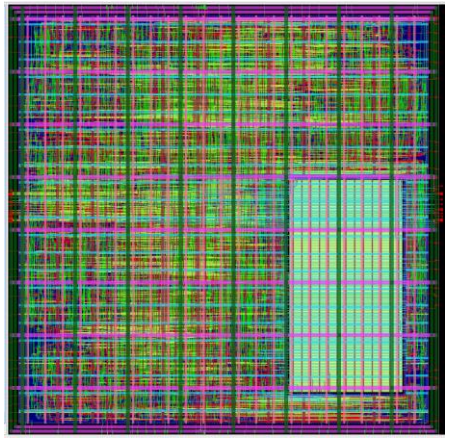
"OpenROAD has made a quantum leap in terms of scalability and stability in 2023. We use Bazel with OpenROAD-flow-scripts to enhance the productivity and efficiency of our workflows as we run multiple experiments, continuously integrate and test design changes. We are seeing many improvements overall in terms of the ability to handle large designs with complex macros, constraints that must be managed across the design hierarchy and efficient placement of specialized instances such as large arrays of standard cells. We look forward to enhancements to CTS, hierarchical timing analysis and other features like the automatic macro placement in OpenROAD to get to the superior performance and power targets that our processors deliver over conventional CPU architectures." , Oyvind Harboe- V.P Engineering, Ascenium

"While the commercial tools maybe able to cover more processes down to the FinFET and Gate-All-Around nodes, the OpenROAD team has identified many issues that the average ASIC Design engineer needs and has set out to solve those. Multi-die and MCM are already included in the flows, and integration of analog and mixed-signal into digital logic design are straightforward. What impressed me even more is the willingness and ability of the team and engineering to react quickly to suggestions. We will use that toolset for all of our proof-of-concept designs, which will also allow us to compartmentalize our designs and assist in better design verification." CEO, Axel Kloth, Abacus Semiconductors

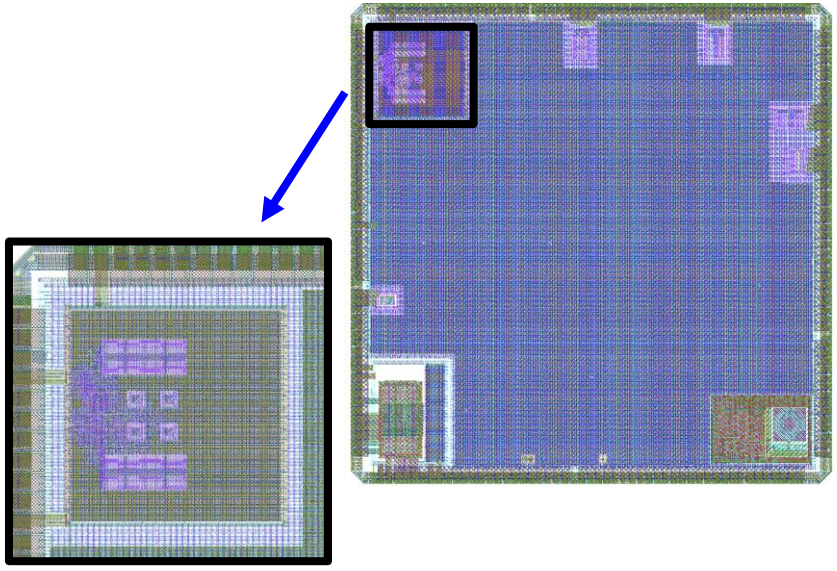
OpenROAD has been tested on Advanced nodes



programmable
GF55 AI platform



GF12LP
reprogrammable AI tile



OpenTitan SoC- integrated temp sensors

Army Research Labs
GF55, GF12LP

U. Michigan / FASoC
GF12LP

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OpenROAD

Trusted Microelectronics for Supply Chain and Security

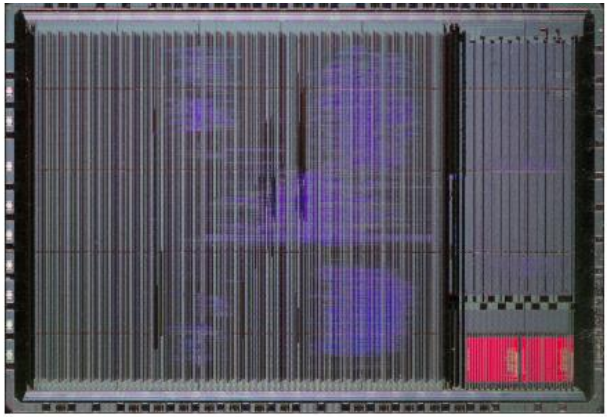
- OpenROAD is important for creating trusted microelectronics
  - Hardware security
  - Root-of-trust SoC design
  - Defense and Military applications
  - Strengthening Supply Chain resilience
- Why?
  - No-Human-in-Loop – eliminates human tampering with malicious intent, transparency
  - Harden the blocks during early stages of design
- Two notable tapeouts in 2023
  - Germany's HEP alliance use OpenROAD-based tool chain for secure hardware regionally
    - Ability to harden hardware security blocks, avoid other vulnerabilities in the design phase like side channel attacks
    - Dec 12 tapeout based on RISC-V
  - U Michigan tapeout out a mixed-signal SoC using OpenTitan and OpenROAD
    - RISC-V , IBEX, AES, temperature sensor

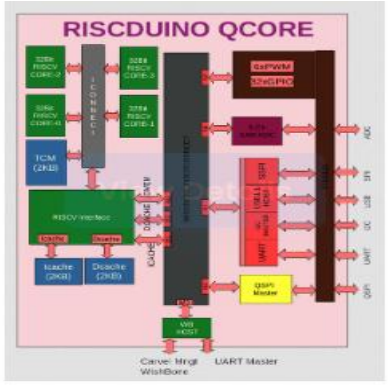
Source: Gen AI

OpenROAD Flow is Silicon Ready

- **SKY130: 600+ tapeouts**
  GF180 : 88
- Supports public (GF, SkyWater, IHP) and private PDKS (intel 22nm, 16nm, GF12nm)
  - **Recently enabled SCL PDK in ORFS**
- Lab-fab learning on TinyTapeout shuttles

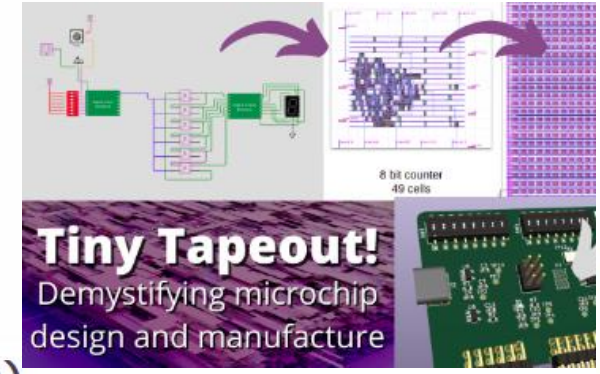
Open MPW Shuttle Program — efabless sponsored by Google





Riscduino-QCore(Q2)

public



Microwatt MPW7 public

Anton Blanchard

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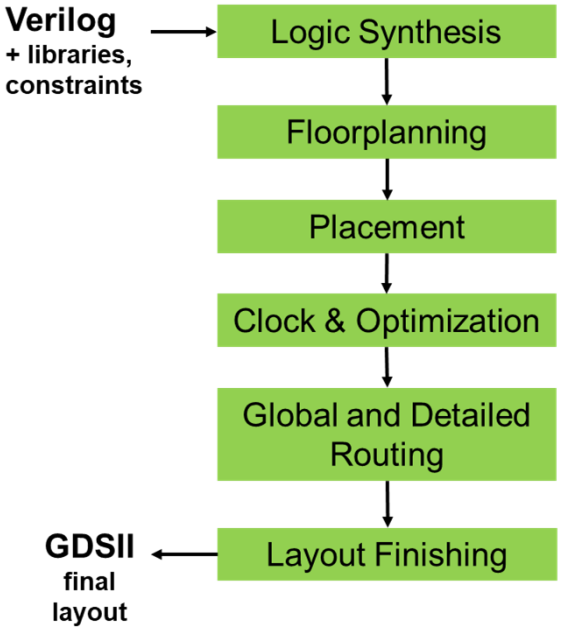
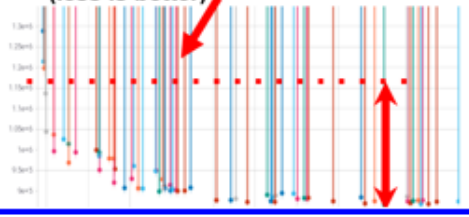
OpenROAD Innovation for the Cloud-scaling of EDA



- **What if tool licenses are unlimited?**
- **"COPILOT"** = **C**loud **O**ptimized **P**hysical
- **I**mplementation using OpenROAD **T**echnology
- **ML challenge: predict failure and intervene**
- **AutoTuner rapid hyperparameter tuning and optimization**

Default flow score = 1,174,346
Our Best Score = 855,373
(370 trials in total 500 #trials)
(less is better)



Improvement
WL 1003801um → 843258um **(-16%)**
Effective CP 20.935ns → 16.185 ns **(-23%)**
Total power 0.024 W→ 0.0133 W **(-45%)**

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OpenROAD

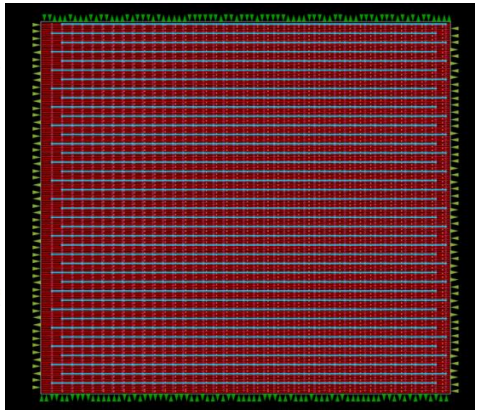
OpenROAD/OpenPOWER for Low-power and HPC applications

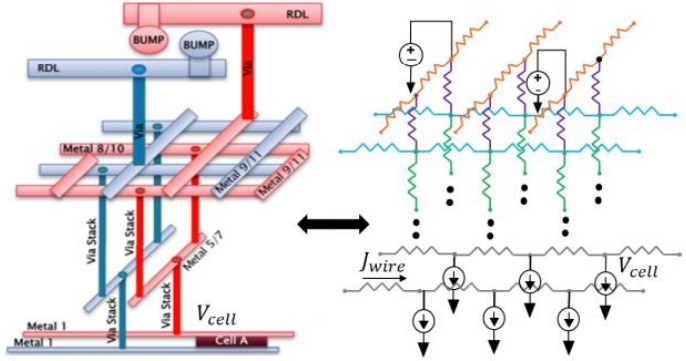
- OpenROAD is part of the IBM OpenPOWER Platform to deliver highly efficient, fast design and low power capabilities
- OpenROAD enables intelligent tradeoffs between performance and Power
  - Multi-Vt libraries, Multiple clock domains and voltage regions
  - Support for both static and dynamic power analysis (Vector based)
  - Support for multiple power domains and switches through UPF – Coming shortly!
- Creation of Microwatt using ORFS is the first step in building open-source, low-power cores for OpenPOWER
- Advanced ML based model for Static IR prediction in OpenROAD
  - http://iccad-contest.org/Document/Problems/Problem_C_%20Static_IR%20Drop_Estimation_Using_Machine_Learning_v5.pdf

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	4.73e-03	1.15e-02	4.55e-09	1.62e-02	35.3%
Combinational	1.05e-02	1.92e-02	3.79e-08	2.97e-02	64.7%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	1.53e-02	3.07e-02	4.25e-08	4.59e-02	100.0%
	33.2%	66.8%	0.0%		

Aes post routing stage final power report:
finish report_power

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	4.40e-03	5.91e-03	4.55e-09	1.03e-02	23.2%
Combinational	1.21e-02	2.19e-02	3.85e-08	3.40e-02	76.8%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	1.65e-02	2.78e-02	4.30e-08	4.44e-02	100.0%
	37.2%	62.8%	0.0%		





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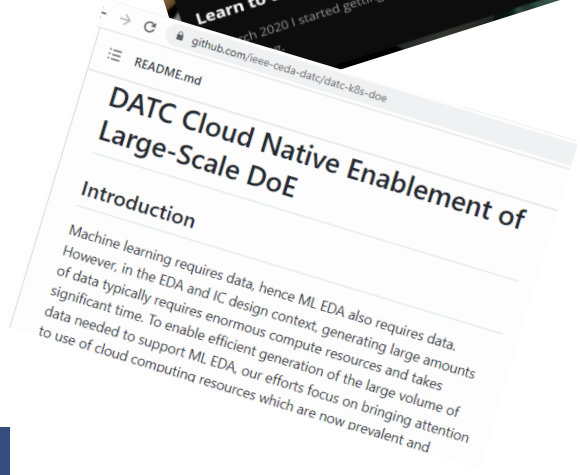
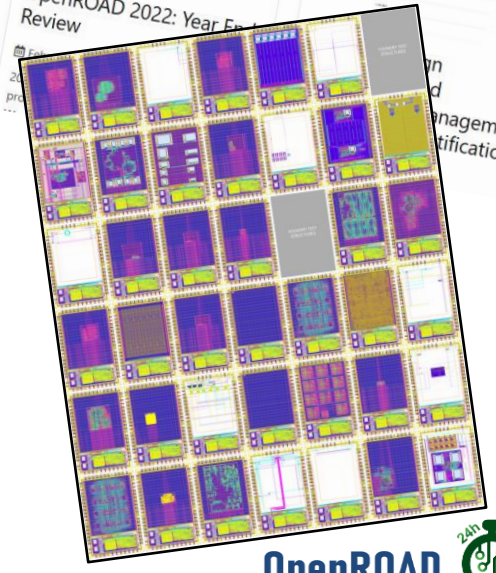
OpenROAD

OpenROAD is About the Future

- Community
- Education
- Research





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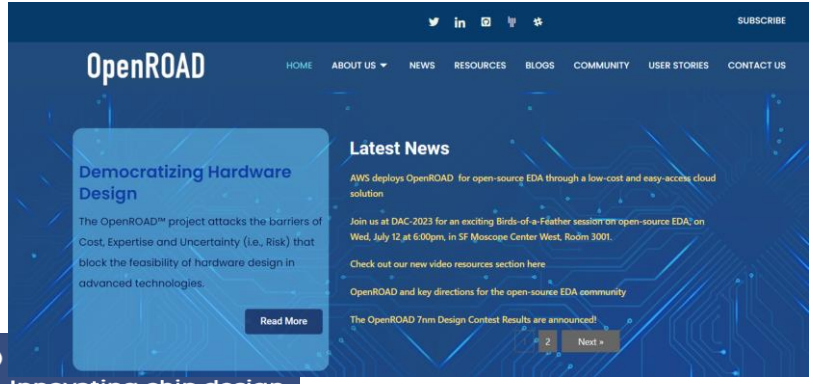
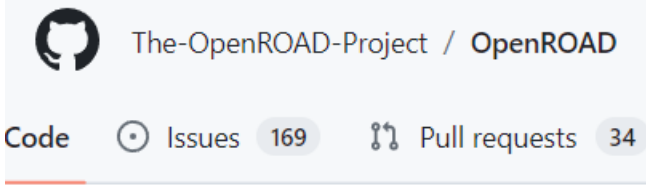
OpenROAD

Our Community is Growing - Join us!

- OpenROAD has gone viral!
  - 2000+ and growing followers on LinkedIn
  - Growing number of users on twitter, slack and github
  - Useful resources on website
- Users range from novice to expert
  - Applications include Trust, 3DIC, AI/ML





Thanks

Many Thanks to the Indian Institute of Technology Guwahati and Professor Gaurav Trivedi for inviting me today!