Ministry of Electronics and Information Technology

Sponsored Workshop on

OpenROAD for Low-Cost ASIC Design and Rapid Innovation

Organized by

Novel Integrated Electronics (NINE) Labs

(Under MeitY, Govt. of India)

Indian Institute of Technology Guwahati

Guwahati Assam, Pin 781039

Static Timing Analysis

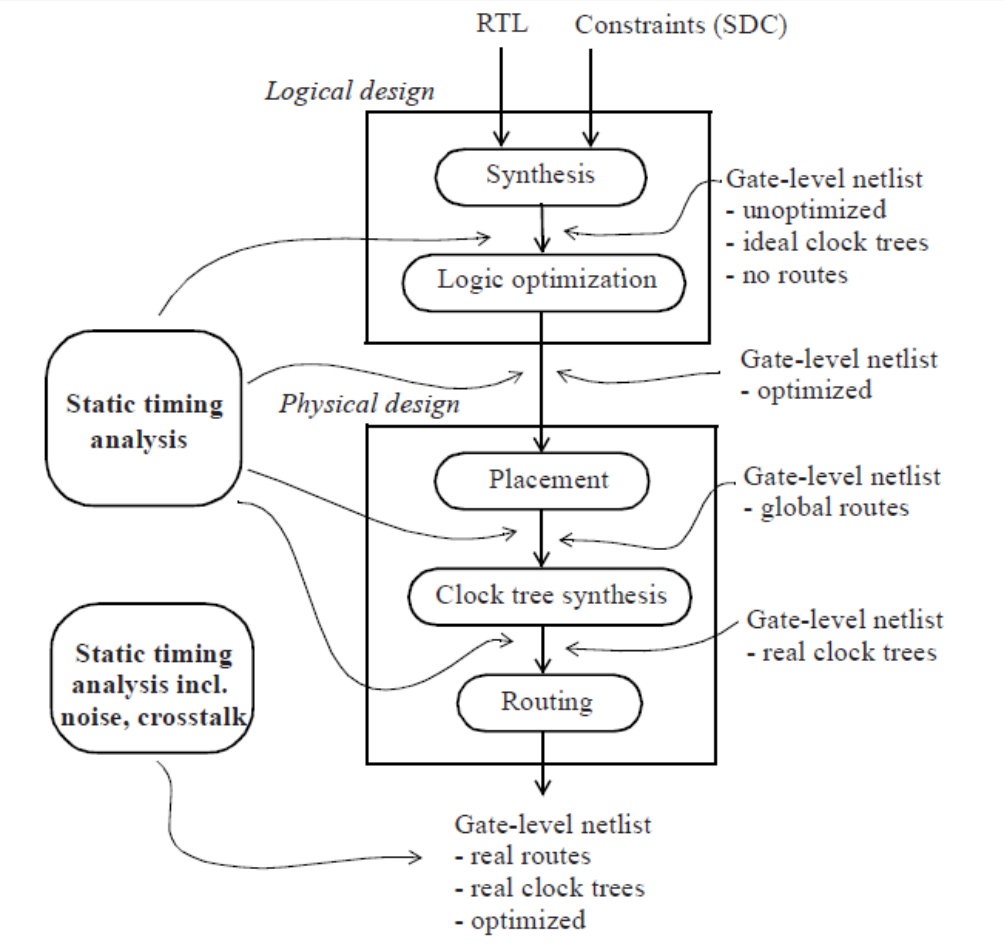
- Analyzing or verifying the timing of a design i.e., whether a design meet all of its timing requirements or not
- it is done by a design tool (Prime by Synopsys) that starts from the optimized gate level netlist and runs automatically
- STA looks for the worst of the following delays in a chip

- **Timing Checks:**
  - set-up, hold, removal, and recovery constraints
  - Minimum Period and minimum Pulse width for clocks

Static Timing Analysis

- STA involves three main steps -
  - Design is broken into sets of timing paths
  - The delay of each path is calculated
  - All path delays are compared to see if timing constraints have been meet.
- **Note:**
- It is more faster than simulator
- timing analysis is used to check for the timing correctness of the design but not used to check for the logical functional correctness for the design

STA Design Flow



Start Point

- clock port of the register
- input port of the design

End Point

- data input of register
- output port

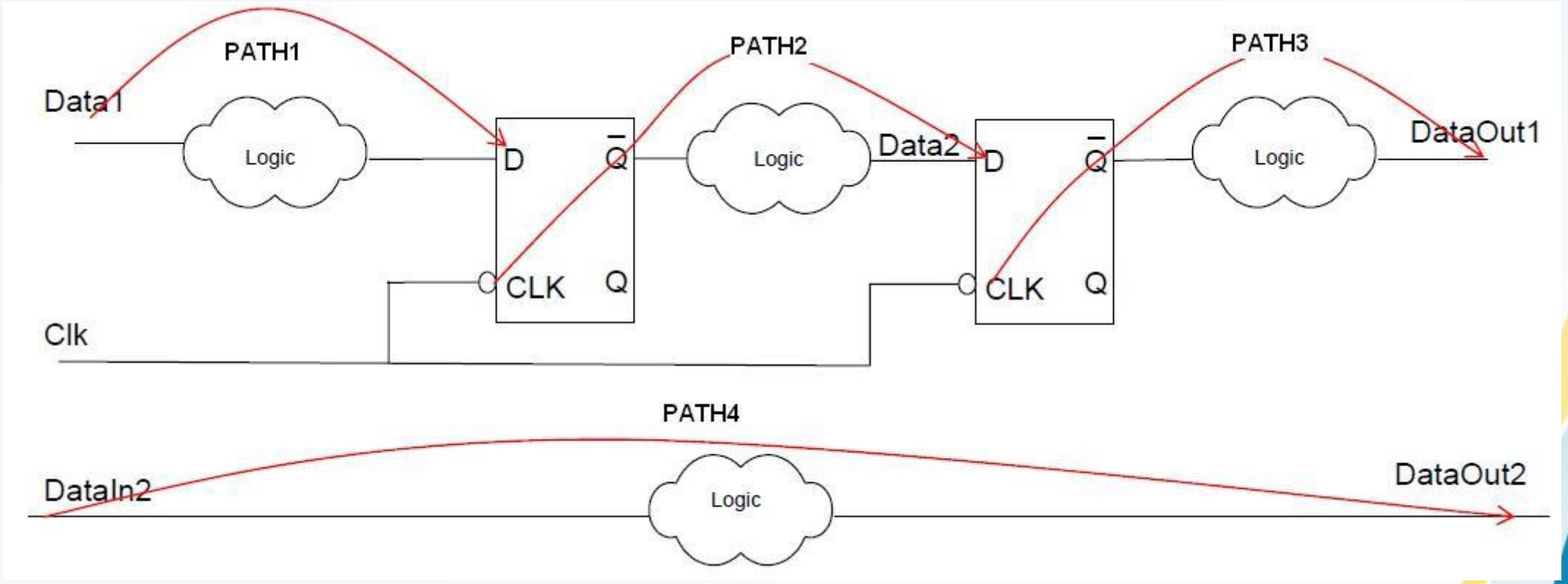
There are four timing paths:

- Data Path
- Clock Path
- Clock gating Path
- Asynchronous path

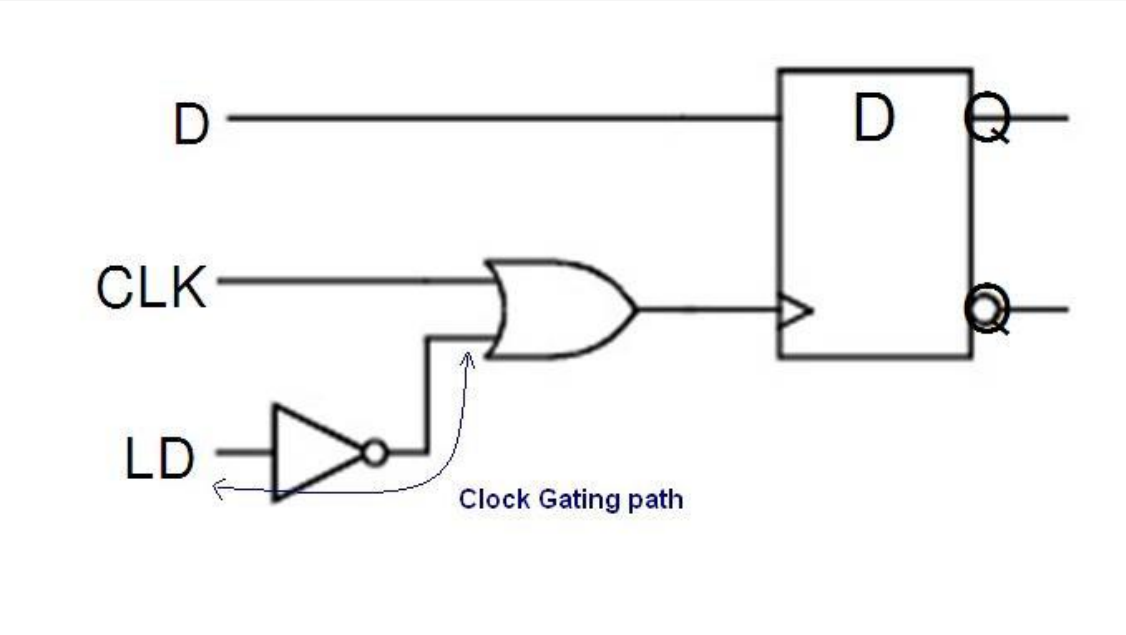
Note:

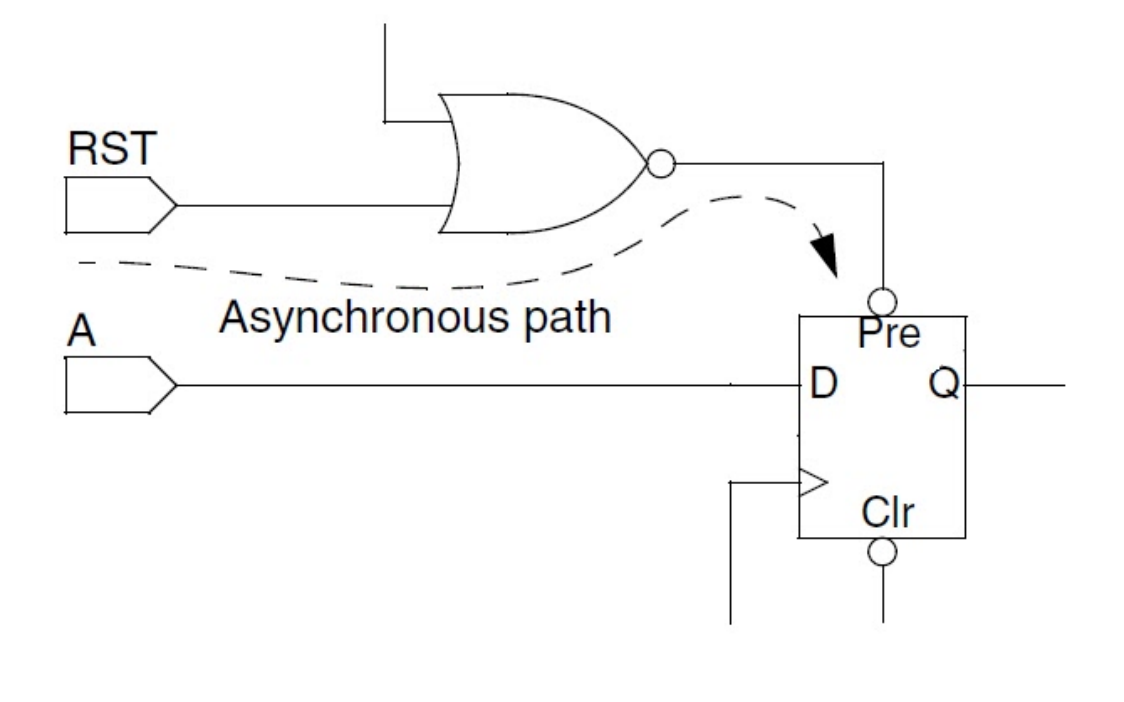
- timing analyzer checks for the worst possible delays through each of the logic elements in the timing paths but ignores the logical operations. (non-vectored approach)

Timing Paths

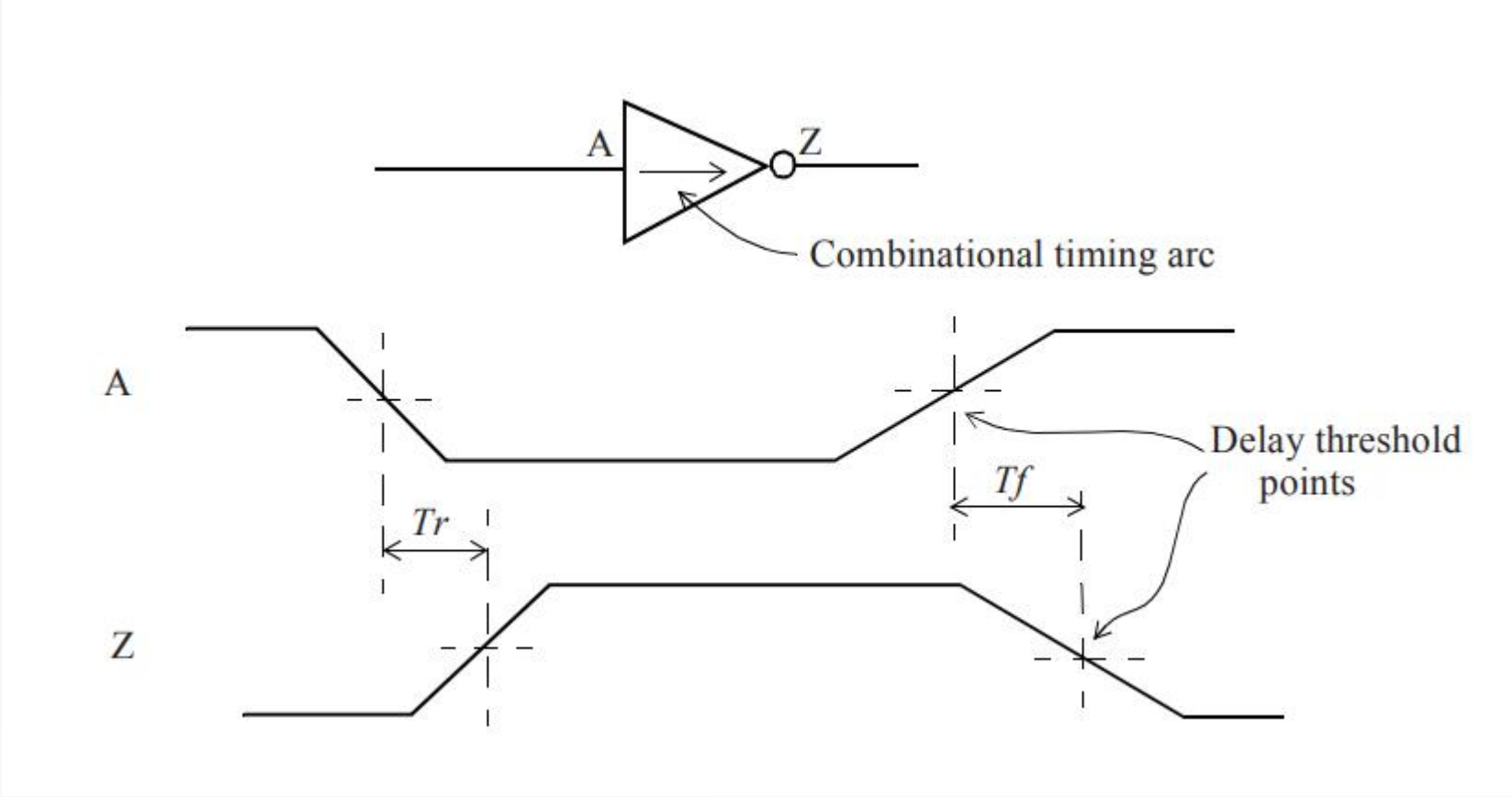


Clock Gating and Asynchronous paths





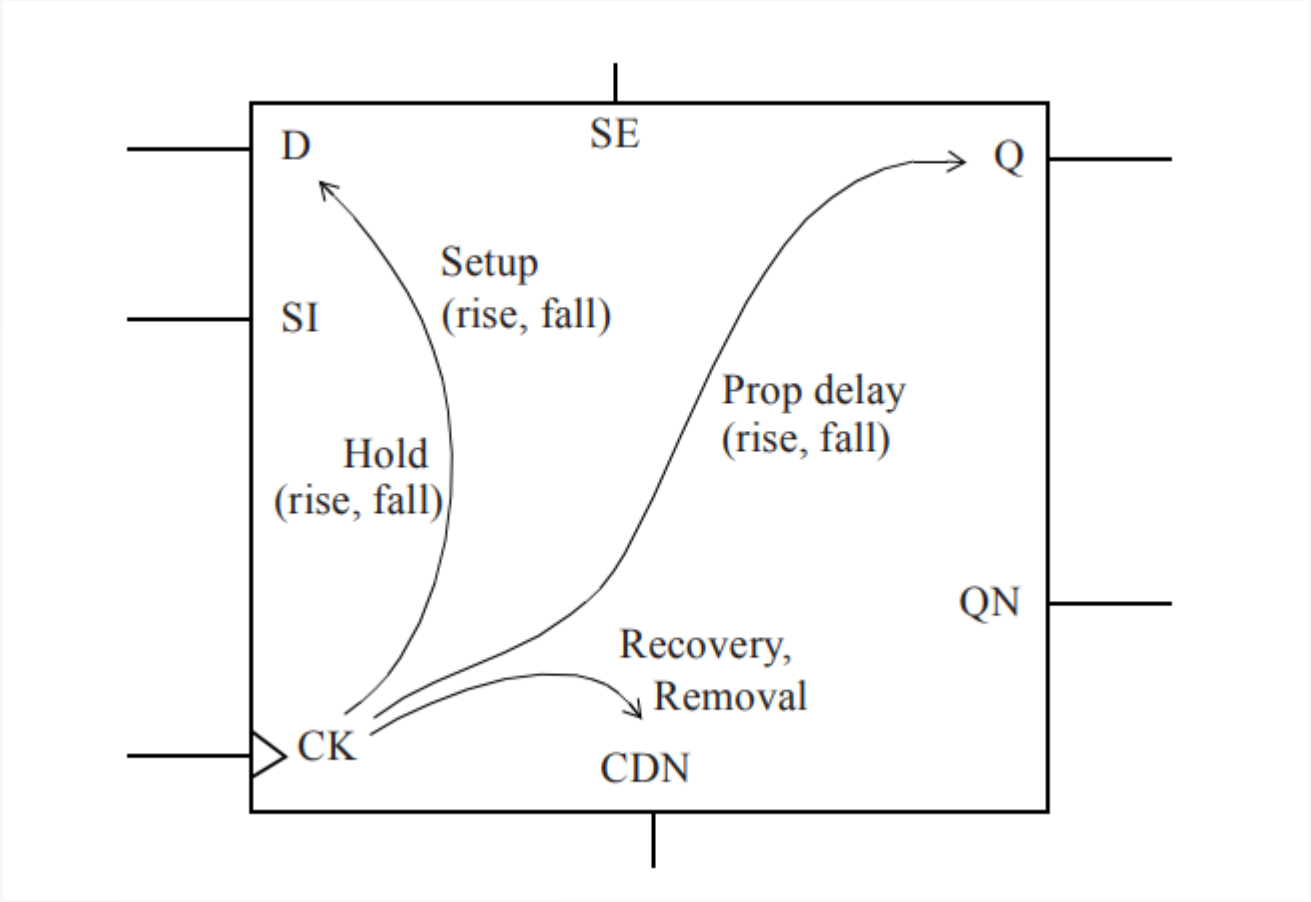
Inverter Cell



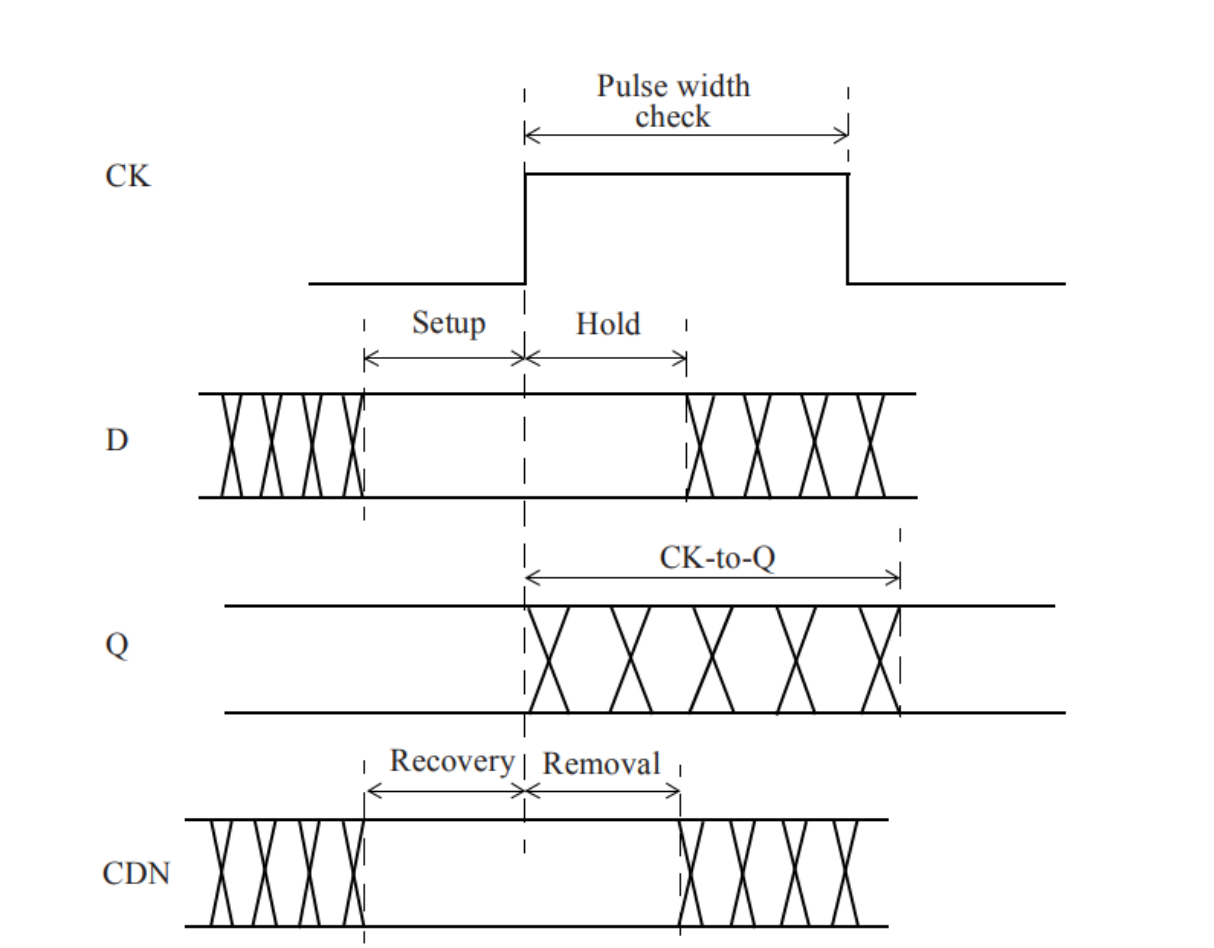
Look-UP table in .LIB

```
fall_transition(delay_template_3x3) {
  index_1 ("0.1, 0.3, 0.7"); /* Input transition */
  index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
  values ( /*    0.16      0.35     1.43 */ \
    /* 0.1 */   "0.0817,  0.1937,  0.7280", \
    /* 0.3 */   "0.1018,  0.2327,  0.7676", \
    /* 0.7 */   "0.1334,  0.2973,  0.8452");
}
```

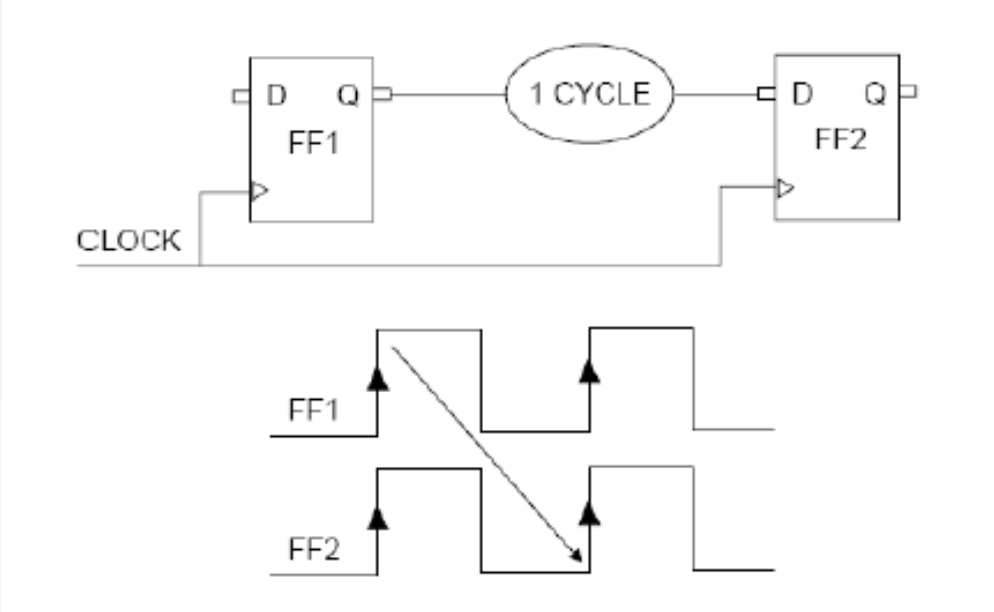
Timing Model of Flipflop



Setup, Hold, Recovery, Removal

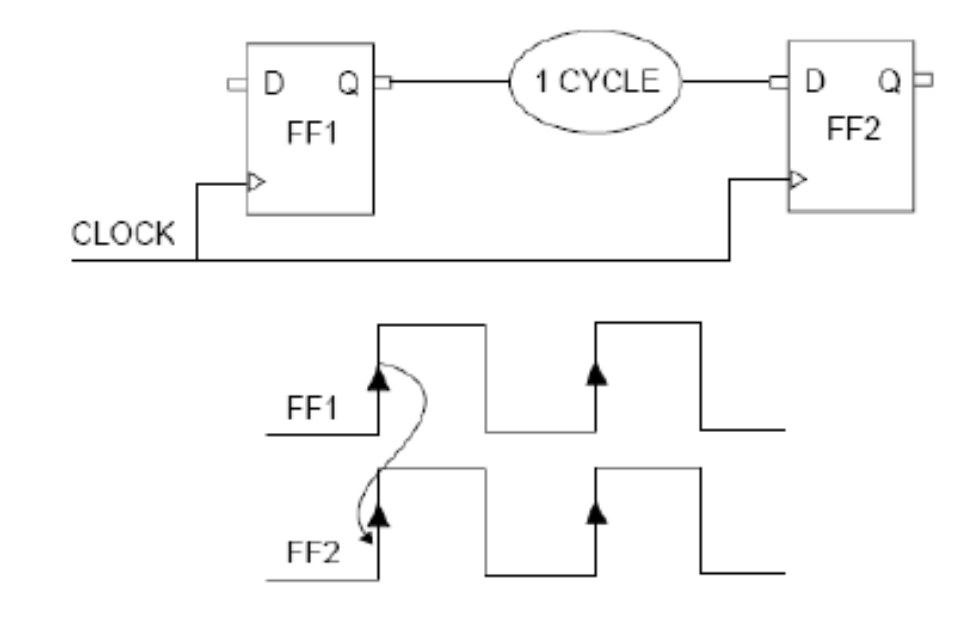


Setup



- Setup Slack = Required time - Arrival time (since we want data to arrive before it is required)
- C2Q+L1+Comb < T+L2-Tsu

Hold

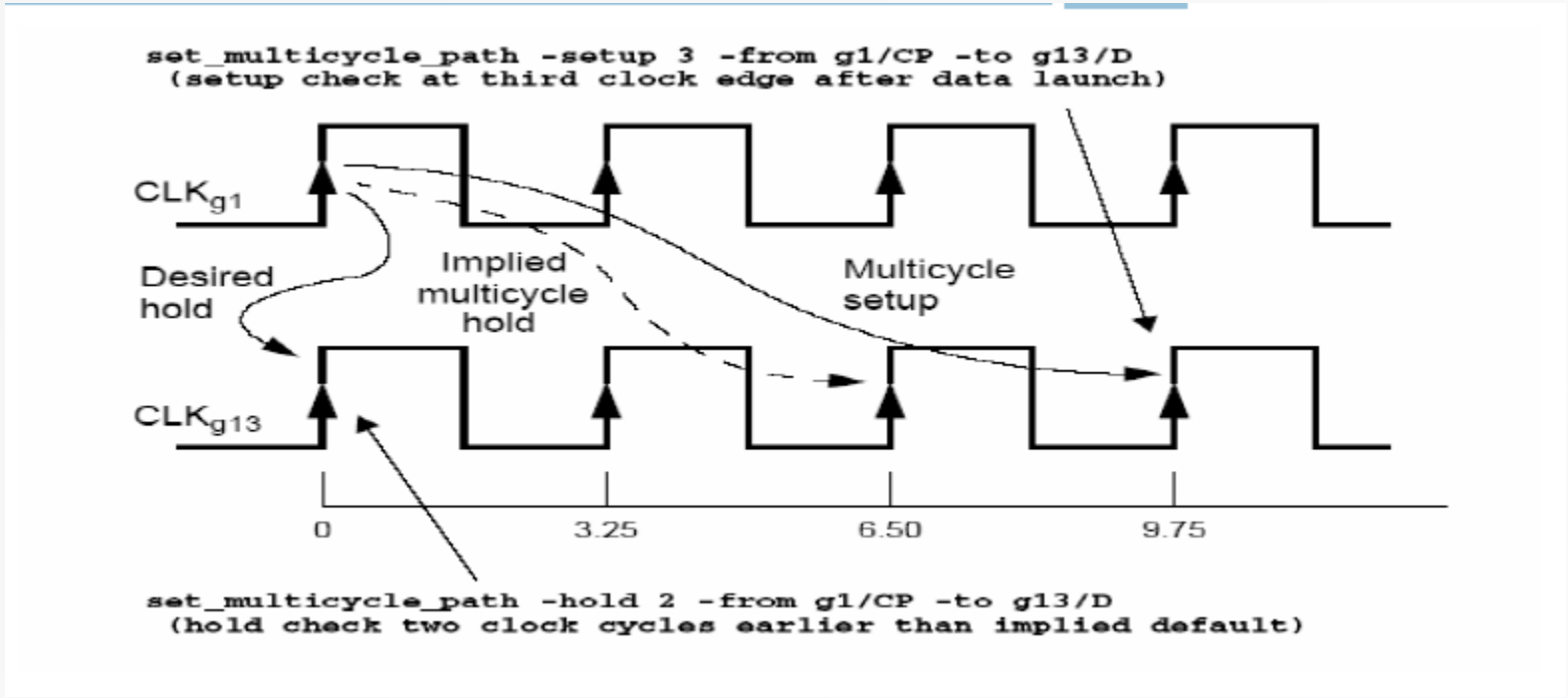


- Hold Slack = Arrival Time - Required time (since we want data to arrive after it is required)
- Comb+L1 > TH+L2+THU

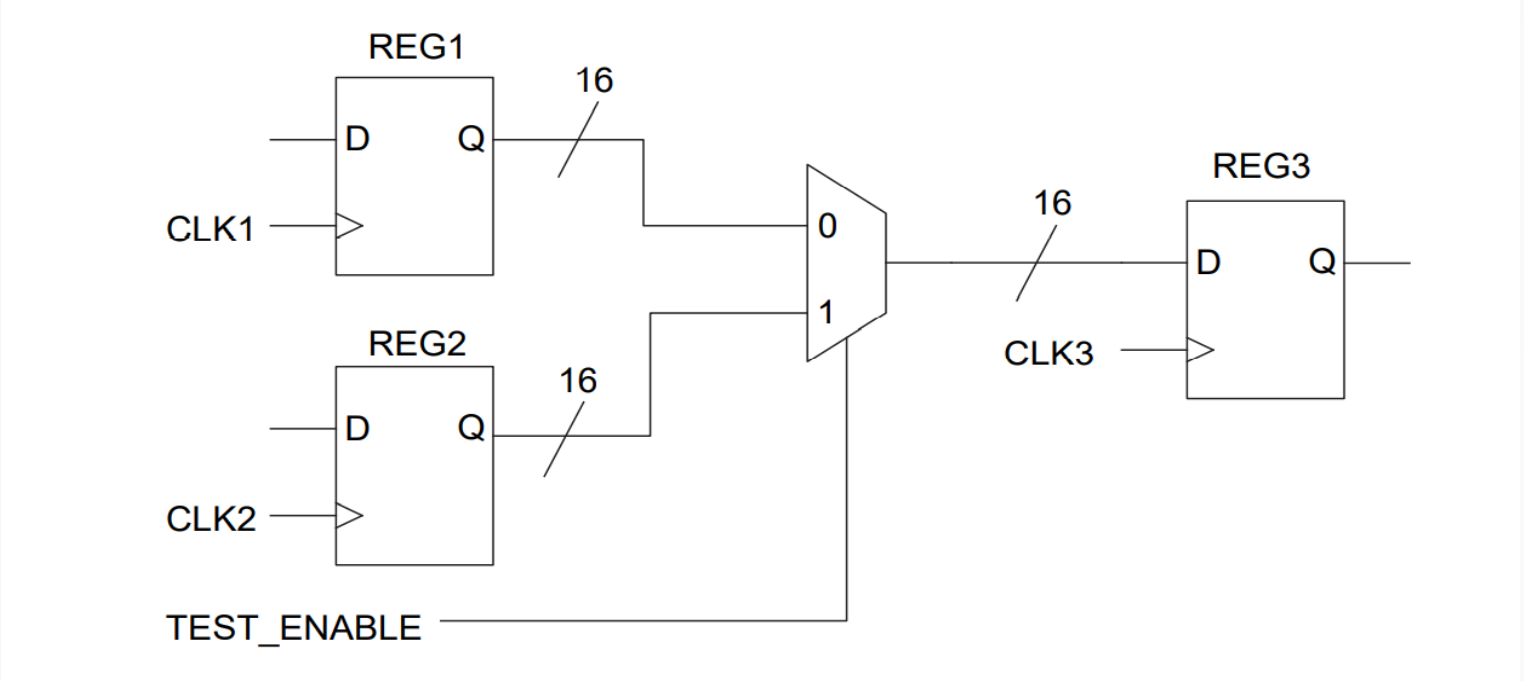
Timing Report

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min
  Min Data Paths Derating Factor  : 1.000
  Min Clock Paths Derating Factor : 1.000
  Max Clock Paths Derating Factor : 1.200

  Point                                    Incr       Path
  -------------------------------------------------------------
  clock CLKM (rise edge)                  0.000      0.000
  clock source latency                    0.000      0.000
  CLKM (in)                               0.000      0.000 r
  UCKBUF0/C (CKB  )                       0.056      0.056 r
  UCKBUF1/C (CKB  )                       0.058      0.114 r
  UFF0/CK (DF  )                          0.000      0.114 r
  UFF0/Q (DF  ) <-                        0.144      0.258 r
  UNOR0/ZN (NR2  )                        0.021      0.279 f
  UBUF4/Z (BUFF  )                        0.055      0.334 f
  UFF1/D (DF  )                           0.000      0.334 f
  data arrival time                                  0.334

  clock CLKM (rise edge)                  0.000      0.000
  clock source latency                    0.000      0.000
  CLKM (in)                               0.000      0.000 r
  UCKBUF0/C (CKB  )                       0.067      0.067 r
  UCKBUF2/C (CKB  )                       0.080      0.148 r
  UFF1/CK (DF  )                          0.000      0.148 r
  clock reconvergence pessimism          -0.011      0.136
  clock uncertainty                       0.050      0.186
  library hold time                       0.015      0.201
  data required time                                 0.201
  -------------------------------------------------------------
  data required time                                 0.201
  data arrival time                                 -0.334
  -------------------------------------------------------------
  slack (MET)                                        0.133
```

Exceptions-Multi Cycle paths

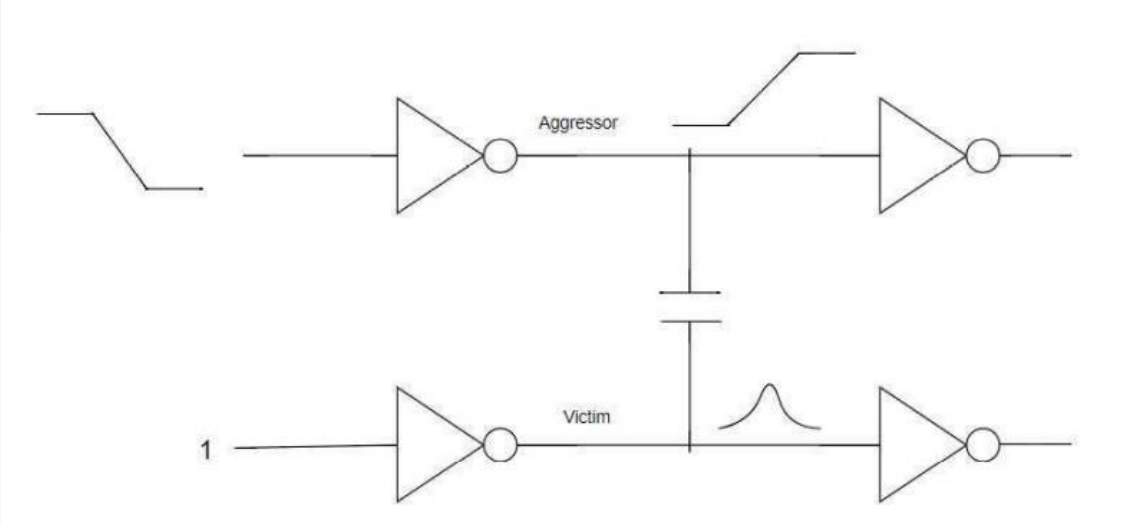


Exceptions- False paths

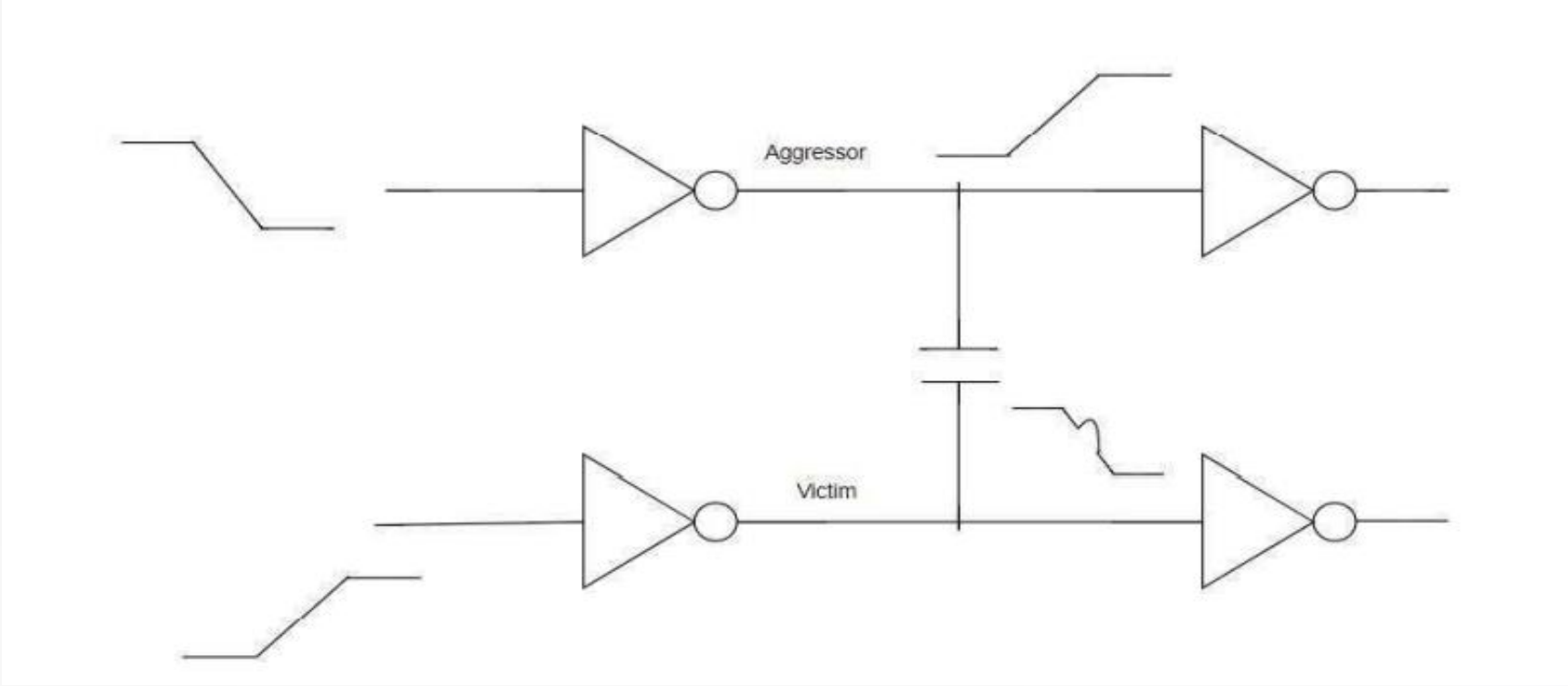


set_false_path \ -from [get_clocks CLK2] -to [get_clocks CLK3]

Cross Talk - Glitch

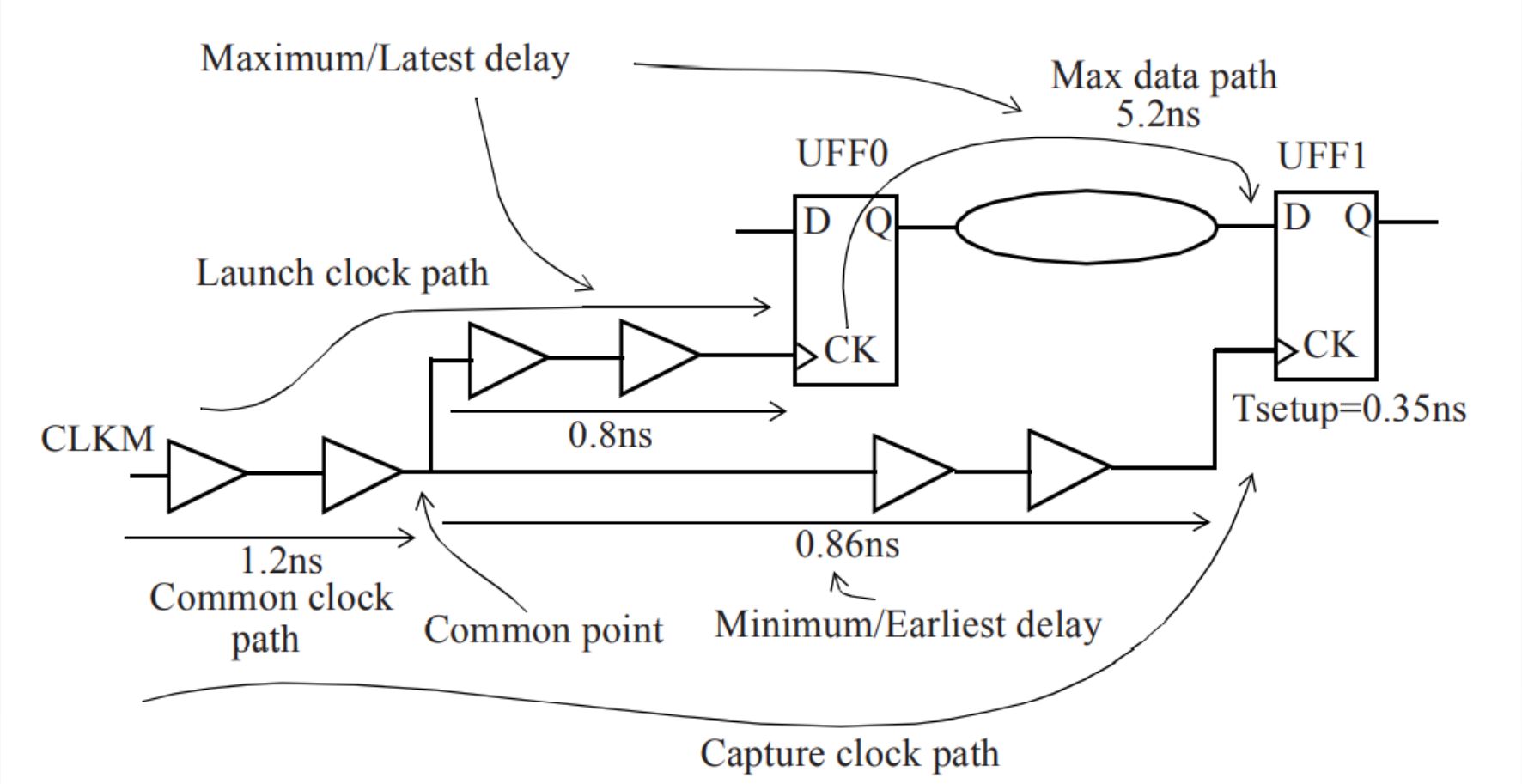


Crosstalk - Delta Delay



$$\text{Skew} = L_2 - L_1 = \blacktriangle$$

On-Chip Variations



LaunchClockPath + MaxDataPath <= ClockPeriod + CaptureClockPath - Tsetup_UFF1

This implies that the minimum clock period = LaunchClockPath + MaxDataPath - CaptureClockPath + Tsetup_UFF1

From the figure,
LaunchClockPath = 1.2 + 0.8 = 2.0
MaxDataPath = 5.2
CaptureClockPath = 1.2 + 0.86 = 2.06
Tsetup_UFF1 = 0.35
This results in a minimum clock period of:
2.0 + 5.2 – 2.06 + 0.35 = 5.49ns

Derates

- set_timing_derate -early 0.8
- set_timing_derate -late 1.1
- Derating the minimum/shortest/early paths by -20% and derate the maximum/longest/latest paths by +10%
- set_timing_derate -cell_delay -early 0.9
- set_timing_derate -cell_delay -late 1.0
- set_timing_derate -net_delay -early 1.0
- set_timing_derate -net_delay -late 1.2

Example

set_timing_derate -early 0.9
set_timing_derate -late 1.2
set_timing_derate -late 1.1 -cell_check
With these derating values, we get the following for setup check:
LaunchClockPath = 2.0 * 1.2 = 2.4
MaxDataPath = 5.2 * 1.2 = 6.24
CaptureClockPath = 2.06 * 0.9 = 1.854
Tsetup_UFF1 = 0.35 * 1.1 = 0.385
This results in a minimum clock period of:
2.4 + 6.24 – 1.854 + 0.385 = 7.171ns

CRPR

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min
  Min Data Paths Derating Factor   : 1.000
  Min Clock Paths Derating Factor : 1.000
  Max Clock Paths Derating Factor : 1.200

  Point                                              Incr         Path
  ---------------------------------------------------------------------
  clock CLKM (rise edge)                            0.000        0.000
  clock source latency                              0.000        0.000
  CLKM (in)                                         0.000        0.000 r
  UCKBUF0/C (CKB   )                                0.056        0.056 r
  UCKBUF1/C (CKB   )                                0.058        0.114 r
  UFF0/CK (DF   )                                   0.000        0.114 r
  UFF0/Q (DF   ) <-                                 0.144        0.258 r
  UNOR0/ZN (NR2   )                                 0.021        0.279 f
  UBUF4/Z (BUFF   )                                 0.055        0.334 f
  UFF1/D (DF   )                                    0.000        0.334 f
  data arrival time                                              0.334

  clock CLKM (rise edge)                            0.000        0.000
  clock source latency                              0.000        0.000
  CLKM (in)                                         0.000        0.000 r
  UCKBUF0/C (CKB   )                                0.067        0.067 r
  UCKBUF2/C (CKB   )                                0.080        0.148 r
  UFF1/CK (DF   )                                   0.000        0.148 r
  clock reconvergence pessimism                    -0.011        0.136
  clock uncertainty                                 0.050        0.186
  library hold time                                 0.015        0.201
  data required time                                             0.201
  ---------------------------------------------------------------------
  data required time                                             0.201
  data arrival time                                             -0.334
  ---------------------------------------------------------------------
  slack (MET)                                                    0.133
```


THANK YOU