OpenROAD – ASIC Design Exploration and a path for Rapid Innovation

Novel Integrated Electronics (NINE) Labs
Indian Institute of Technology Guwahati

Indira Iyer Almeida, OpenROAD team member

Head of Customer Success - Precision Innovations inc.

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https://theopenroadproject.org

www.precisioninno.com

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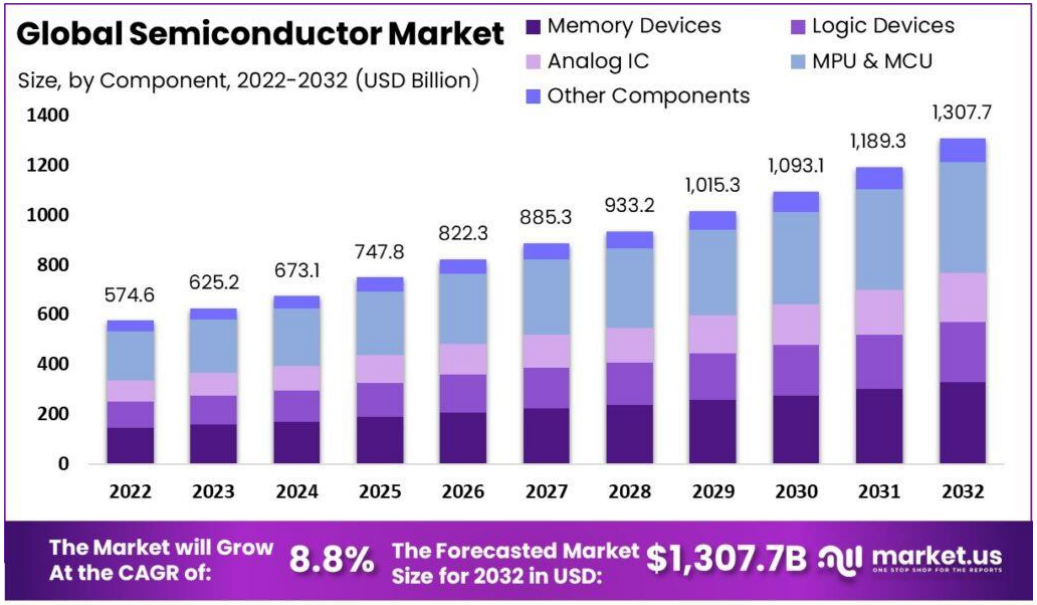
Innovation: A Key Driver for the Semiconductor Industry

- Innovation is the driver for growth and to meet the demands of the Semiconductor Industry
  - Current Size $600B, > $1T by 2030
  - Indian semiconductor Industry is poised to grow to $55B -2026 to $85B in 2030
    – source Deloitte, 2023
- Geo-political stability
  - Supply chain resilience
  - National security



Source Statista – 2023

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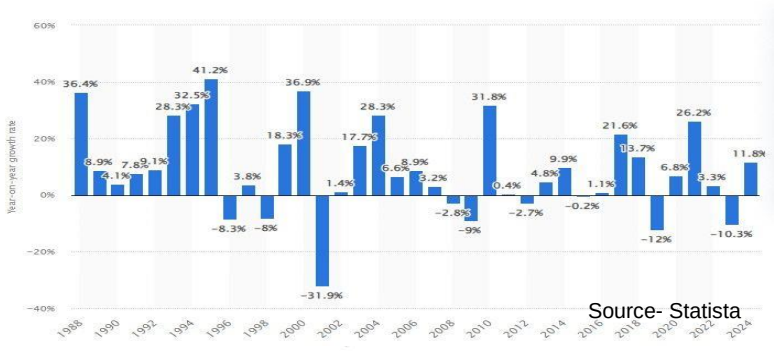
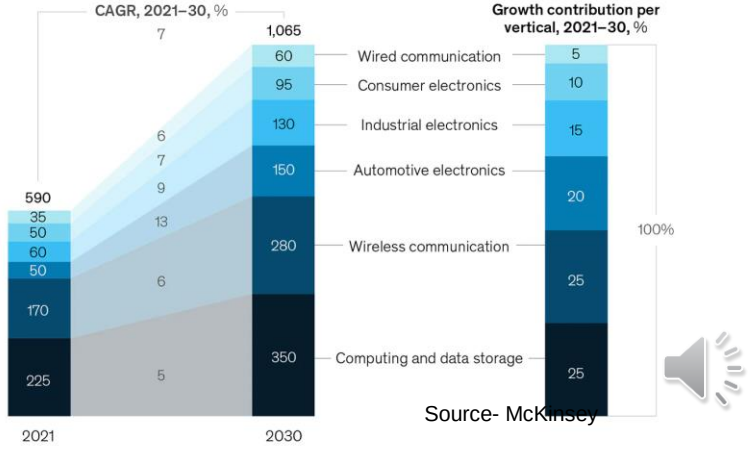
What Drives Innovation in Semiconductors?

- Market demands- Fast, New, Cheap
  - Efficient ways of building products- lower costs, higher efficiency, better quality
  - boom-bust cycles hard to predict
- Better technology, tools and design methodologies
  - Performance, Power, Costs
  - Smaller, higher density
- Complex functions on the SoC
  - Faster computation, better memory design, microarchitectures
  - Better integration, packaging
- Rapid Demand for AI Chips
  - Global AI chip market size valued at $14.9 billion in 2022, CAGR of 40.5% from 2023 to 2030 to around $227.6 billion by 2030. – source xresearch
  - Demand for AI chips
    - Faster, energy-efficient chips
    - Wireless, Automotive, HPC, Computation



Source- Statista



Source- McKinsey

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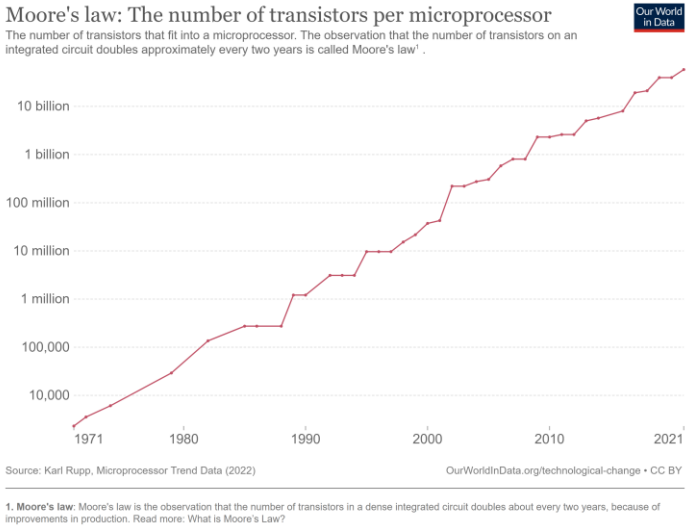
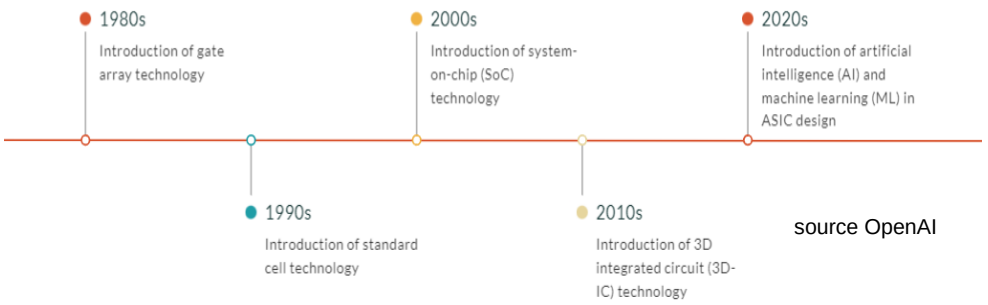
Exploring Chip design – Tools must track Process Innovation





source OpenAI

- Moore's law – Every two years chips double as cost/transistor sizes reduces
  - Driving principle for the Chip industry to produce smaller, faster and more power devices

- ASIC and SoC design methodology – key inflection point in 2000s
  - Increased functional integration, increases complexity in EDA software
    - Design flow, Database, analyses, verification, packaging
    - Disparate tools from vendors, expert software and hardware engineers

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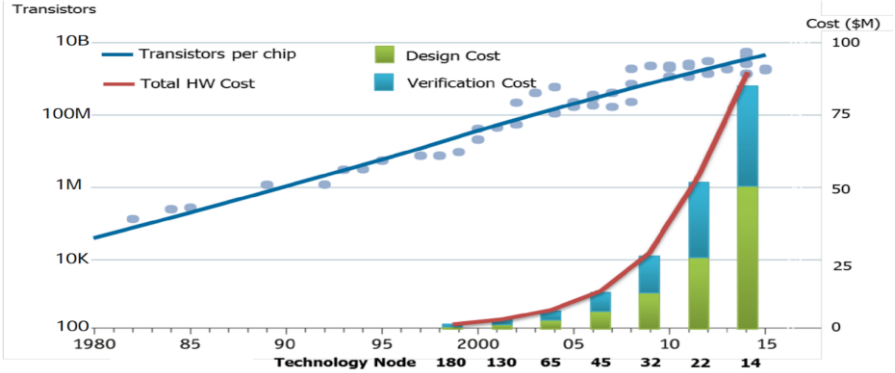
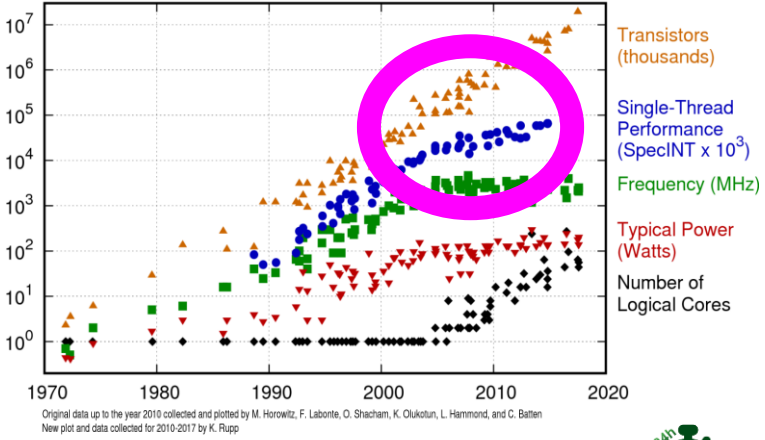
Challenges to Innovation in Chip Design

- Innovate or Stagnate – Chips are the bedrock of the semiconductor industry
- What is blocking Innovation?
  - Costs, Expertise, Uncertainties, Schedule constraints
  - EDA tools focus on delivering to the latest technology node
    - Failed to take advantage of computational resources- Cloud, advanced processors, GPUs
    - OpenROAD architected for scale- capacity, computational efficiency- exploit parallelism



A. Olofsson, ISPD-2018



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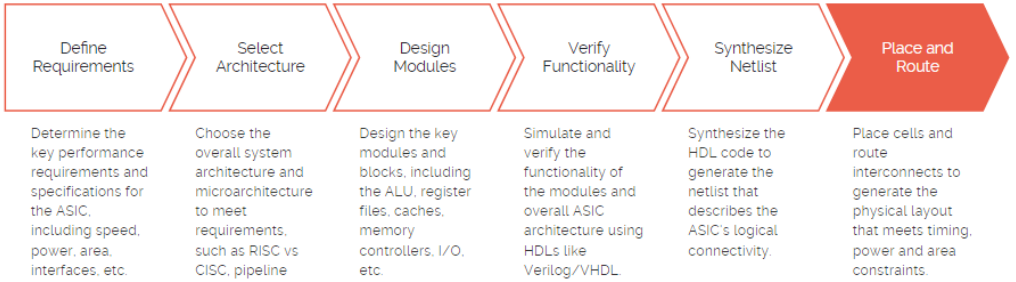
ASIC Design - Microarchitecture is crucial

- Microarchitecture – Organization of high-level components
  - Processors, datapath, memory, input/output interfaces, and control units.
  - Determines how the functional logic will perform in Physical design
- Goals – Achieve design targets- performance, power, area, with high confidence before final implementation
- Iterative process ->Model, Simulate, Analyze
  - Explore model and design configurations to achieve good physical design
  - Predict early design target feasibility



Identify performance bottlenecks

Finding parts of the design that limit overall performance

Reduce power consumption

Decreasing power usage to extend battery life

Improve reliability

Increasing robustness and lifetime of the chip

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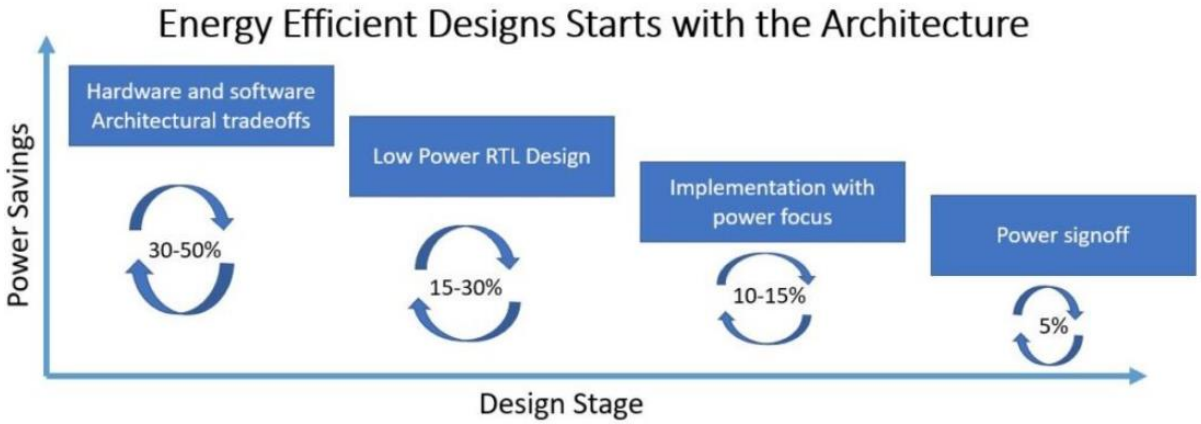
Key Factors for a Good ASIC Architecture

- Design decisions are based on targets, constraints and tradeoffs

- ASIC Microachitectural considerations:
  - Technology choice – early in the flow, manage variability, manufacturing
  - Performance-
    - Pipeline depth, throughput, potential hazards (e.g., data hazards, control hazards
    - Clock – fmax, timing-constraints, distribution
    - parallelize – Instruction, data, pipelines, workloads
    - multi-processor cores
  - Memory hierarchy
    - Data access, storage, cache levels, subsystems- optimize access times, bottlenecks

  - Power –clock gating, multiple power domains, operating modes, voltageand frequency scaling
  - Area, Utilization- Minimize area, higher density
  - Costs – design, manufacturing, rework

OpenROAD Advantages for Design Exploration



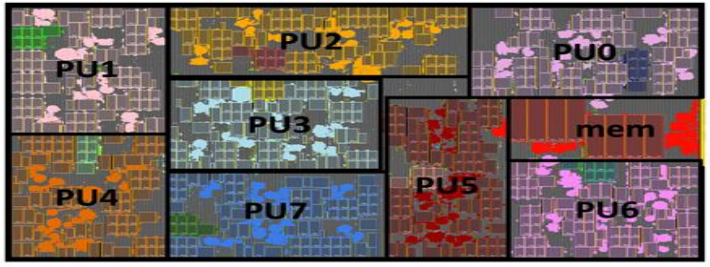
- Deploys "Shift left" Strategy in Semiconductor design - Shift important design designs earlier in the design stage for early problem identification, good starting point for PD, reduce iterations , accelerate TTM
  - Early design exploration for a good microarchitecture and overall accuracy
- Key advantages for hardware designers
  - Automation- tools, scripts, continuous integration to reduce manual effort
  - No licensing limits, limitless runs, distribution, parallelization
    - Some EDA tools are licensed based on the number of cores or machines they can use concurrently. This results in an inefficient use of processor cores and hence limits achievable speed in execution of EDA workloads that can be parallelized.
  - Rapid analyses of design decisions at any stage of the design

Design Partitioning – TritonPart large designs

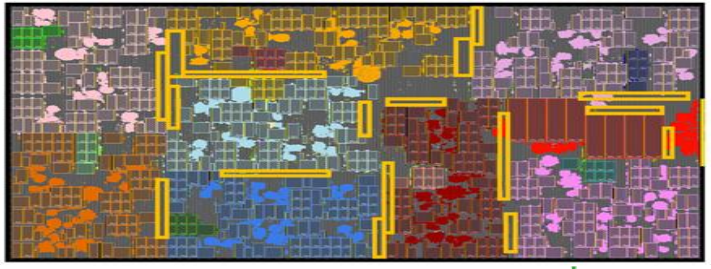
- **Goals**
  - Break design (hypergraph) into manageable sizes (partitions) to optimize design targets and ease design process
  - Reduce min cut size- number of nets crossing in between partitions
    - A smaller cut size typically leads to more compact and efficient layouts, with fewer signals crossing over , reducing wirelength, inter-block delays etc.
  - Balanced partition size with min cut- optimal number of vertices, hyperedges
  - Modern Partitioning algorithms (hMETIS) have intrinsic limitations
  - Scalability or large designs, large computation time, works well only for certain applications, sensitive to input parameters etc.
- **TritonPart/par** : State-of-the-art multiple-constraints driven partitioning
  - Supports both hypergraph and netlist partitioning
  - User-defined constraints priority – cost function
  - Timing-driven
  - Min-cuts
  - Balanced weights
  - Embedded- aware
- **OpenROAD advantages for design partitioning**
  - Designers can explore best ways to partition using multi-tool options to and achieve design objectives
  - Explore trade-offs across multi-objectives- area, performance, and power with priorities
  - Easy to design hierarchically and concurrently
  - Integrated into the flow- directly analyze impact on floorplan, Physical design
  - Scalable for large designs, multiple SoC architectures - for 3DIC and Chiplet based flows

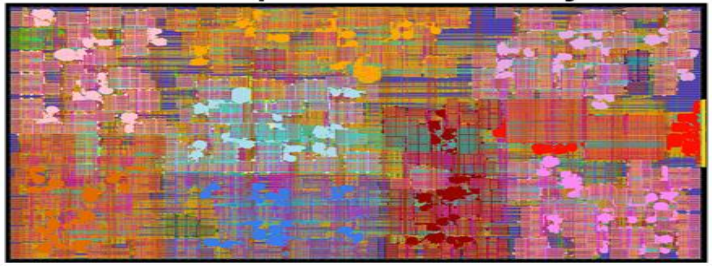
Automatic Macroplacement – Hier-RTLMP/mpl2

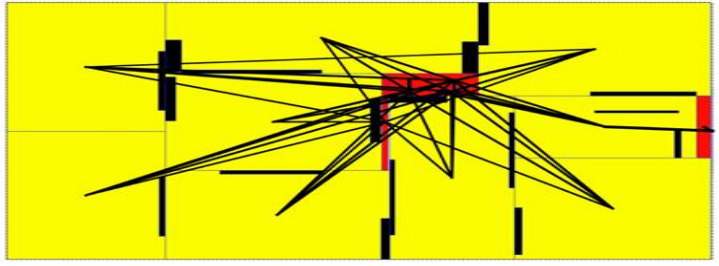
- Macro Placement is important for good design quality but difficult and often needs human expertise
- **Hier-RTLMP is a hierarchical macro placer that exploits logical awareness for faster and better placement in designs with a large > 100 macros**
  - Uses RTL logical hierarchy for dataflow by selectively merging and dissolving logical modules
  - Transforms **multi-level** hierarchy for physical implementation with full constraint-awareness (pin access, notch avoidance etc) for timing and routability
  - Automatic clustering- Two-step cluster shaping process for improved runtime and QOR



Post-placement layout


Pin access regions*


Post-routing layout


Top-level bus planning

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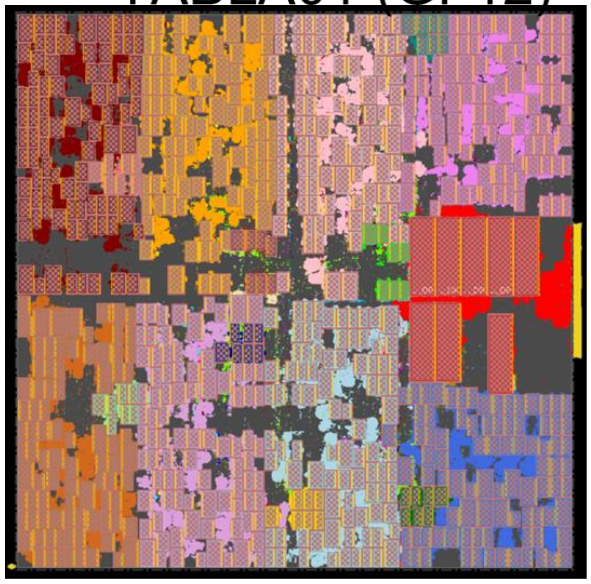
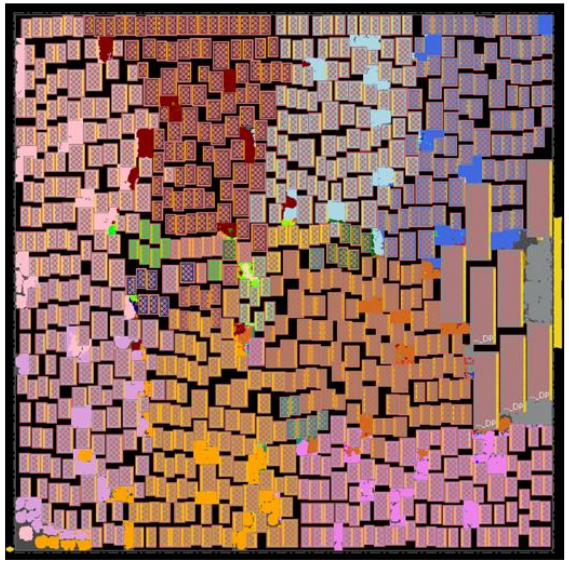
Early results are promising

- TABLA01 (GF12) **760** macros



Hier-RTLMP (postRoute)



Commercial Macro Placer (postRoute)

Macro Placer	Std Cell Area (mm^2)	Power (mW)	WNS (ns)	TNS (ns)
Hier-RTLMP	**0.160**	**640**	**-0.085**	**-0.417**
Comm	0.165	689	-0.370	-92.246

OpenROAD is optimal for Cloud-based EDA workloads

- COPILOT -Deploys cloud and compute resources intelligently to enhance runtime performance of the distributed router

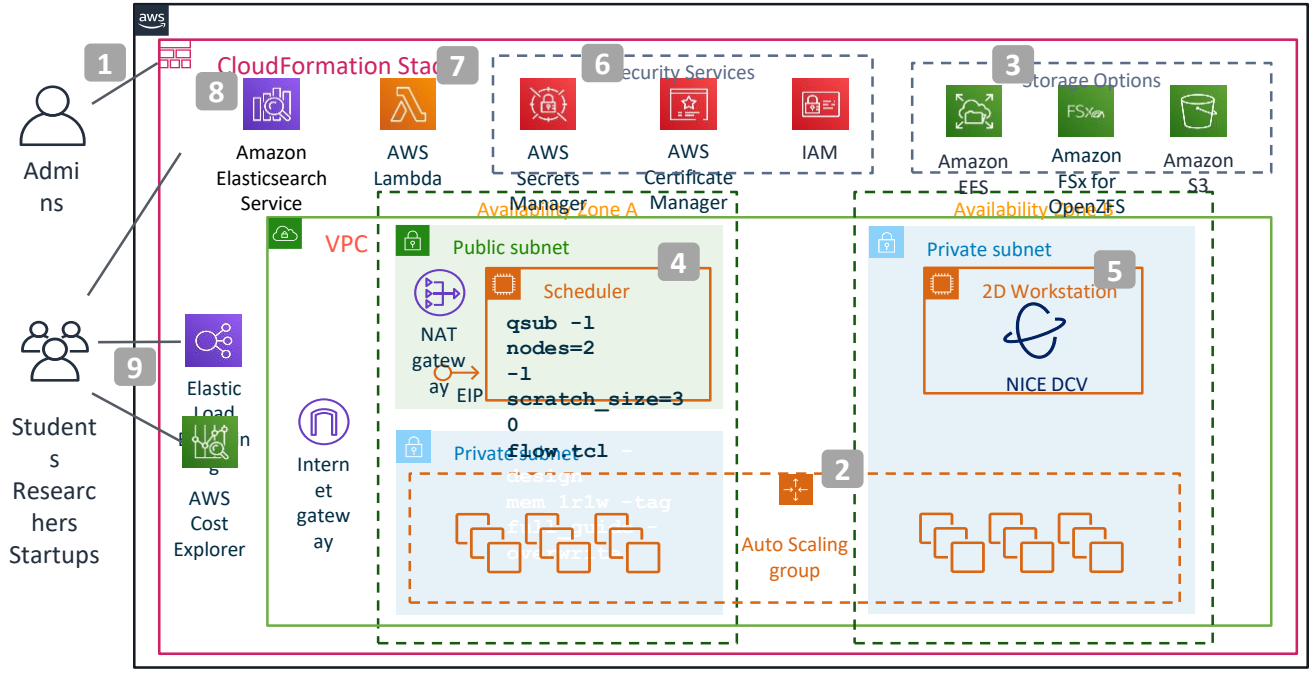
.

- Hyperscalers like AWS are pro-actively building use cases based pn open EDA

Open-Source Chip Design on AWS- source AWS

Solution location: https://aws.amazon.com/solutions/scale-out-computing-on-aws/

https://github.com/awslabs/scale-out-computing-on-aws



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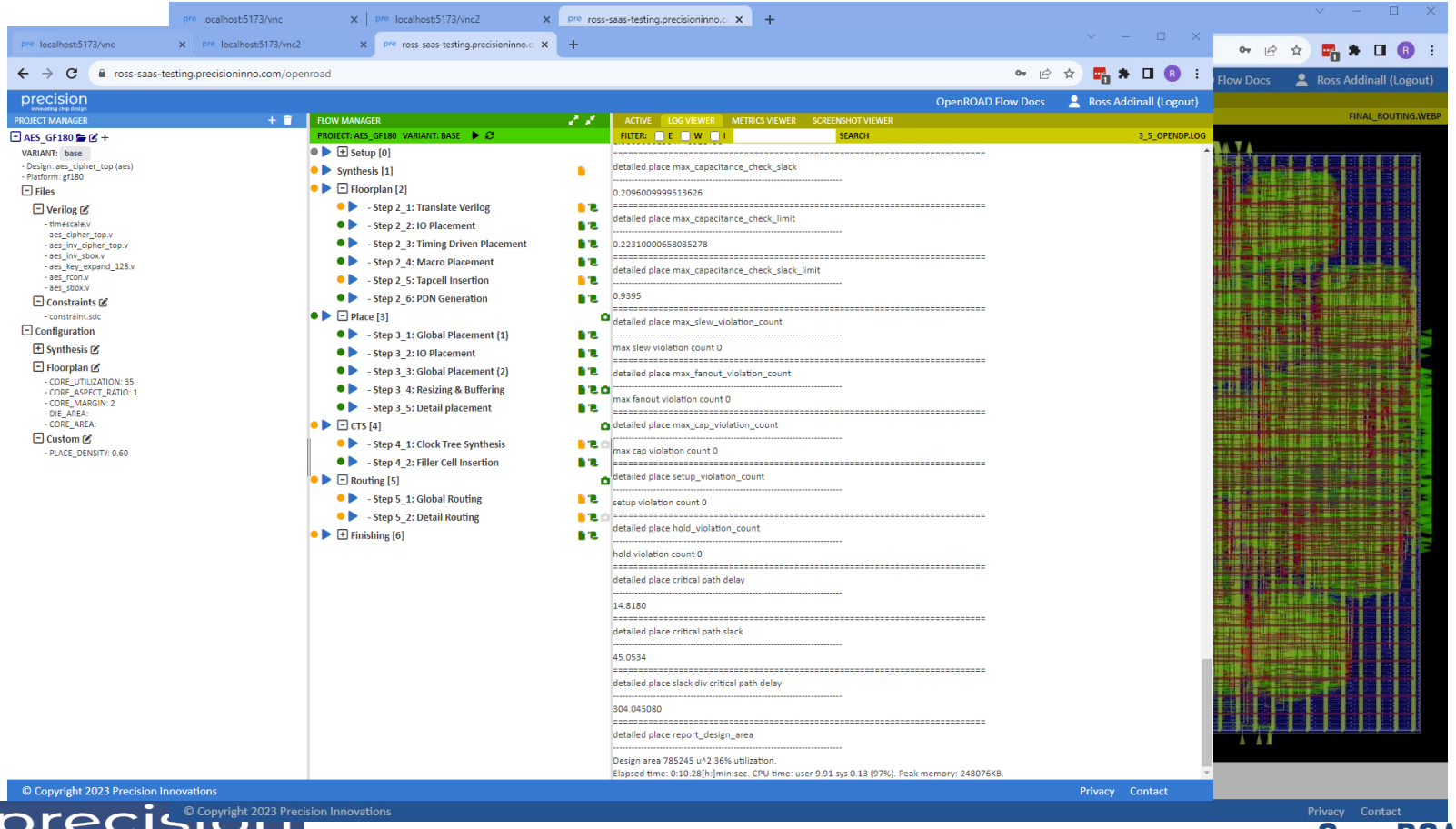
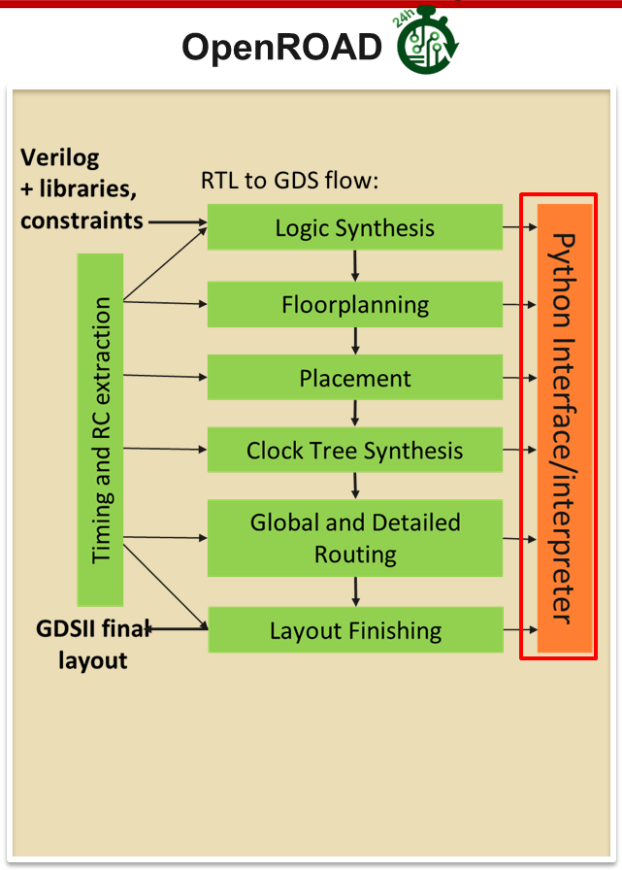
SaaS Site for Cloud-based Projects



Machine learning- Next Frontier for Innovation in Chip design

- Areas of Application:
  - **Design Space Exploration - AutoTuner**
    - Dimensionality reduction by feature selection
    - Flow stages- placement, routing
  - Flow Orchestration, script generation
  - Performance Prediction- PPAC
  - Multi-objective optimization- tradeoffs
  - Algorithmic exploration
  - Design assistance
  - Computational efficiency- resource allocation

- OpenROAD has the right infrastructure for ML-based design to enable and scale
  - Algorithmic expertise
  - Python based APIs – for faster data-generation
  - Metrics capture and tracking
  - Fostering creation of testbenches and other datasets for learning
  - Collaborative mindset with other researchers and industry tools
    - ChatEDA, NVIDIA CircuitOps



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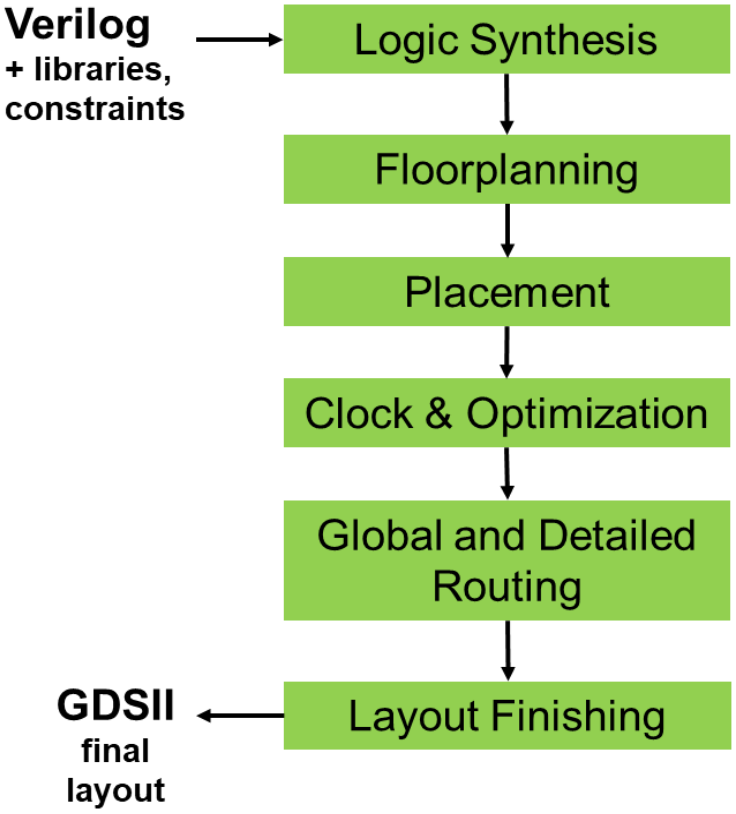
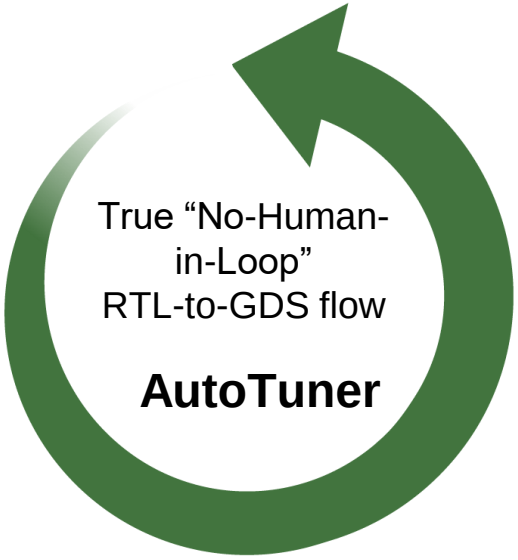
AutoTuner – ML-based Design Exploration





Best human-tuned flow
vs.
Auto-tuned (no-human-in-loop) flow

23% improvement in fmax
45% less power

Testcase: ibex lowRISC core in SKY130HD

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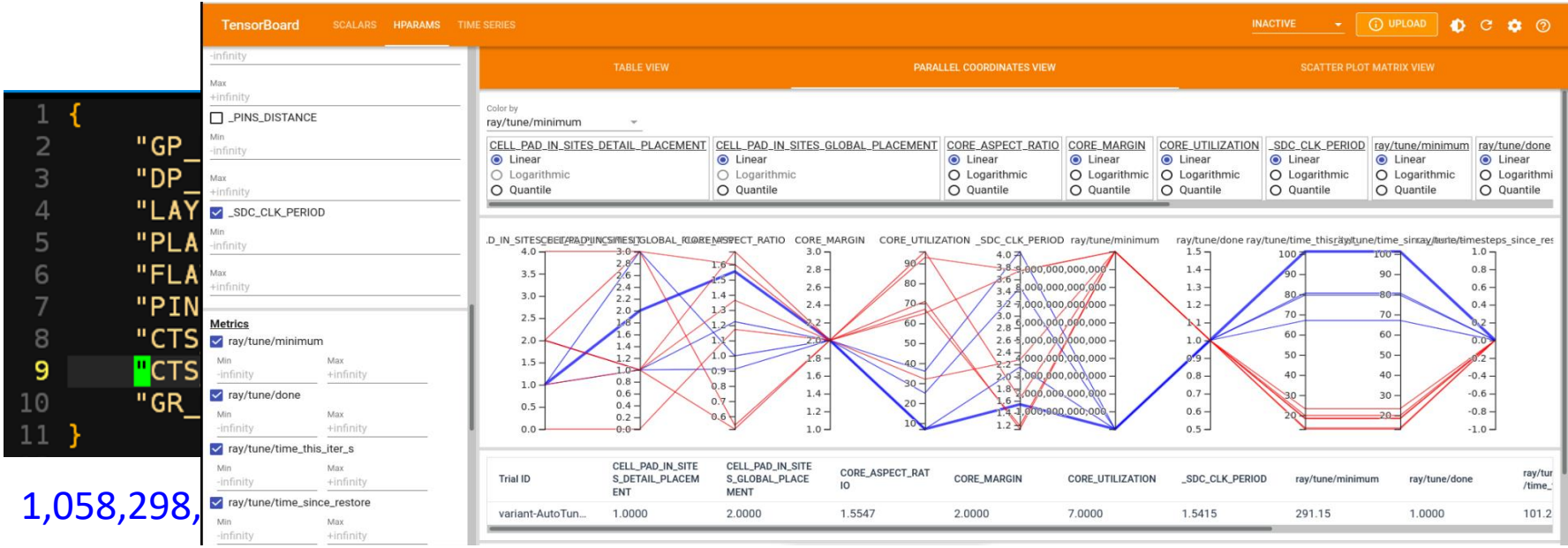
Automatic Hyperparameter Tuning

- Design space exploration depends on careful selection of goals and metrics- real-time monitoring and visualization
  - Design parameters and constraints determine optimization and accuracy of PPA

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    "PIN
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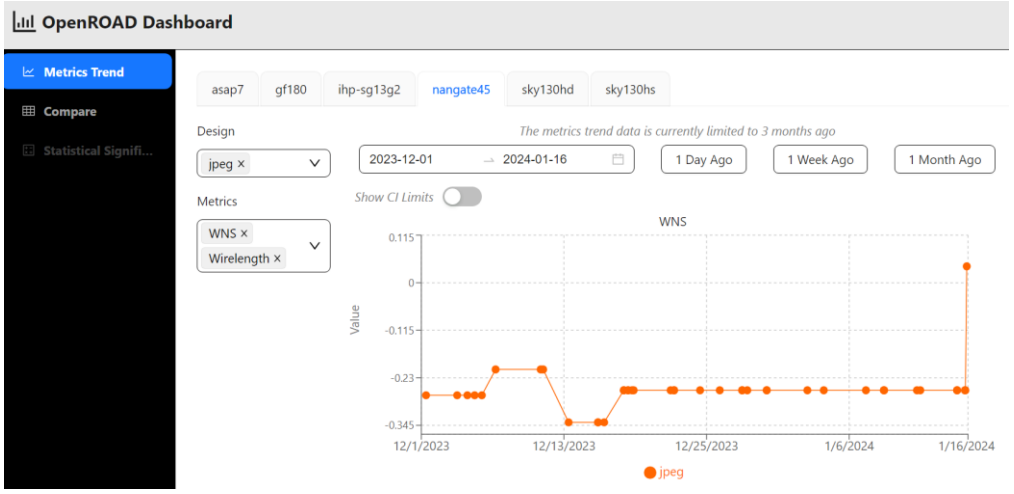
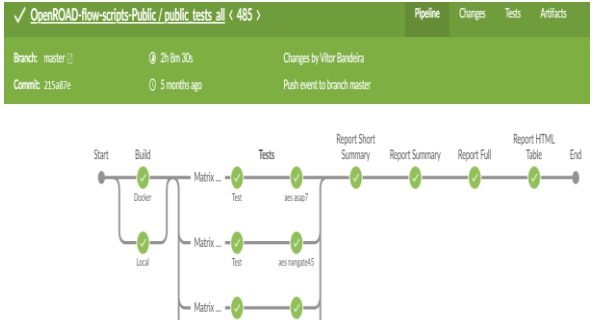
Continuous PPA improvement

- Track, analyze for continuous improvement
- https://dashboard.theopenroadproject.org/
- Continuous Integration and regression testing
  - The head is always stable
- Enable users to track PPA through Github Workflows
  - Tests will fail if PPA degrades
  - Results are updated proactively when they improve to lock in changes





Thanks

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