

# OpenROAD: A Foundation for IC Design Innovation and Workforce Development

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<https://theopenroadproject.org>

<https://github.com/The-OpenROAD-Project>



QUALCOMM arm



precision  
Innovating chip design

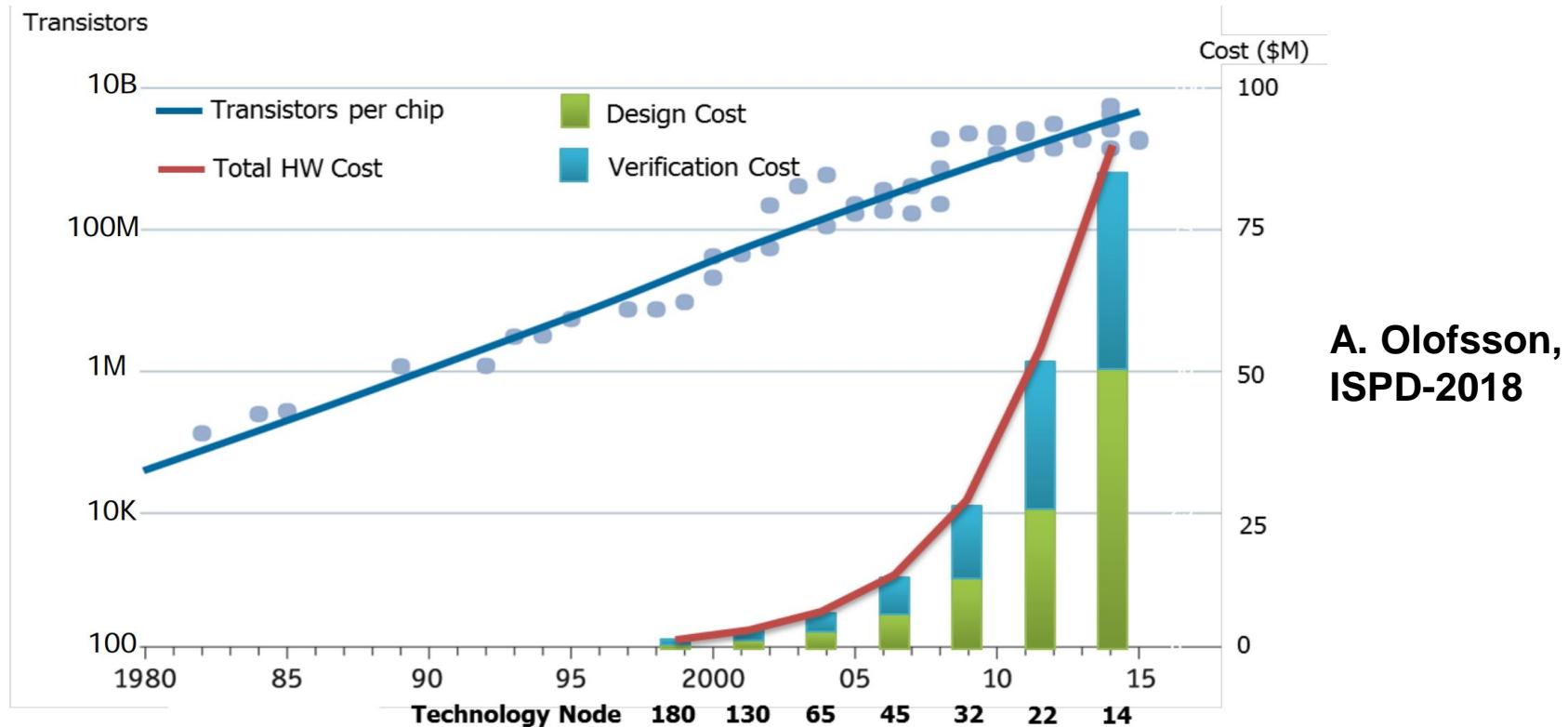
# Agenda

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- **What is OpenROAD ?**
- **How did we get here ? (The Journey)**
- **Where are we going ? (The Roadmap)**
- **Concluding thoughts**

# The Crisis of Hardware Design

- ASIC design in advanced nodes: barriers of Cost, Expertise, Risk



- Innovators can't evaluate PPAC metrics of their design ideas

# Design with Proprietary EDA: Need \$\$\$, Experts

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- Very sophisticated tools with 1000's of commands
- Vendor focus: performance, power, area for bleeding-edge customers
  - 20+ years of “hyperoptimization” in **two main platforms (= closed silos)**
- Need large teams of expert users, many manual steps
- Long project schedules: tool latencies, limited licenses, ...
- Significant project risks

# OpenROAD: June 2018 – December 2023

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- “Foundations and Realization of Open, Accessible Design”
- Funded by U.S. DARPA as part of the Electronics Resurgence Initiative (ERI). (UCSD = prime contractor)
- Mission: Democratize IC Design, Boost HW & EDA Innovation
  - Revitalize EDA
  - Contract: Deliver an Open-Source, RTL-to-GDS EDA system
  - 24-hour, no-human-in-loop, tapeout-clean layout in FinFET nodes



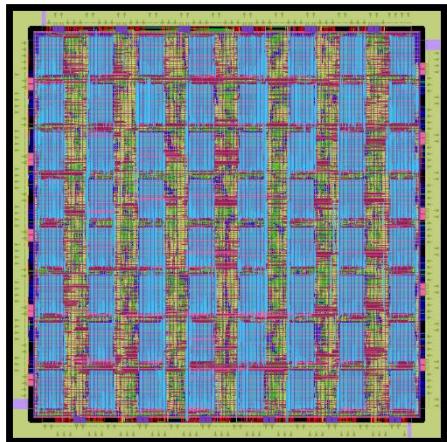
- Since 2020, Precision Innovations, Inc has been the key industrial developer: R&D, support, outreach
- Major support from Google (+ commercial engagements)

# OpenROAD: RTL-to-GDS, No Humans, 24 Hours

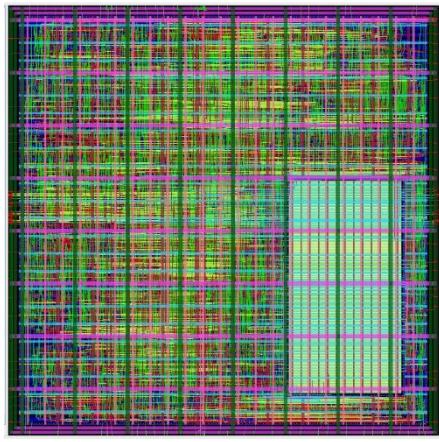
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- **FOCUS:** Ease of use and runtime
- **Directly attack the crises of design and innovation**
  - **Schedule barrier:** **RTL-to-GDS** in 24 hours
  - **Expertise barrier:** No-human-in-loop, tapeout GDS
  - **Cost barrier:** Open source (and, runs in 24 hours)
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

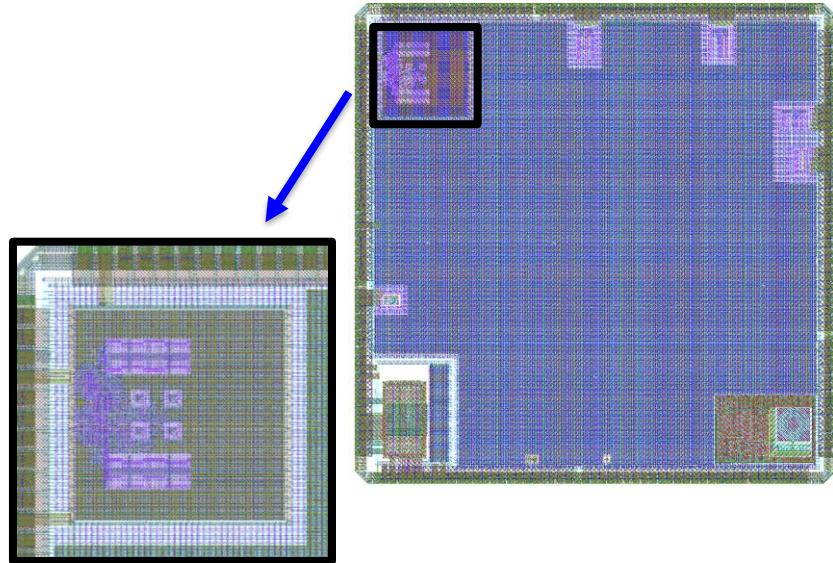
# Usage in Advanced Nodes



GF55 AI platform



GF12LP AI tile



OpenTitan SoC

Army Research Labs  
GF55, GF12LP

U. Michigan / FASoC  
GF12LP

# Today: Momentum, “Going Viral”



Data Prep

Synthesis (Yosys+ABC)

Floorplan

Placement

Clock Tree Synthesis

Routing

Static Timing Analysis

BEOL Fill

GDSII

DRC + LVS (KLayout)

## Supported Nodes

GF180nm

SKY130nm

SKY90nm

TSMC 65nm

GF55nm

Intel 22/16nm

GF12LP

- **Functionality:** 600+ tapeouts at 180-12nm
- **Community:** OpenROAD app has >20K commits from 94 contributors
- **Education and Workforce:** from high school to graduate level, extension
- **Researchers**
- **Small R&D teams, startups**

Proprietary Signoff



QUALCOMM arm



precision  
Innovating chip design

# OpenROAD Availability

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- The Project on GitHub
  - <https://github.com/The-OpenROAD-Project>
- The Flow
  - Automated full flow, built using tool components that are created for automation
  - <https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts>
- The Top-level Application
  - An integrated EDA tool focused on full automation
  - <https://github.com/The-OpenROAD-Project/OpenROAD>
- More!
  - Documentation:  
<https://openroad.readthedocs.io/en/latest/main/README.html>
  - Slack: <https://skywater-pdk.slack.com/archives/C0161A4A59V>
  - OpenTapeout video:  
<https://www.youtube.com/watch?v=wvPZREaP7E0&t=2652s>
  - See also: <https://theopenroadproject.org/videos/>

# Agenda

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- How did we get here ? (The Journey)
- Where are we going ? (The Roadmap)

MARCO [GSRC](#) Calibrating Achievable Design

## VLSI CAD Bookshelf 2

 Andrew B. Kahng, and Igor Markov

The bookshelf is a new electronic medium centered around *high-quality implementations of optimization algorithms* for VLSI CAD and information relevant to creating and evaluating such implementations. The project started with emphasis on Physical Design for VLSI and is now rapidly expanding to related areas.

*If you would like to contribute* : see [instructions](#)

• [Overview](#)

• [Bookshelf as a New Electronic Medium](#)

• Our talk at Berkeley on Sept 2, 1999 ([ppt](#)) ([ps](#))

• Stanford, Sept 24, 1999 (GSRC Workshop) ([ppt](#))

• San Jose, Dec 9, 1999 (GSRC Annual review) ([ppt](#))

• Los Angeles, Jun 4, 2000 (GSRC workshop) ([ppt](#))

• Los Angeles, Jun 8, 2000 (Design Automation Conference) ([ppt](#)), ([ps](#)), ([pdf](#)), • [Source Code Standards](#) (to be greatly expanded)

• Las Vegas, Jun 18 2001 (GSRC Workshop) ([ppt](#))

• Santa Clara, Sep 6 2001 (GSRC Workshop) ([ppt](#))

• [Submission \(release\) Standards](#)

• [New Data Formats](#) 

• [Copyright issues and support issues](#)

<https://vlsicad.eecs.umich.edu/BK>

# “Seeding an Ecosystem”

- ERI Summit 2018: Critical mass and critical quality
- ICCAD 2019: Open Source is a mirror
- VLSI-SoC 2020: If we build it, who will come?

## SWINGING FOR THE FENCES

- Must achieve critical mass and critical quality



11 of 13 IDEA TA-1 subtasks  
+ Base Technologies, Design

Common Infrastructure	Databases / Processing
✓ Cloud Infrastructure	
✓ Timing Analysis	
✓ Parasitic Extraction	
✓ Readers + Writers	
✓ Power and SI Analysis	
Layout Generators	Logic Synthesis
✓ Floorplanning	
✓ Placement	
✓ Clock Tree Synthesis	
✓ Detailed Routing	
✓ Layout Finishing	
Design	SoC Design Advisors

## Looking Into the Mirror of Open Source

(Invited Paper)

Andrew B. Kahng

CSE and ECE Departments, UC San Diego, La Jolla, CA 92093  
abk@ucsd.edu

## Open-Source EDA: If We Build It, Who Will Come?

Andrew B. Kahng

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La Jolla, CA 92093-0404 USA

abk@eng.ucsd.edu <https://vlsicad.ucsd.edu/~abk/>

All talks are at <https://vlsicad.ucsd.edu>

# If We Build It, Who Will Come? **Who is “We”?**

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*Lesson: Open-source EDA goes beyond academic research abilities*

- **Original proposal:** OpenROAD would be developed by Ph.D. students and post-docs at **five** universities
- Separately, students and post-docs at a sixth university would be the “internal design advisors”
  - Vision: span product engineering, expert user testing, corporate AE-like functions
- **Key point:** clear separation between “internal design advisors” and “tool developers” is built into OpenROAD
- Deliverables such as PPA assessment and calibration must come from design advisors

# If We Build It, Who Will Come? **Who is “We”?**

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- *What actually happened ...*
- By 9 months in, need for experienced EDA architect was clear → belt-tightening and non-DARPA gift funds allowed EDA veterans to be brought into the project



JAMES  
CHERRY



DIMITRIS  
FOTAKIS



MOHAMED  
SHALAN



TOM  
SPYROU



MATT  
LIBERTY



DON  
MACMILLEN

- Technical leadership and know-how: tool delivery, project management, infrastructure (DB, GUI, build/CI), key engines (STA, RCX)

Cho  
Moon



***Lesson: “We” must include professional  
EDA software developers and architects.***

# Skills and Mindset

- Strongest contributors have software skills **and** the right mindset
  - E.g., undergraduate and graduate students from CS backgrounds, in other countries (!)
  - Coached by EDA veterans
  - Obtain thesis topics, publications along the way

ICCAD-2020

## Contributions to OpenROAD from Abroad: Experiences and Learnings

Invited Paper

Mateus Fogaça<sup>1,3</sup>, Eder Monteiro<sup>3</sup>, Marcelo Danigno<sup>5</sup>, Isadora Oliveira<sup>1,3</sup>, Paulo F. Butzen<sup>1,4</sup> and  
Ricardo Reis<sup>1,2,3</sup>

<sup>1</sup>PGMicro/<sup>2</sup>PPGC, <sup>3</sup>Inst. de Informática, <sup>4</sup>Dep. de Elétrica, Universidade Federal do Rio Grande do Sul

<sup>5</sup>Centro de Ciências Computacionais, Universidade Federal do Rio Grande - FURG

{mpfogaca,emrmonteiro,isoliveira,reis}@inf.ufrgs.br,marcelo@furg.br,paulo.butzen@ufrgs.br

### Abstract

The OpenROAD project is an ambitious initiative seeking to develop an automated, open-source RTL-to-GDSII flow. To build its complex toolset, OpenROAD brings together a

### 1 Introduction

Modern technologies introduce an ever-increasing set of design rules and ever-more demanding power, performance, and area targets. The cost of IC design continues to increase,

# “Not Research As Usual”

- An **academic** research project, delivering **tapeout-clean** layout generation for **commercial** FinFET nodes in **permissive open source**, per **contract** with the U.S. Government
- → expectations, names, “signoff”, ...
- “**Not Research As Usual**”

**SWINGING FOR THE FENCES**

- Must achieve critical mass and critical quality

UCSD Qualcomm arm  
BROWN MICHIGAN UNIVERSITY OF MINNESOTA  
ILLINOIS UIUC

11 of 13 IDEA TA-1 subtasks + Base Technologies, Design

Common Infrastructure	Databases / Processing
✓ Timing Analysis	✓ Cloud Infrastructure
✓ Parasitic Extraction	✓
✓ Readers + Writers	✓
✓ Power and SI Analysis	✓
✓ Logic Synthesis	✓
✓ Floorplanning	✓
✓ Placement	✓
✓ Clock Tree Synthesis	✓
✓ Detailed Routing	✓
✓ Layout Finishing	✓
Design	SoC Design Advisors

First ERI Summit, July 2018

New: OpenROAD RTL-to-GDS v1.0 Expectations

30 Nov 2019

NEW: OpenROAD “Safe Names” Conventions, v1.0

10 Dec 2019

A post-route timing evaluation flow with OpenRCX is available !

14 Dec 2020

## AND MORE ...

- Open-sourcing of commercial timing engine
- Donated commercial tool source code base
- Industry advisors and technical contributors
  - Dr. Chi-Ping Hsu, Avatar
  - Dr. Noel Menezes, Intel
  - Dr. Richard Ho, Google
  - ...
- Worldwide outreach, engagement, support ...

Parallax software



National  
Taiwan  
University



KAIST



UNIVERSIDADE FEDERAL  
DO RIO GRANDE DO SUL



CUHK  
香港中文大學



SEOUL  
NATIONAL  
UNIVERSITY



intel



AVATAR  
Integrated Systems



# And More Dimensions: The Next Generation

- Help with curriculum development, sharing, mentoring !

## Semiconductor Engineering certificate program objectives

- Implement Verilog modeling of digital logic
- Write assertions for formal verification using SystemVerilog
- Build an advanced UVM verification environment
- Understand and implement DFT concepts in an ASIC design
- Complete practical designs with Xilinx FPGAs
- Implement a design from RTL to GDS

## Access to premier tools

Using premier industry tools from Cadence, OpenROAD, Siemens, and Synopsys, you'll learn front-end and back-end ASIC design and leave the classroom ready to apply new skills at your job.



before



VSD-IAT CLOUD BASED  
5 DAY WORKSHOP ON  
**ADVANCED PHYSICAL DESIGN**  
**USING OPENLANE/SKY130**

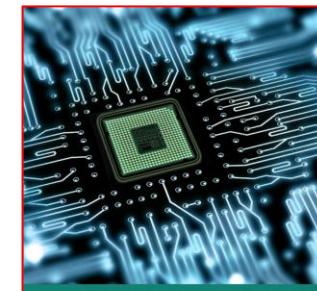
OPENLANE BY EFABLESS  
SKY130 PDKS BY GOOGLE/SKYWATER

**STEM workshops**



Learn to design your own chips

In March 2020 I started getting interested in Open Source ASIC tooling.



## Why teach Chip Engineering?

The design and creation of semiconductor products is an exciting field that requires a high-demand skill set in the industry. As a first of its kind, high school students will learn how to design microchips, learn and apply software methodologies to create hardware designs including logic representation in binary systems, basic building blocks and structure of digital, analog and mixed-signal components. You will learn the use of Verilog - a popular hardware description language, open-source software such as OpenROAD and the main stages of building a chip, from specification, testing and to manufacturing.

These are very important skills that lead to fulfilling and long term opportunities -- jobs in industries -- from building toys, cellphones, cars, thermostats and military systems. Entry level pay can start at \$48K + per year depending on location, position and background. So sign up fast!

INPUT	OUTPUT
0 0	1
0 1	1
1 0	1
1 1	0

Foundational Path



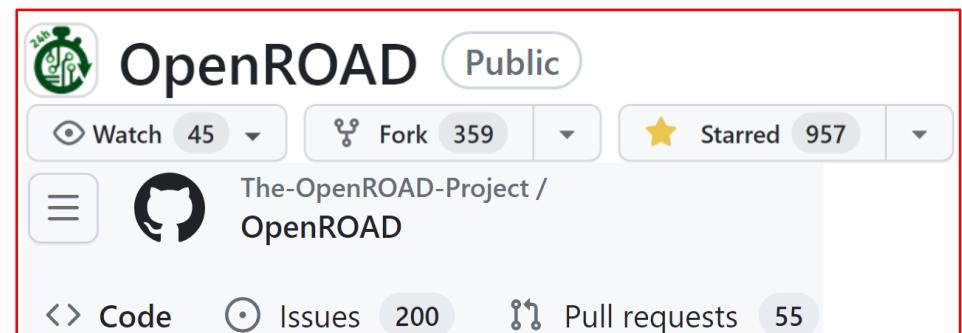
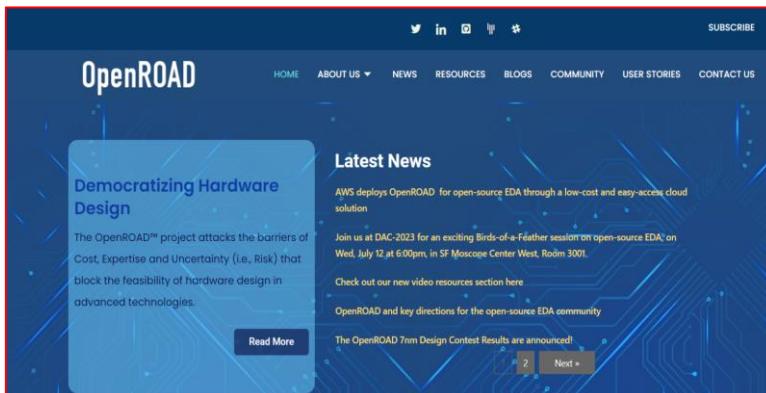
Partial Path



OpenROAD  
Full Path

# And More Dimensions: Community

- Join the community !
  - Novice to Expert
  - Applications: Trust, 3DIC, AI/ML, ...



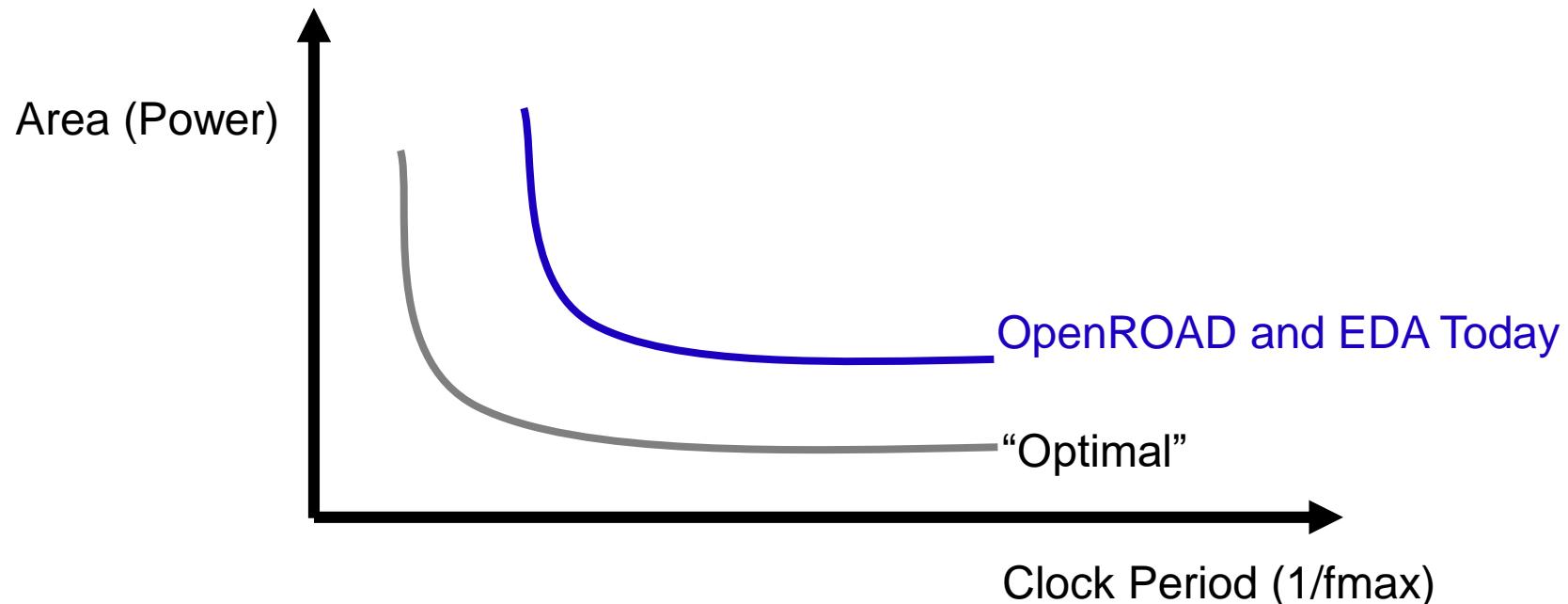
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- What is OpenROAD ?
- How did we get here ? (The Journey)
- Where are we going ? (The Roadmap)
  - Future EDA: Better, Faster Optimization + Machine Learning !

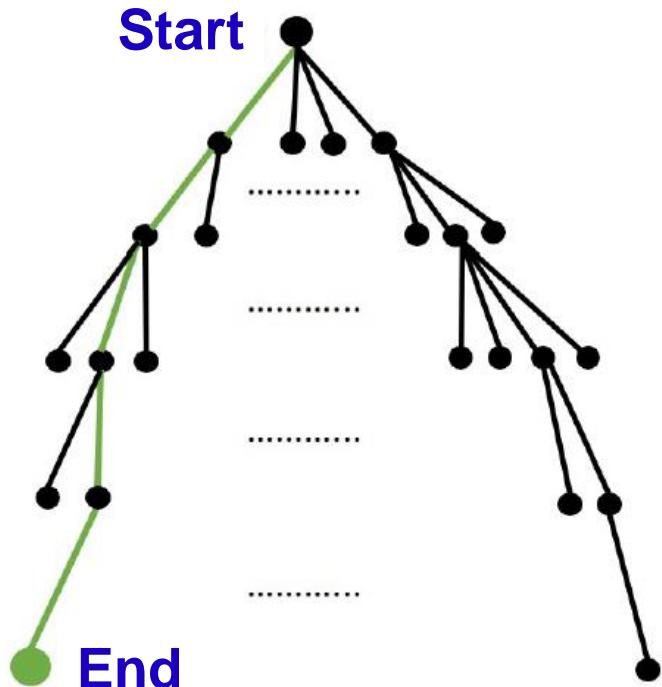
# IC Design and EDA = Optimization

- Optimization of Power, Performance, Area, Cost...  
... within design resources !



# Challenge: IC Design “Lives in a Box”

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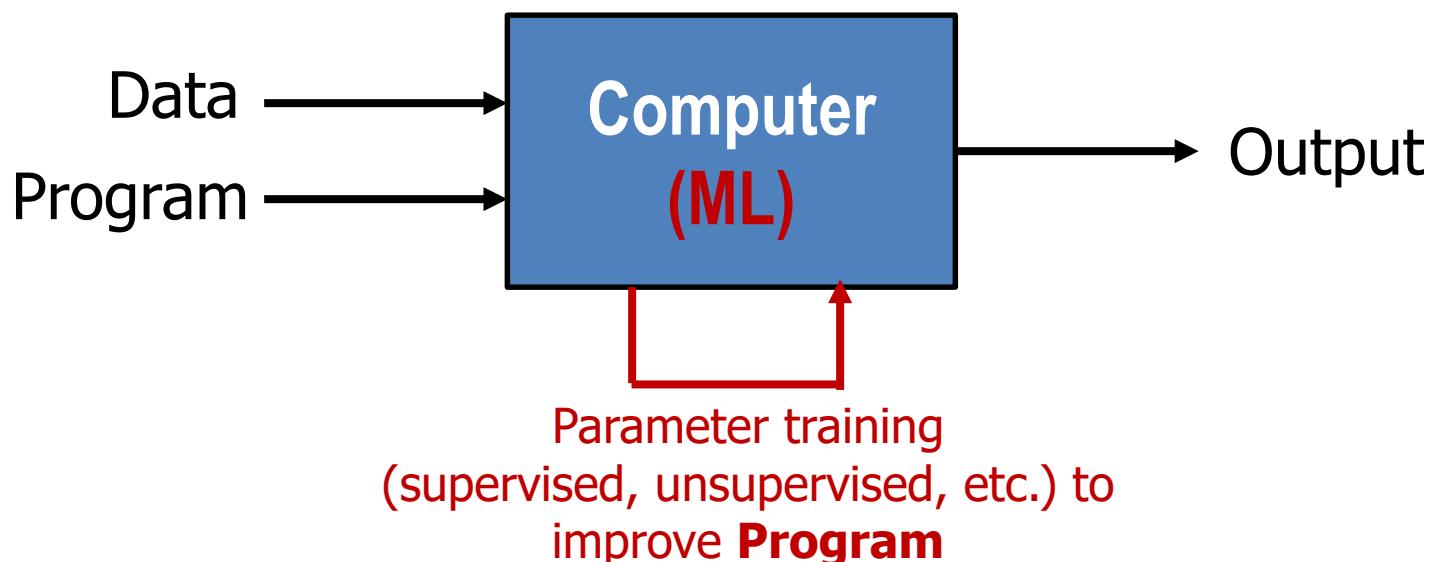


Huge space of trajectories: architecture, enablement, IPs, tools, manual fix, ...

- Start to End: expensive!
  - O(year) for product
  - O(weeks) for SP&R and Opt
- Goal: best possible End
- Constraint: stay in “Box”
  - {compute}
  - X {licenses}
  - X {people}
  - X {weeks}

# Machine Learning

- [Simon et al.] Learning is any process by which a system improves performance from experience
- [Mitchell et al.] Machine learning is the study of algorithms  $\langle P, T, E \rangle$  that
  - Improve performance  $P$  at task  $T$
  - Using training data (experience)  $E$



# ML for EDA and IC Design: What

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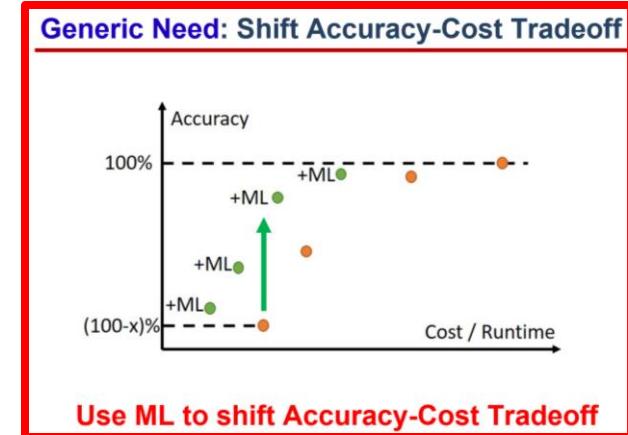
- **Predict**
  - Will RouteOpt finish with clean signoff, <1000 DRVs by tomorrow night?
- **Classify**
  - Out of these 50 floorplans + timing budgets, which 3 should go into trial SP&R?
- **Estimate**
  - How many hold buffers will the tool eventually add into this post-CTS layout?
- **Guide / advise**
  - What P&R tool setup/script will obtain the best QOR within next 36 hours?
- **More broadly: answer any question that is difficult for humans**
  - Google Brain, 2020: “super-human macro placement” on arXiv
  - **Overarching: “intelligent flow”, “automated super-human expertise”**
- **More directly: regressions and image classifications**
  - LSF queues, lithography hotspots, ...

# ML for EDA and IC Design: Why

- A. You need models to have predictions
- B. You need predictions to leverage in exploration
- C. What you can't predict, you guardband
- D. What you don't explore, you leave on the table
- E. C and D are bad for product quality and schedule

- We are in an **Era of Optimization**
  - Look for ML to win quality, schedule, cost
  - E.g., reduce analysis runtime, miscorrelation

→ We hope that ML will bring Scaling



# 4 Aspects of ML for EDA and IC Design

## 1. Mechanization and Automation

*Create super-human robot engineers*

## 2. Orchestration of Search and Optimization

*Optimize the use of N robot engineers*

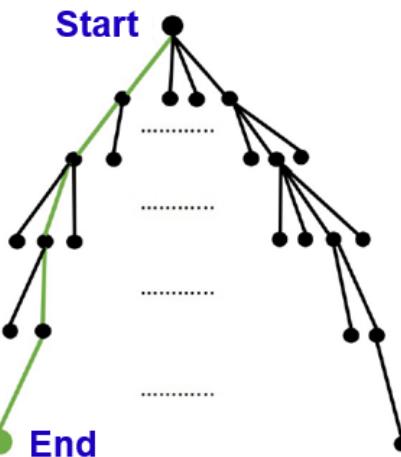
## 3. Pruning via Predictors, Models

*Predict design-specific tool outcomes*

*Prune “doomed runs”*

## 4. From Reinforcement Learning to Intelligence

*Target: “MLDA”, “self-driving tools and flows”, “superhuman”*



Huge space of trajectories: architecture, enablement, IPs, tools, manual fix, ...

The METRICS Initiative

Recent Updates

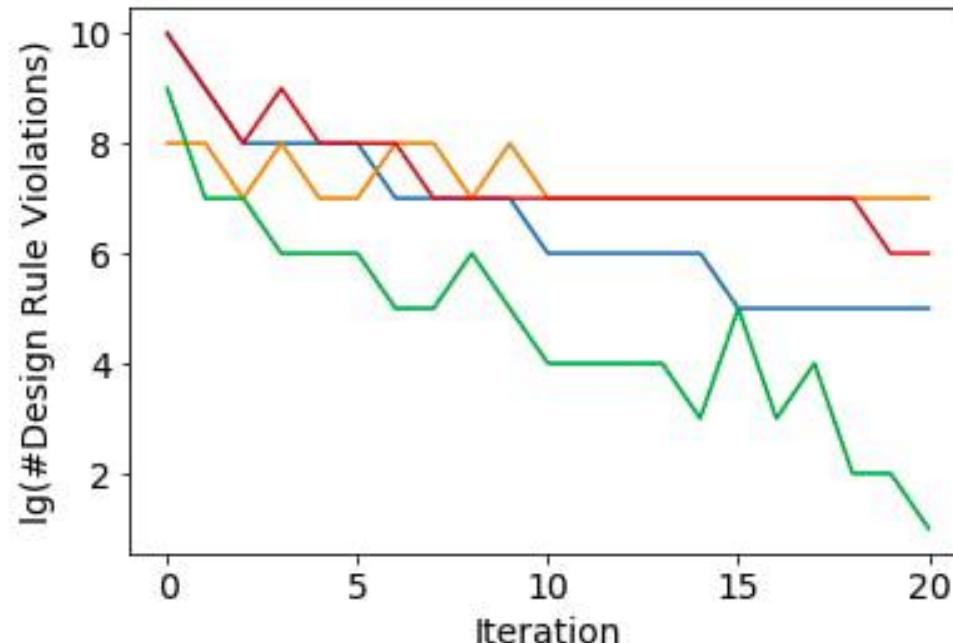
- [Survey \(1st draft\)](#) for design quality and productivity ([the multiple-choice version](#))
- [Reduced survey \(2nd draft\)](#) for design quality and productivity that is distributed at June 2001 GSRC workshop
- [Updated survey \(3rd draft\)](#) for design quality and productivity that reflects the discussion at June 2001 GSRC workshop
- [Workshop notes](#) for METRICS discussion at June 2001 GSRC workshop
- [List of prediction/estimator models](#) enabled by METRICS System
- [DAC02 Birds-of-a-Feather meeting summary](#) (June 12, 2002)

<https://vlsicad.ucsd.edu/GSRC/metrics/>

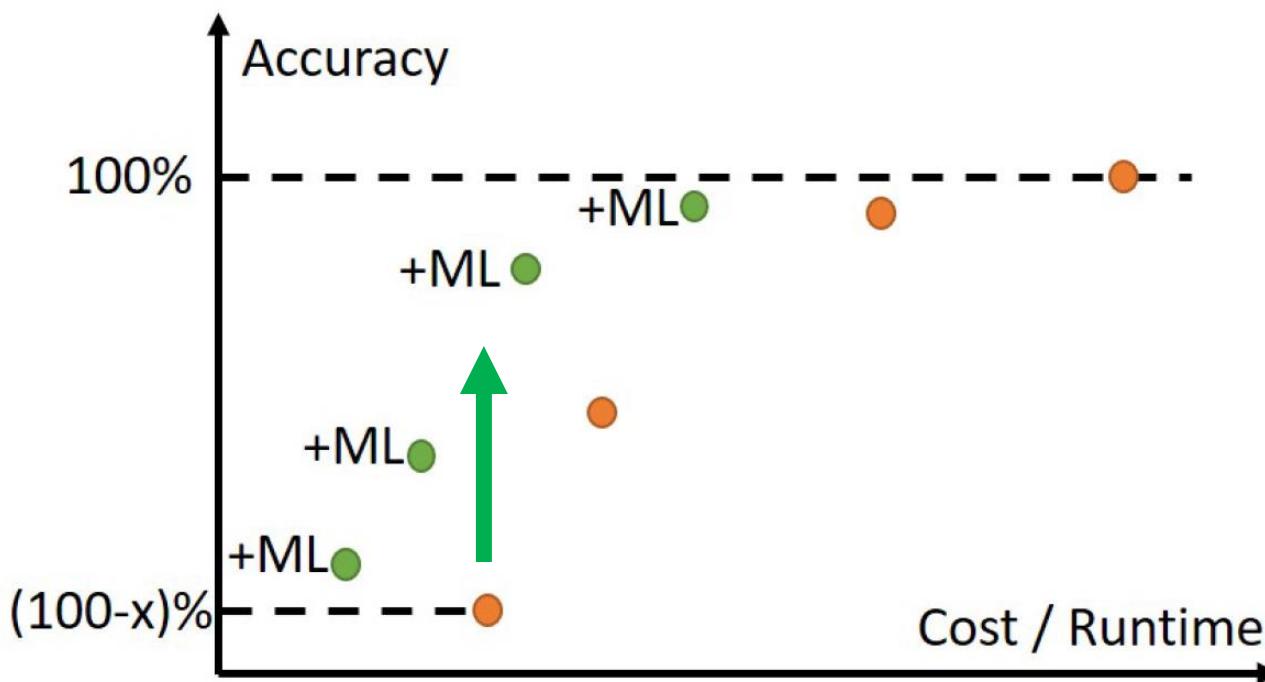
# Generic Need: Predict Doomed Runs

Figure from  
[link](#) [link](#) [link](#)

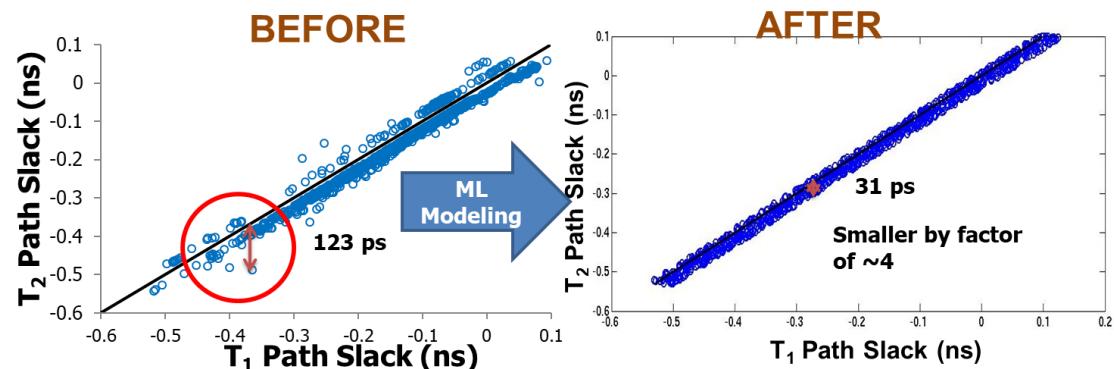
- Example: progression of DRC violations in commercial router
- Simple strategy: **track and project key metrics as time series**
- Example method: use Markov decision process (MDP): “GO” vs. “STOP” strategy card to terminate “doomed runs” early



# Generic Need: Shift Accuracy-Cost Tradeoff

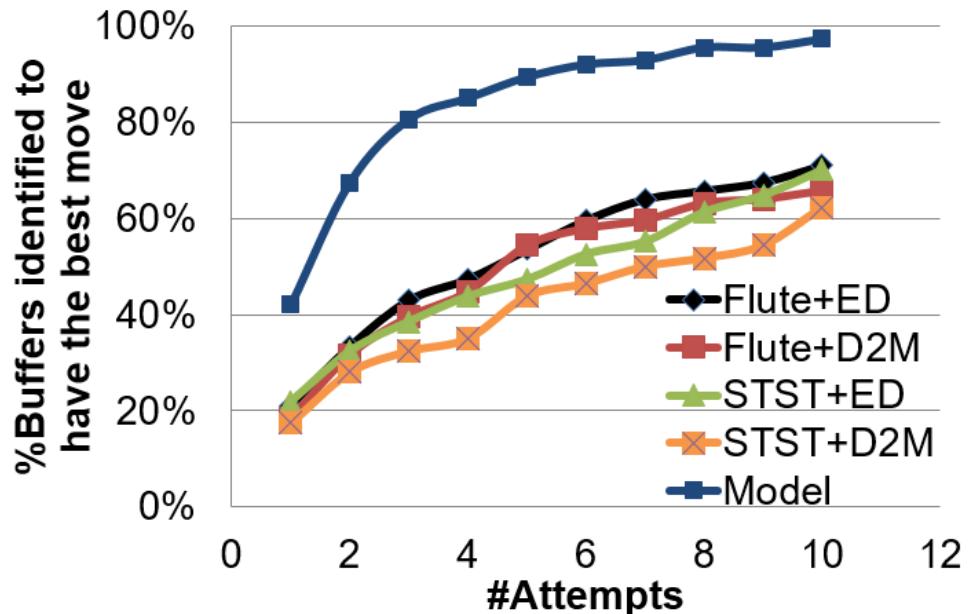
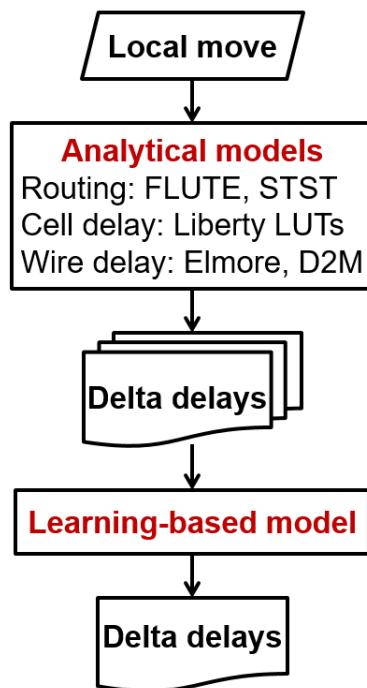
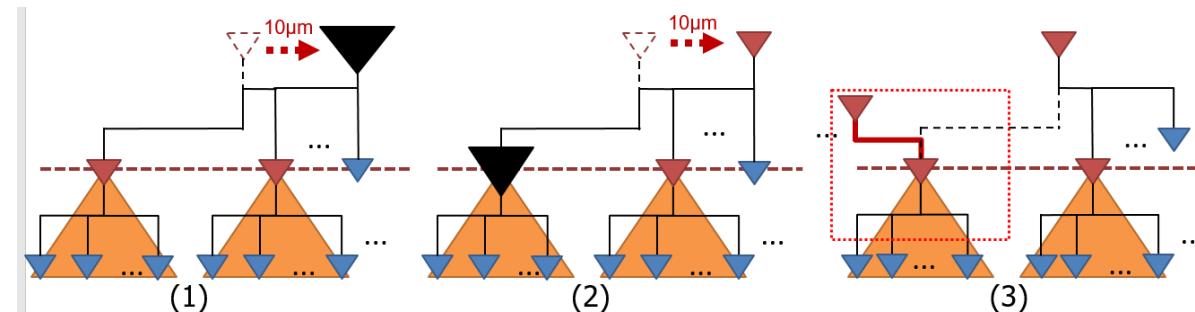


Use ML to shift the Accuracy-Cost Tradeoff



# Generic Need: Model-Guided Optimization

- Which CTS tweak will improve skew variation across corners?

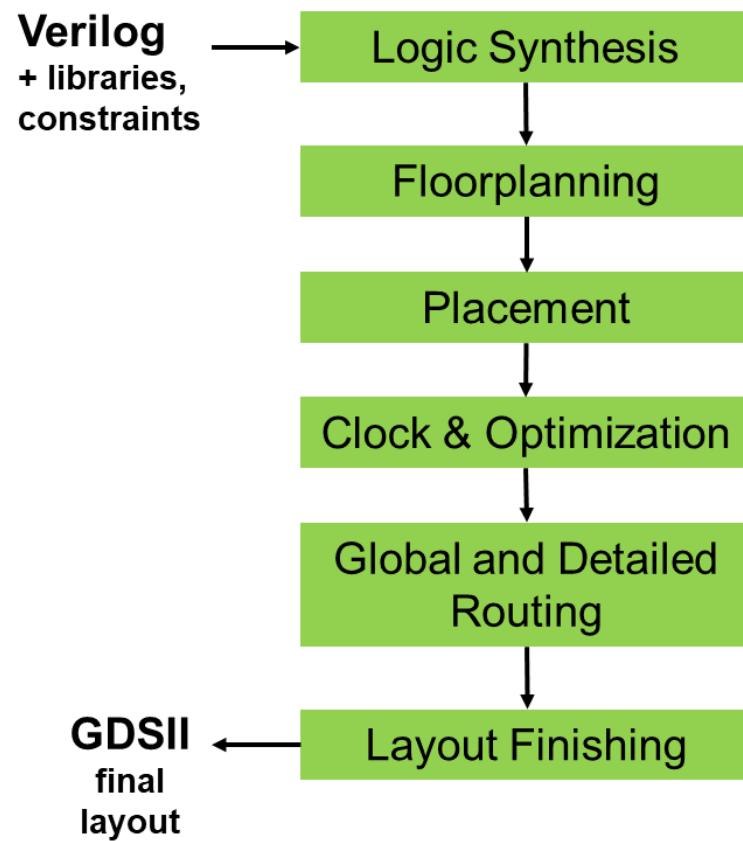


# Agenda

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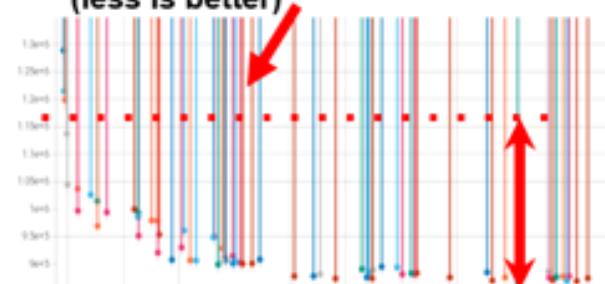
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- Where are we going ? (The Roadmap)
  - Future EDA: Better, Faster Optimization + Machine Learning !
  - OpenROAD Tool Development

# Direction #1: Cloud, Machine Learning



- What if tool licenses are unlimited?  
“COPILOT” = Cloud Optimized Physical Implementation using OpenROAD Technology
- ML challenge: predict failure and intervene
- + low-hanging fruits such as AutoTuner

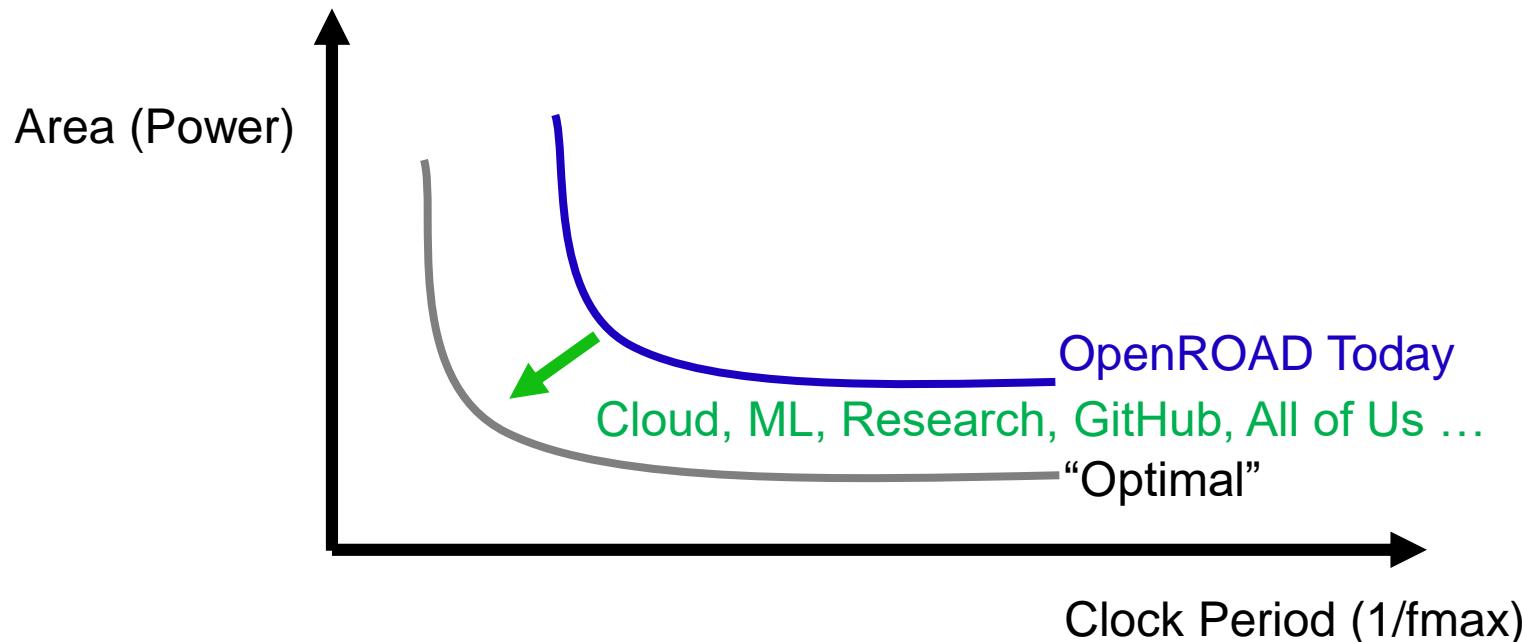
Default flow score = 1,174,346  
Our Best Score = 855,373  
(370 trials in total 500 #trials)  
(less is better)



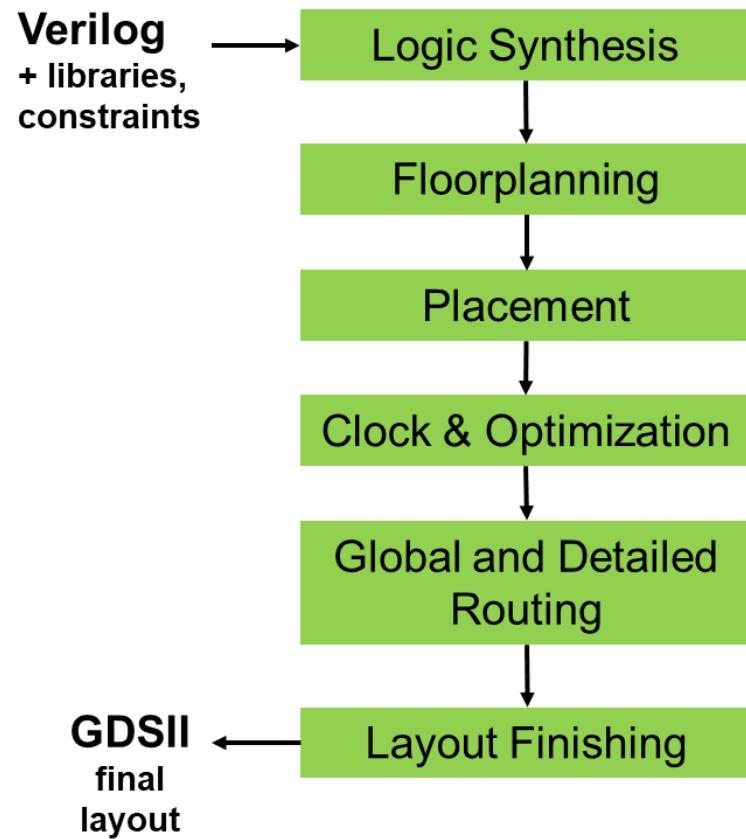
Improvement  
**WL** 1003801um → 843258um (**-16%**)  
**Effective CP** 20.935ns → 16.185 ns (**-23%**)  
**Total power** 0.024 W → 0.0133 W (**-45%**)

# IC Design and EDA = Optimization

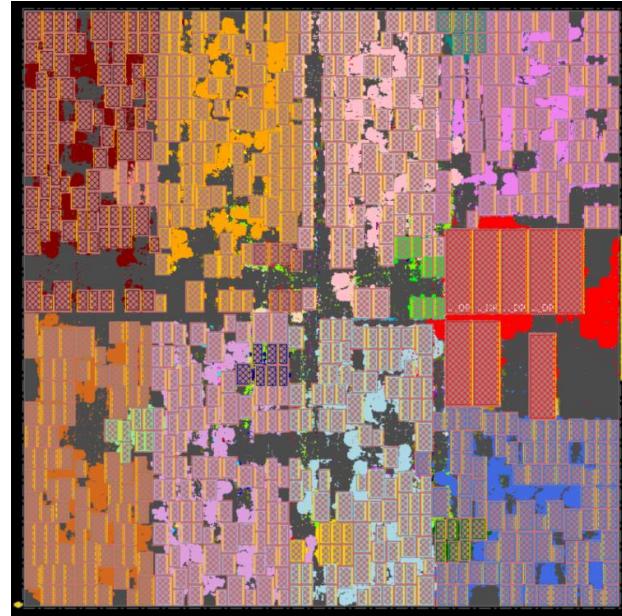
- Optimization of Power, Performance, Area, Cost...  
... within design resources !  
... boosted by AI and Machine Learning !



# Direction #2: Early Design Exploration

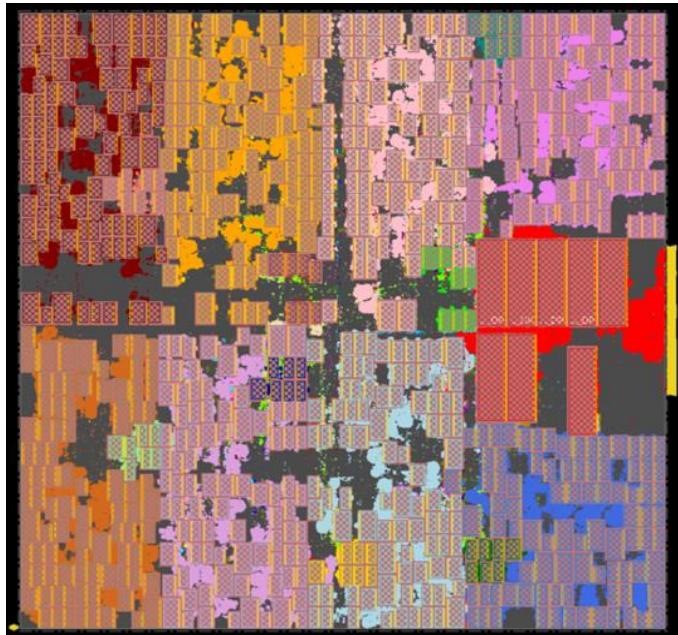


- Can we better explore architecture and System-on-Chip floorplan design spaces?
- Hier-RTLMP: /src/mpl2
  - RTL and dataflow-driven, human expert-like

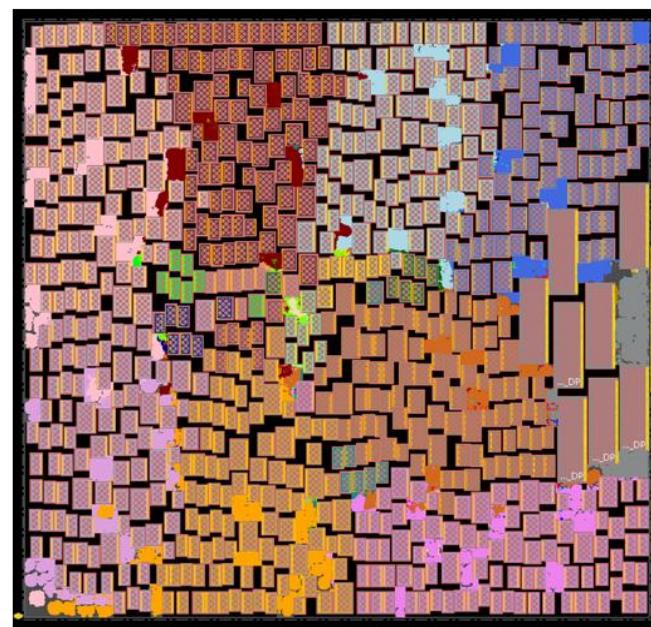


# Hier-RTLMP vs. Commercial Macro Placer

- TABLA01 (GF12) 760 macros



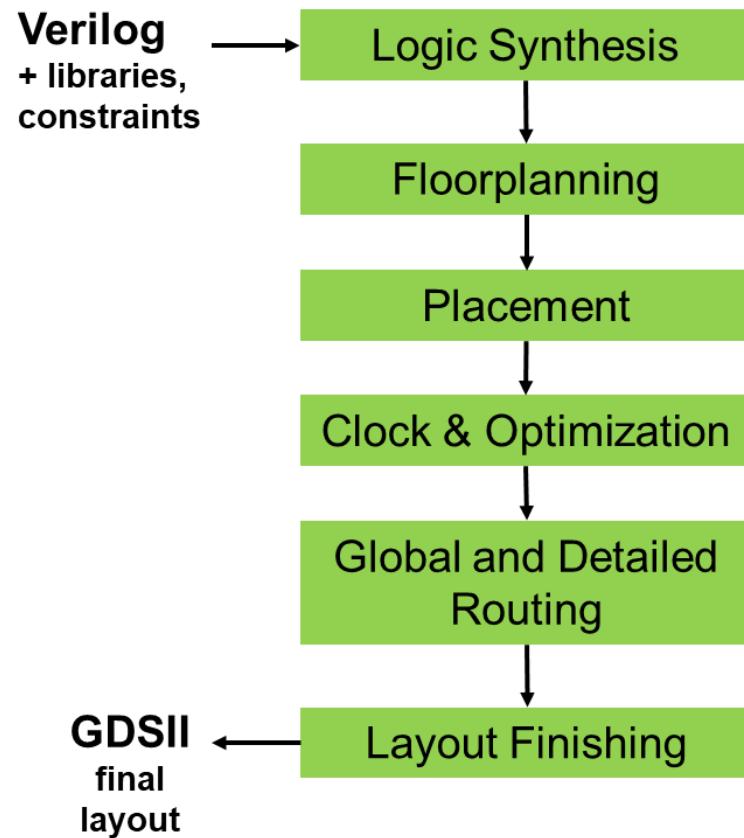
**Hier-RTLMP (postRoute)**



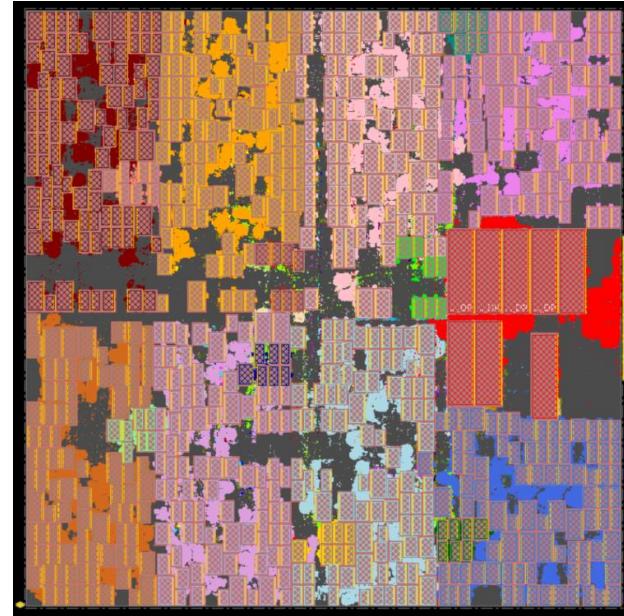
**Commercial Macro Placer (postRoute)**

Macro Placer	Std Cell Area (mm <sup>2</sup> )	Power (mW)	WNS (ns)	TNS (ns)
<b>Hier-RTLMP</b>	<b>0.160</b>	<b>640</b>	<b>-0.085</b>	<b>-0.417</b>
<b>Comm</b>	0.165	689	-0.370	-92.246

# Direction #2: Early Design Exploration



- Can we better explore architecture and System-on-Chip floorplan design spaces?
- Hier-RTLMP: /src/mpl2
  - RTL and dataflow-driven, human expert-like

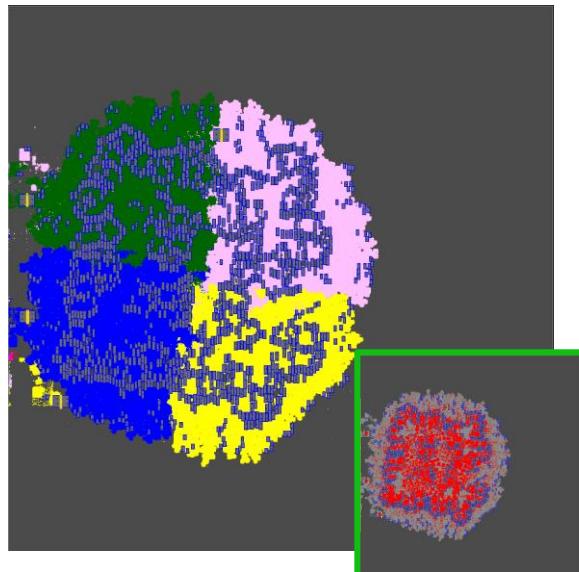


- TritonPart: /src/par
  - Timing- and constraint-driven partitioner
  - Displaces hMETIS, KaHyPar

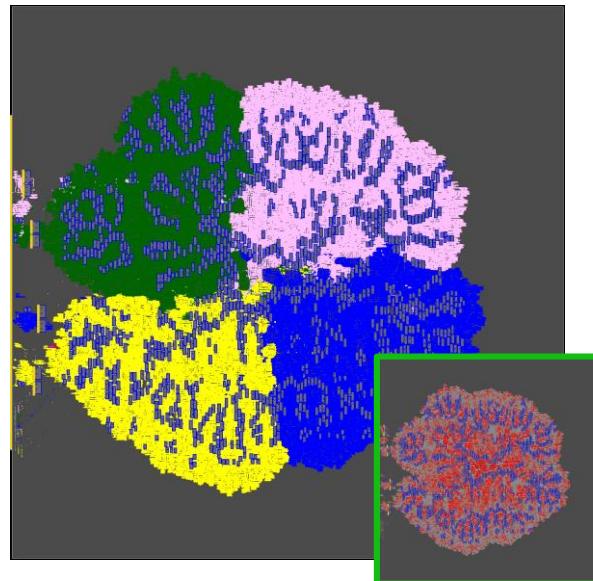
# New: Fast Mixed-Size Global Placement

	Runtime (s)	HPWL (m)	eGR WL (m)
RePIAce	65381	325	404
Comm	24561	414	478
New	<b>1808</b>	<b>327</b>	<b>407</b>

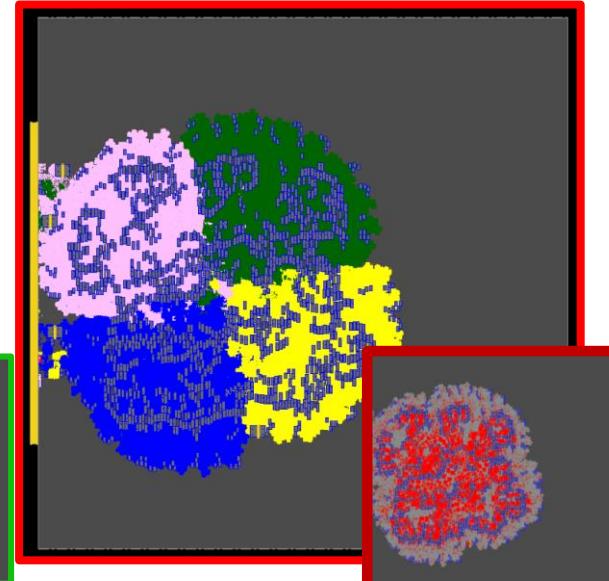
OpenROAD RePIAce



Commercial



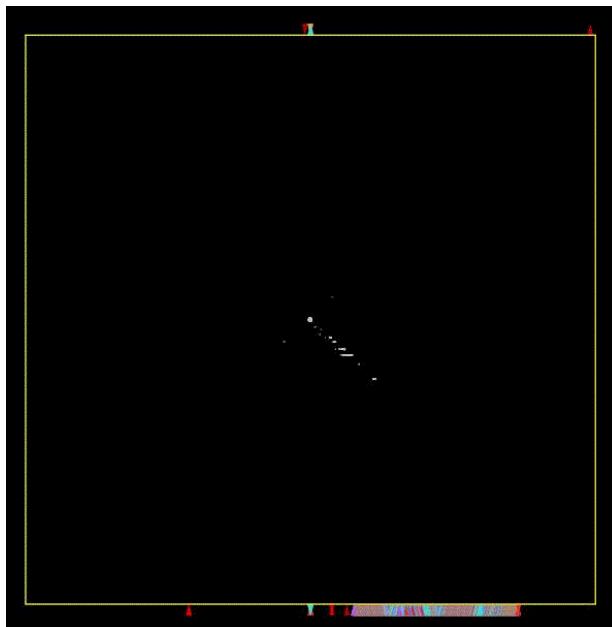
New



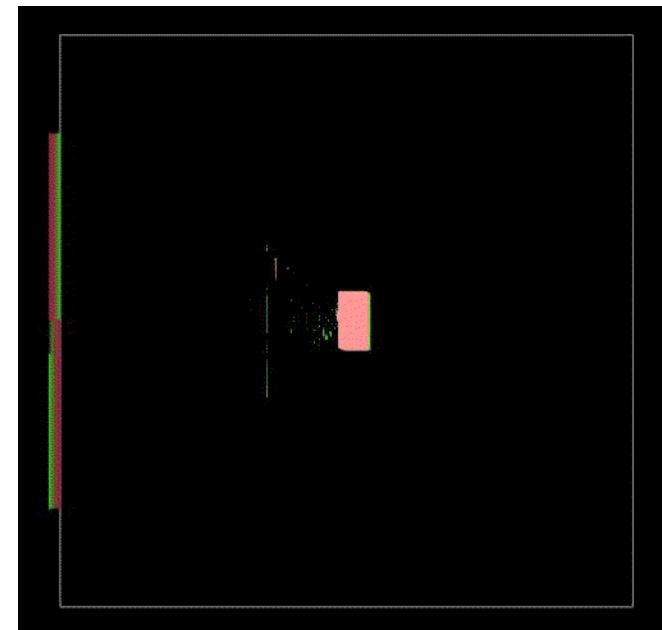
**Testcase:** MemPool Cluster, ETH Zurich (**9.5M cells, 1296 macros in NG45**)

# New: 3D Timing-Driven Placement

- Database, hierarchy support: **OpenDB**
- Partitioning: **TritonPart**
- Global placement: **RePIAce**
- Detail placement: **OpenDP**
- Hybrid-bond placement: **RePIAce** and **OpenDP**
- Timing-driven: **OpenSTA**



**Netcard: 274K instances,  
290K nets**



**Ariane: 126K instances  
(133 macros), 142K nets**

# Agenda

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- What is OpenROAD ?
- How did we get here ? (The Journey)
- Where are we going ? (The Roadmap)
  - Future EDA: Better, Faster Optimization + Machine Learning !
  - OpenROAD Tool Development
  - ML Enablement with OpenROAD

# OpenROAD as an ML for Chip Design Playground

<https://github.com/NVlabs/CircuitOps>



CircuitOps graph creation using OpenROAD DB APIs

Verilog  
+ libraries,  
constraints

RTL to GDS flow:

Logic Synthesis

Floorplanning

Placement

Clock Tree Synthesis

Global and Detailed  
Routing

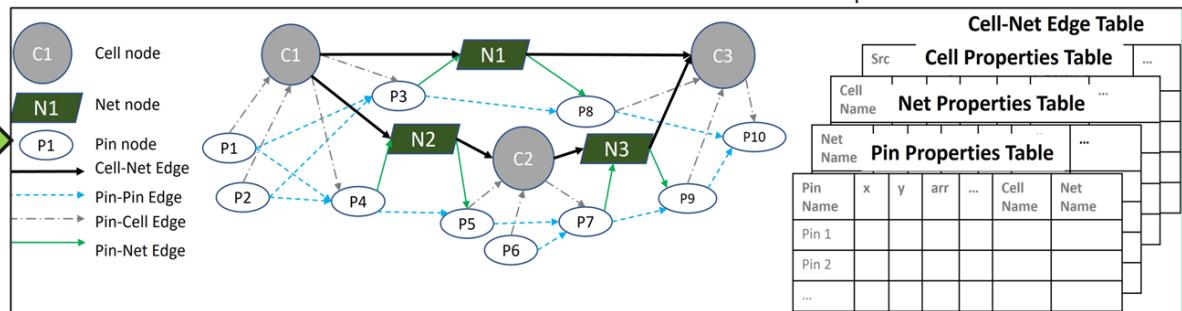
Layout Finishing

Timing and RC extraction

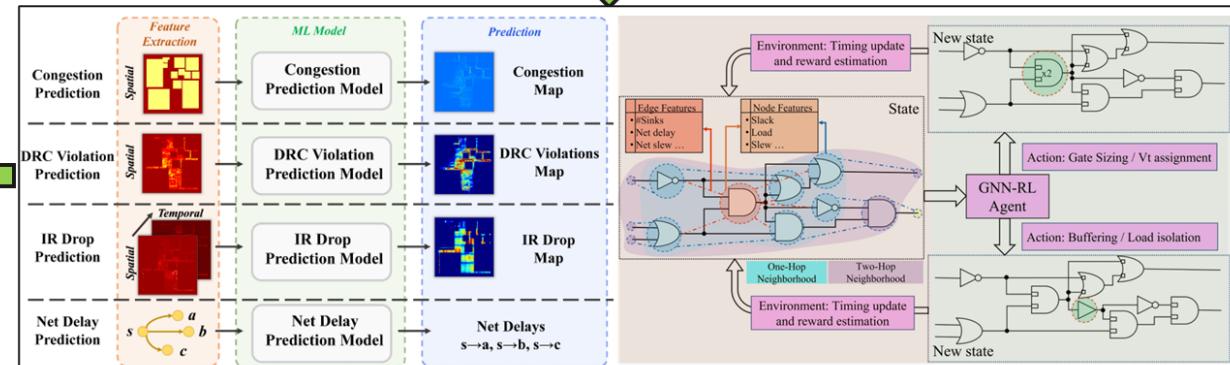


## CircuitOps: ML-friendly data representation format within OpenROAD

pandas.DataFrame features



Easy application of ML training within  
OpenROAD interpreter



## ML/RL algorithms integrated within OpenROAD

CircuitOps and OpenROAD: Unleashing  
ML EDA for Research and Education

ASP-DAC 2024  
next Monday!

Andrew B. Kahng, UCSD  
Vidya A. Chhabria, ASU  
Bing-Yue Wu, ASU

EDA-schema:  
Graph Datamodel Schema and Dataset for Design Automation

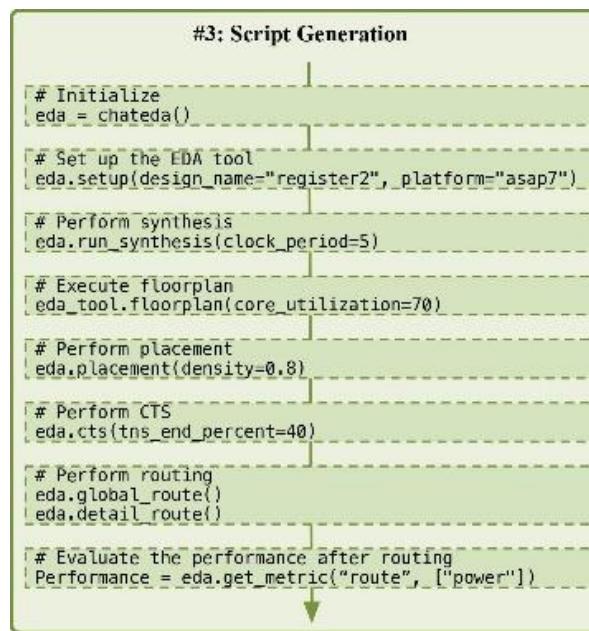
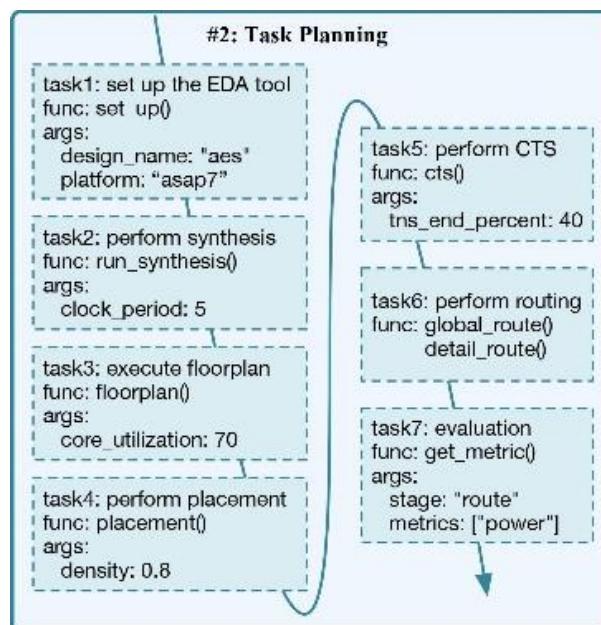
Prof. Ioannis Savidis, Drexel U. [is338@drexel.edu](mailto:is338@drexel.edu)

# ChatEDA: Autonomous EDA Agent Empowered by LLM

**Conversational interface for human-toolflow interaction**  
→ improved productivity

## #1. User Requirement

For the design named “aes” on the platform “asap7”, please perform synthesis with a clock period of 5, followed by floorplan with a core utilization of 70%. Then, execute placement with a density of 0.8. Next, proceed with CTS to fix 40% of violating paths. Finally, evaluate the performance after routing using “power” metric.



## Workflow

1. (user) natural language input
2. (ChatEDA) task planning
3. (ChatEDA) script generation
4. (OpenROAD) task execution

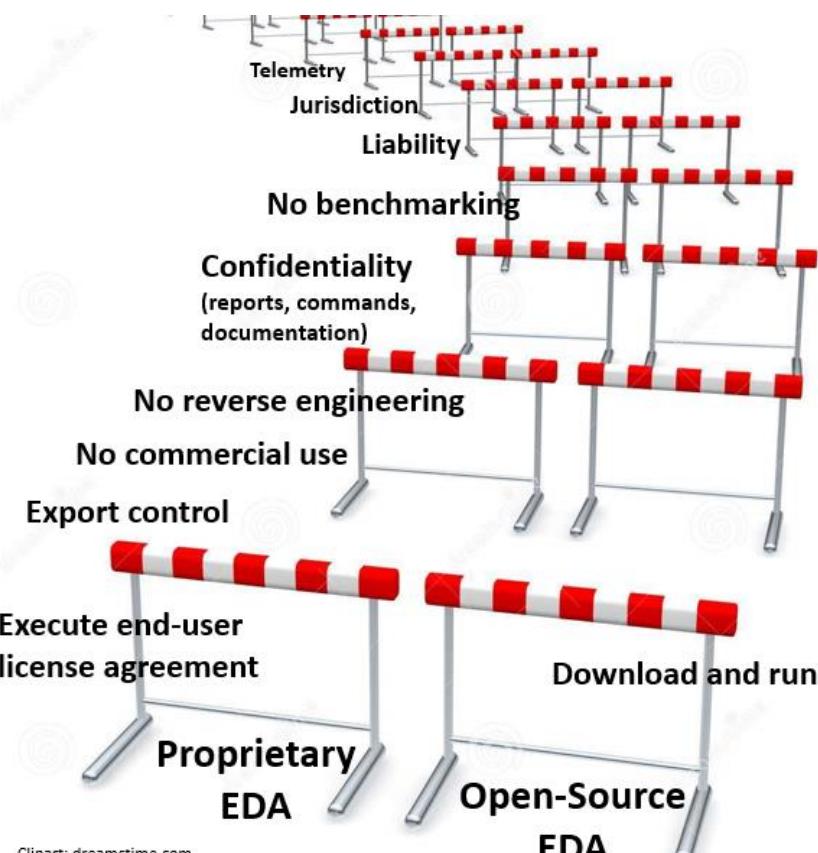
# Agenda

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- What is OpenROAD ?
- How did we get here ? (The Journey)
- Where are we going ? (The Roadmap)
  - The Future: Better, Faster Optimization + Machine Learning !
  - OpenROAD Tool Development
  - ML Enablement with OpenROAD
- Concluding thoughts

# Food for Thought: On Bars and Barriers

- Is it good enough for training?
- Does it accelerate research?
- Can students access and use it?
  - Commercial EDA EULAs
    - No benchmarking
    - No reverse-engineering
    - Copyrighted command language
    - Copyrighted report formats
  - Every student signs an NDA (!)
  - Export control
- Platforms such as CircuitOps and OpenROAD are open
  - → avoid Bars and Barriers

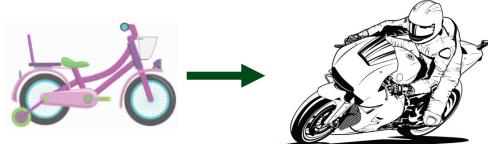


ICCAD22 [talk](#) on “A Mixed Open-Source and Proprietary EDA Commons for ...”

# About “Chips Acts”

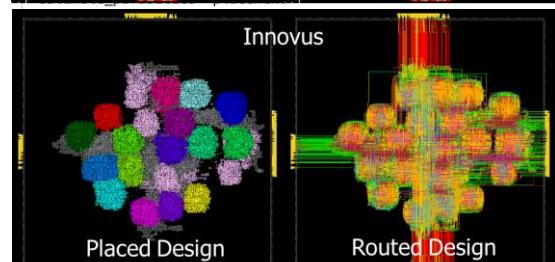
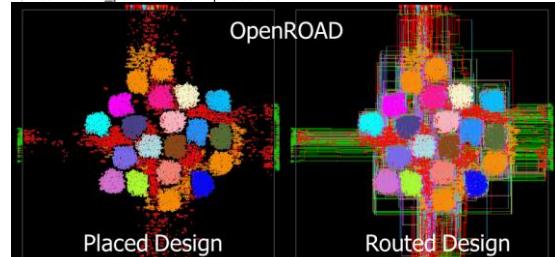
## Training the Future Workforce

Better onramps

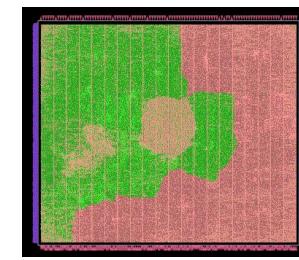
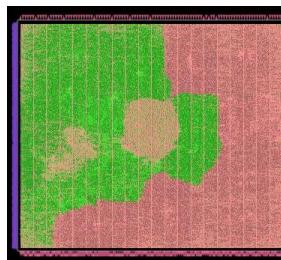


No friction *(Ex.: "skin" creation)*

```
proc place_opt_design {args} {
    remove_buffer
    set place_density [expr $place_density_lb + ($place_density_hb - $place_density_lb) * 0.5]
    set target_density [expr $place_density_lb + (1 - $place_density_lb) * 0.5]
    global_placement -density $target_density
    estimate_parasitics -placement
```



## Accelerate Innovation



OpenROAD

cādence®

SYNOPSYS®

Ansys

Qualcomm

IBM

SIEMENS

Technology Leadership

SAMSUNG

tsmc



AMD

NVIDIA

Logos and images are property of respective owners. The “skin” script was written and developed by students at UCSD; however, the underlying commands and reports are copyrighted by Cadence. We thank Cadence for granting permission to share our research to help promote and foster the next generation of innovators.

# Some Links

(talks are always posted at [vlscicad.ucsd.edu](http://vlscicad.ucsd.edu))

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- Panel position statement at IEEE-USA's [Designing Chips with CHIPS: West Coast Pre-Silicon Summit](#), November 3, 2023. [.pptx](#)
- "Leveling Up: A Trajectory of OpenROAD, TILOS and Beyond", *Proc. ISPD*, March 2022. [.pdf](#) [.pptx](#)
- "Our Real Scaling Challenge: People", ACCESS-CEDA seminar, Sept. 2022. [.pptx](#)
- "Bars and Barriers to Overcome for Shared ML EDA Infrastructure", NSF Workshop on Shared Infrastructure for Machine Learning EDA, March 2023. [.pptx](#)
- Thoughts on open source in EDA
  - 2002: "Toward CAD-IP Reuse: The MARCO GSRC Bookshelf of Fundamental CAD Algorithms" [\[.pdf\]](#) (+ [\[.pdf\]](#))
  - 2019: "Looking Into the Mirror of Open Source" [\[.pdf\]](#)
  - 2020: "Open-Source EDA: If We Build It, Who Will Come?" [\[.pdf\]](#)
  - 2021: "The OpenROAD Project: Unleashing Hardware Innovation" [\[.pdf\]](#)
  - 2022: "The OpenROAD Project: A Foundation for Research and Education in EDA and IC Design" [\[.pptx\]](#)
  - 2022: "A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping", [\[.pdf\]](#) [\[.pptx\]](#)
  - 2023: Talk on OpenROAD at the 3<sup>rd</sup> Open-Source Design Automation Workshop (OSDA-2023) [\[.pptx\]](#)
  - 2023: "OpenROAD: A Platform for Innovation and Workforce Development" (U.S.-Japan Collaborative Workshop: Accelerating IC Design) [\[.pptx\]](#)
- <https://theopenroadproject.org> + <https://github.com/The-OpenROAD-Project>

# Summary

- OpenROAD is now in its 6<sup>th</sup> year
  - “Going viral” in many dimensions: community, education, workforce development, commercial use
- U.S. DARPA contract has ended
  - Precision Innovations, Inc is the core R&D organization taking the project forward
  - OpenROAD Initiative 501(c)(3) foundation for philanthropic support
- OpenROAD can support and collaborate with this community!
  - Platform for Innovation (EDA algorithms, tools, flows; AI/ML, IC design)
  - Onramp for Workforce Development

**Workshop Outline**

- Introduction to VLSI Backend Flow
- Stages and Sign-off Checks Overview
- OpenROAD Design Flow
- Detailed VLSI Backend Flow
  - RTL Synthesis
  - Floorplanning
  - Placement
  - Static Timing Analysis
  - Clock Tree Synthesis
  - Routing
  - GUI
  - OpenROAD for PPA
- Hands-on
  - Installation of the OpenROAD Tool.
  - Input files
  - RTL synthesis
  - Floorplan and Placement
  - Post-placement Timing Analysis
  - Clock Tree Synthesis (CTS)
  - Post-CTS Timing Analysis
  - Routing and DRC/LVS Check.

**Contact:**  
For queries related to accommodation:  
Mr. Ravi Dubey  
Contact No.: 9893112942/8651976428  
For queries related to registration:  
Email: [prajit@iitg.ac.in](mailto:prajit@iitg.ac.in)  
Landline No.: 0361-256-3182  
Time to contact : 9.00 AM to 6.00 PM

**Objective**  
The objective of this workshop is to train the participants with VLSI design backend flow through the open-source VLSI design tool “OpenROAD”. After successful completion of this workshop, the participants would be able to run the RTL synthesis to GDS-2 flow for their own design.

**IIT Guwahati**  
in association with  
Ministry of Electronics and Information  
Technology

**Workshop on**  
**“OpenROAD for Low-cost ASIC design for Rapid Innovation”**

**Organized by**  
**“NINE Labs, IIT Guwahati”**

**17 Jan – 24 Jan 2024**  
Conference Hall 3,  
Indian Institute of Technology Guwahati - 781039, Assam, India

**Website:**  
<https://www.iitg.ac.in/proj/ninelabs/WORKSHOP/index.html>



Let's continue the journey !!!

# THANK YOU !

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