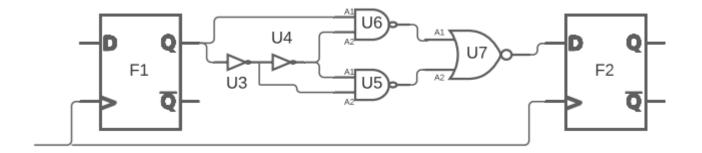


Day5



- Consider the following picture
- How many paths do you see F1:CK \rightarrow F2:D?
 - $F1:CK \rightarrow U3 \rightarrow U4 \rightarrow U6:A2 \rightarrow U7:A1 \rightarrow F2:D$
 - $F1:CK \rightarrow U6 \rightarrow U4 \rightarrow U5:A1 \rightarrow U7:A2 \rightarrow F2:D$
 - $F1:CK \rightarrow U6:A1 \rightarrow U7:A1 \rightarrow F2:D$
 - $F1:CK \rightarrow U6 \rightarrow U5:A2 \rightarrow U7:A2 \rightarrow F2:D$
- Type 'leafpad out.txt' the slack reported for the path is -217.323
- Which of the 4 paths above it corresponds to





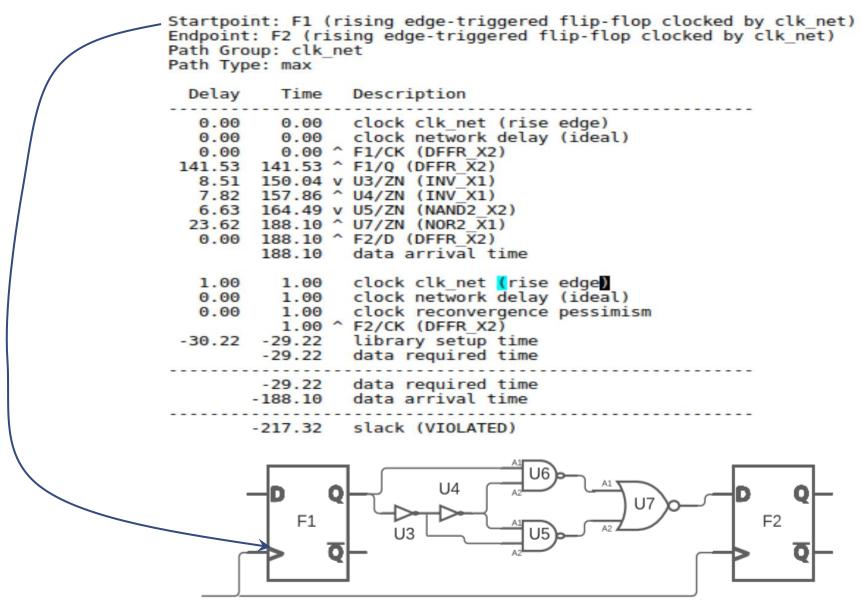


Running the lab

- Type "cd lab3"
- Run 'sta run.tcl -noexit | tee out.txt'





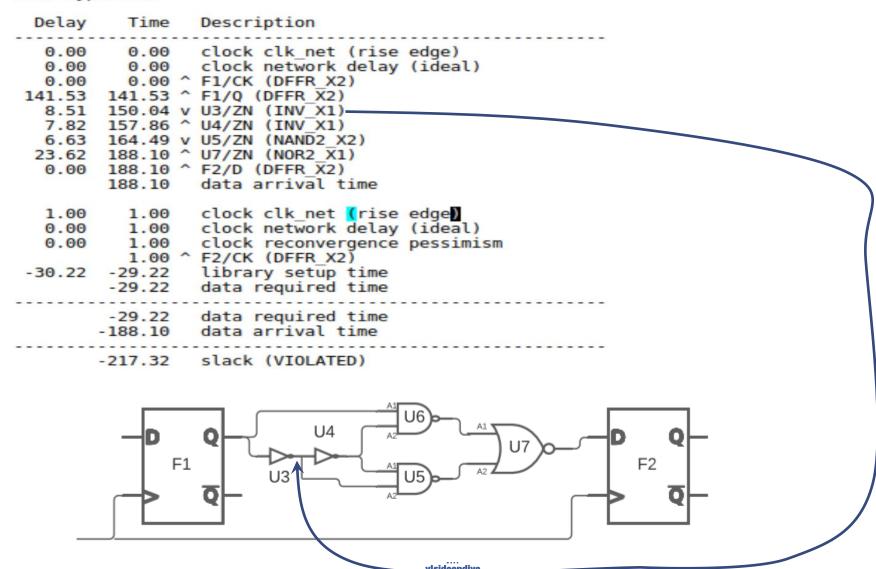




Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk net)

Path Group: clk_net

Path Type: max





Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)

Path Group: clk net Path Type: max

rath Type. max				
Delay Time Description				
0.00				
7.82 157.86 ^ U4/ZN (INV_X1) 6.63 164.49 v U5/ZN (NAND2_X2) 23.62 188.10 ^ U7/ZN (NOR2_X1) 0.00 188.10 ^ F2/D (DFFR_X2) 188.10 data arrival time				
1.00 1.00 clock clk_net (rise edge) 0.00 1.00 clock network delay (ideal) 0.00 1.00 clock reconvergence pessimism 1.00 ^ F2/CK (DFFR_X2) -30.22 -29.22 library setup time -29.22 data required time				
-29.22 data required time -188.10 data arrival time				
-217.32 slack (VIOLATED)				
P Q U3 U4 A2 U7 P Q F2 Q				
vlsideepdive				



Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net) Path Group: clk net

Path Type: max

racii Type.	IIIGA				
Delay	Time	Description			
0.00 0.00 141.53 14 8.51 15 7.82 15 6.63 16 23.62 18 0.00 18	1.53 ^ 0.04 v 7.86 ^ 4.49 v 8.10 ^				
0.00 0.00 -30.22 -2	1.00 1.00 1.00 1.00 ^ 9.22 9.22	clock clk_net (rise edge) clock network delay (ideal) clock reconvergence pessimism F2/CK (DFFR_X2) library setup time data required time	\		
	9.22 8.10	data required time data arrival time			
-21	7.32	slack (VIOLATED)	/		
P Q U4 A1 U7 P Q F2 Q VIsideepilve					



Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net) Path Group: clk net

Path Type: max

Path Type	: max	
Delay	Time	Description
8.51 7.82 6.63 23.62 0.00	0.00 0.00 ^ 141.53 ^ 150.04 v 157.86 ^ 164.49 v 188.10 ^	clock clk_net (rise edge) clock network delay (ideal) F1/CK (DFFR_X2) F1/Q (DFFR_X2) U3/ZN (INV_X1) U4/ZN (INV_X1) U5/ZN (NAND2_X2) U7/ZN (NOR2_X1) F2/D (DFFR_X2) data arrival time
	1.00 1.00 1.00 1.00 ^ -29.22 -29.22	clock clk_net {rise edge} clock network delay (ideal) clock reconvergence pessimism F2/CK (DFFR_X2) library setup time data required time
	-29.22 188.10	data required time data arrival time
-	217.32	slack (VIOLATED)
	Q F1 Q	U4 A2 U7 P F2 P
		vlsideepdive



```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
```

Path Type: max				
Delay	Time	Description		
0.00 0.00 0.00 141.53 8.51 7.82 6.63 23.62 0.00	141.53 ^ 150.04 v 157.86 ^ 164.49 v 188.10 ^			
0.00	1.00	clock clk_net (rise edge) clock network delay (ideal)		
0.00	1.00	clock reconvergence pessimism F2/CK (DFFR X2)		
-30.22	-29.22 -29.22	library setup time data required time		
	-29.22 -188.10	data required time data arrival time		
	-217.32	slack (VIOLATED)		
D	Q - {	U4 A2 U7 P F2 P		
		vlsideepdive		



visideepdive Exercises

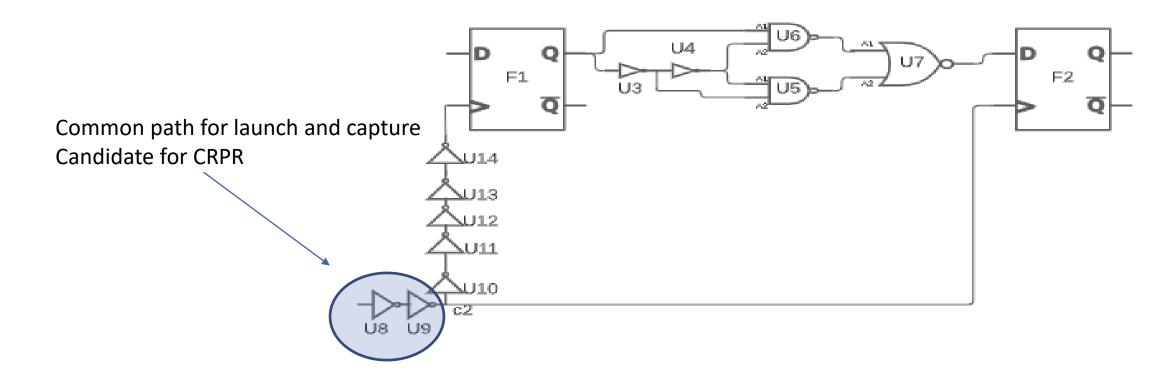
- Change the number of paths being reported to 100
 - report_checks –from F1/CK -endpoint_count 100
 - Analyze each path in detail and understand





Common Path Pessimism Removal(CPPR)

- Type 'cd lab4'
- Run 'sta run.tcl –exit | out.txt'







Common Path Pessimism Removal(CPPR)

Now, get the timing of circuit

```
% report_checks -to F2/D
```

Worst Path: through U5/A1

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk net)
Path Group: clk net
Path Type: max
  Delay
           Time
                 Description
           0.00
                 clock clk net (rise edge)
   0.00
   0.00
           0.00
                 clock source latency
  0.00
          0.00 ^ clk net (in)
  34.84 34.84 ^ U8/Z (CLKBUF X2)
  35.15
       69.99 ^ U9/Z (CLKBUF_X2)
  34.85 104.84 ^ U10/Z (CLKBUF_X2)
  34.84 139.68 ^ U11/Z (CLKBUF_X2)
  34.84 174.53 ^ U12/Z (CLKBUF X2)
  34.84 209.37 ^ U13/Z (CLKBUF X2)
  34.71 244.08 ^ U14/Z (CLKBUF X2)
   0.00 244.08 ^ F1/CK (DFFR X2)
 141.54 385.62 ^ F1/Q (DFFR_X2)
   8.51 394.12 v U3/ZN (INV_X1)
   7.82 401.94 ^ U4/ZN (INV_X1)
   6.63 408.57 v U5/ZN (NAND2 X2)
  23.62 432.19 ^ U7/ZN (NOR2 X1)
   0.00 432.19 ^ F2/D (DFFR X2)
         432.19
                 data arrival time
                  clock clk_net (rise edge)
   1.00
           1.00
   0.00
          1.00
                  clock source latency
        1.00 ^ clk net (in)
   0.00
  31.53 32.53 ^ U8/Z (CLKBUF X2)
  31.80 64.32 ^ U9/Z (CLKBUF X2)
  0.00 64.32 ^ F2/CK (DFFR X2)
 -30.23
                 library setup time
          34.09
                 data required time
          34.09
                  data required time
          34.09
                  data arrival time
        -432.19
```





Common Path Pessimism Removal(CPPR)

- 'c2' is node which requires CPPR
- Now change (following from 0 to 1)
 - set sta_crpr_enabled 1
- Now, get the timing of circuit

% report_checks -to F2/D

Worst Path: through U5:A1

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk net)
Path Group: clk net
Path Type: max
  Delay
                  Description
   0.00
           0.00
                  clock clk net (rise edge)
   0.00
           0.00
                  clock source latency
           0.00 ^ clk net (in)
          34.84 ^ U8/Z (CLKBUF X2)
          69.99 ^ U9/Z (CLKBUF X2)
         104.84 ^ U10/Z (CLKBUF_X2)
         139.68 ^ U11/Z (CLKBUF X2)
         174.53 ^ U12/Z (CLKBUF_X2)
         209.37 ^ U13/Z (CLKBUF X2)
         244.08 ^ U14/Z (CLKBUF X2)
         385.62 ^ F1/Q (DFFR X2)
         394.12 v U3/ZN (INV X1)
         408.57 v U5/ZN (NAND2 X2)
         432.19 ^ U7/ZN (NOR2_X1)
        432.19 ^ F2/D (DFFR X2)
         432.19
   1.00
           1.00
                  clock clk_net (rise edge)
                  clock source latency
           1.00 ^ clk net (in)
                ^ U8/Z (CLKBUF X2)
                ^ U9/Z (CLKBUF X2)
                ^ F2/CK (DFFR X2)
 6.67
                  clock reconvergence pessimism
          40.76
                  library setup time
          40.76
```

slack (VIOLATED)



-432.19



ECO – Engineering Change Order

- In the ECO cycle, we perform various analysis one by one for every check which we need to close but not closed till PnR stage.
- There are specialized signoff tools that help us to analyze the issue and also suggest the changes we need to do in order to close the issue.
- The suggested change is captured in an eco file.
- In this lab we will focus on ECO for timing purposes, this is done to fix setup and hold violations





ECO insertion

- Type 'cd lab5'
- Open 'run.tcl'
- Notice the commands being used in run.tcl

```
### Inserting Timing ECOs
make_instance U16 CLKBUF_X3
make_net c6
disconnect_pin c5 U15/Z
connect_pin c6 U15/Z
connect_pin c6 U16/A
connect_pin c5 U16/Z
```

- Check for description of commands in openSTA pdf doc.
- Run sta run.tcl –exit | tee run.log
- Open Verilog file s27_eco.v, what differences you find compared to s27.v
 - Document the differences
- Observe the change in slack values at timing report

