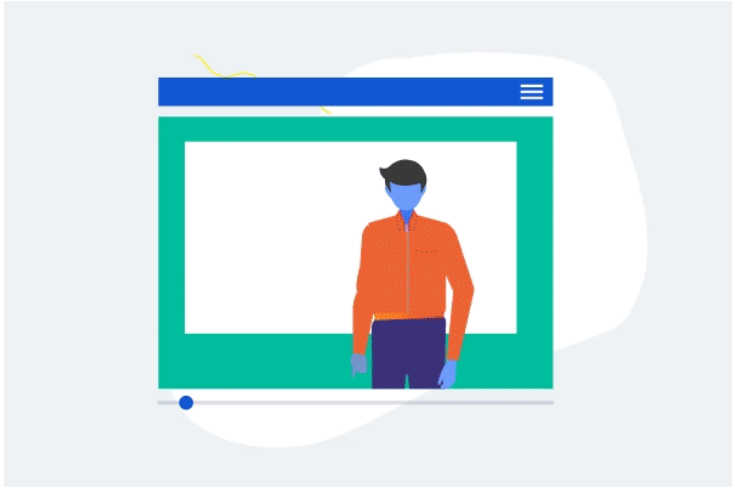

Day2

Liberty File

- The .lib file is an ASCII representation of the timing and power parameters associated with any cell in a particular semiconductor technology
- The .lib file contains timing models and data to calcumax
  - I/O delay paths
  - Timing check values
  - Interconnect delays
- Liberty File Reference
  - https://people.eecs.berkeley.edu/~alanmi/publications/other/liberty07_03.pdf

Understanding Liberty File

```
library (name_of_library)
technology ( cmos ) ;

delay_model      : table_lookup;
date : "date_of_creation)" ;
revision : revision_number ;
time_unit : "1ns" ;
leakage_power_unit : "1pW" ;
voltage_unit : "1V" ;
pulling_resistance_unit : "1kohm" ;
current_unit : "1uA" ;
capacitive_load_unit(1.000,ff) ;

nom_voltage      : 1.200000;
nom_temperature : 125.0;
nom_process : 1.000;
```

Name of Library

Name of Technology

Units

```
operating_conditions("TYPICAL") {
    process :   1.0;
    temperature :   125;
    voltage :   1.2;
```

PVT – Process, Voltage and Temperature

Liberty File Cell Part

```
cell(AND2X1) {
  /* gs005 */
  pg_pin(VDD) {
    voltage_name : V;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
    scaling_factors : AND2X1_factors ;
    area : 7.445 ;
    leakage_power() {
   /* gs006 */
   related_pg_pin : VDD;
        when : "(IN1'*IN2')";
        value : 162490.000;
    }
    leakage_power() {
   /* gs006 */
   related_pg_pin : VDD;
        when : "(IN1*IN2')";
        value : 171100.000;
    }
    leakage_power() {
   /* gs006 */
   related_pg_pin : VDD;
        when : "(IN1'*IN2)";
        value : 178960.000;
    }
    leakage_power() {
   /* gs006 */
   related_pg_pin : VDD;
        when : "(IN1*IN2)";
        value : 149790.000;
    }
```

Cell Name in the Library

Power Pin Name

Leakage power under this condition

Leakage power under this condition

Liberty File Pin Part

```
pin(IN2) {
    direction : input;
    internal_power() {
    power(power_inputs_0) {
    values( " 4.87 3.35 2.86 3.50 2.03 1.56 1.83");
    }
    }
    capacitance : 1.460;
    fanout_load : 0.073;
    rise_capacitance : 1.529;
    fall_capacitance : 1.392;
}
```

Pin Name inside the Cell

Direction of the pin

Capacitance of the pin

Understanding LIB parsing

- Command for reading liberty file

  Cmnd: `read_liberty`

Argument	Type	Description
`-min`	Optional	Use library for min delay
`-max`	Optional	Use library for max delay
`filename`	Required	The name of the liberty file to read

  By default, filename for both options if none are given.

- Type ‘cd lab2’
- Type ‘ls’, you will see 2 lib files with the following names
  - simple_min.lib open using ‘leafpad simple_min.lib’
  - simple_max.lib, open using ‘leafpad simple_max.lib’

vlsideepdive

Exercises

- Find all the cells in simple_max.lib.
- Find all the pins of the cell NAND2_X1 in simple_max.lib
- What difference you see between NAND2_X1 and NAND3_X1
- What is the difference between ‘simple_max.lib’ and ‘simple_min.lib’

SPEF File

- A SPEF (Standard Parasitic Exchange Format) file describes parasitic information of the design.
- Users would never create this file manually.
- It is automatically generated by the tool.
- It is mainly used to pass parasitic information from one tool to another.

General Syntax

- A Typical SPEF File has 4 main sections
  - Header
  - Name Map
  - Top Level Ports
  - Parasitic description
- More information about SPEF format can be found here
  - https://www.vlsisystemdesign.com/spef-format-part-1/

Lab2: Understanding SPEF parsing

- Command for spef parsing

  Cmnd: `read_spef`

```
15
16 *D_NET inp1 5.4
17 *CONN
18 *P inp1 I
19 *I u1:a I
20 *CAP
21 1 inp1 1.2
22 2 inp1:1 1.3
23 3 inp1:2 1.4
24 4 u1:a 1.5
25 *RES
26 1 inp1 inp1:1 3.4
27 2 inp1:1 inp1:2 3.5
```

Report Timing

- report_checks command is used to report timing on the design
- Add following command in run.tcl
  - report_timing –num_paths 5
  - Rerun ‘`sta run.tcl -exit | tee run.log`’
- `Open ‘leafpad run.log’`

Understanding Timing Reports

```
Startpoint: inp1 (input port clocked by tau2015_clk)
Endpoint: f1 (rising edge-triggered flip-flop clocked by tau2015_clk)
Path Group: tau2015_clk
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock tau2015_clk (rise edge)
   0.00    0.00   clock network delay (ideal)
   5.00    5.00 ^ input external delay
   0.00    5.00 ^ inp1 (in)
 113.95  118.95 v u1/o (NAND2_X1)
 119.78  238.73 ^ u4/o (NOR2_X1)
   8.32  247.05 ^ f1/d (DFF_X80)
         247.05   data arrival time

  50.00   50.00   clock tau2015_clk (rise edge)
   0.00   50.00   clock network delay (ideal)
   0.00   50.00   clock reconvergence pessimism
          50.00 ^ f1/ck (DFF_X80)
  -1.50   48.50   library setup time
          48.50   data required time
---------------------------------------------------------
          48.50   data required time
        -247.05   data arrival time
---------------------------------------------------------
        -198.55   slack (VIOLATED)
```

Means setup analysis

Input delay value

Delays from liberty files

Value from liberty

Exercises

- Understand other paths in run.log
- Understand where each of the values coming from
- Increase number of paths reported and analyze those