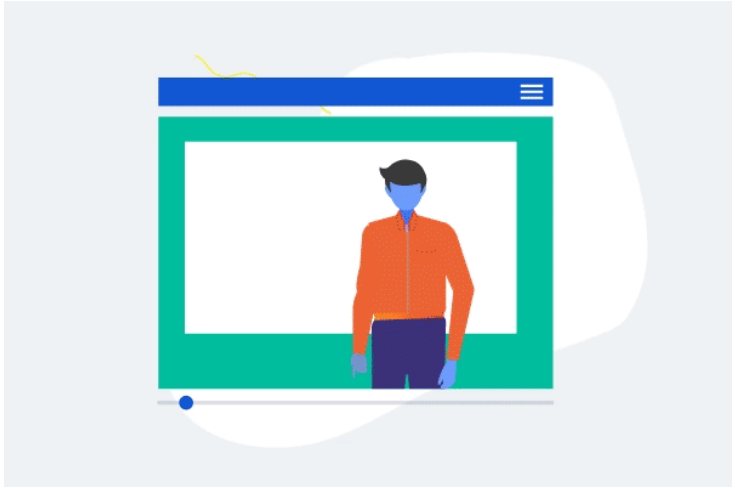
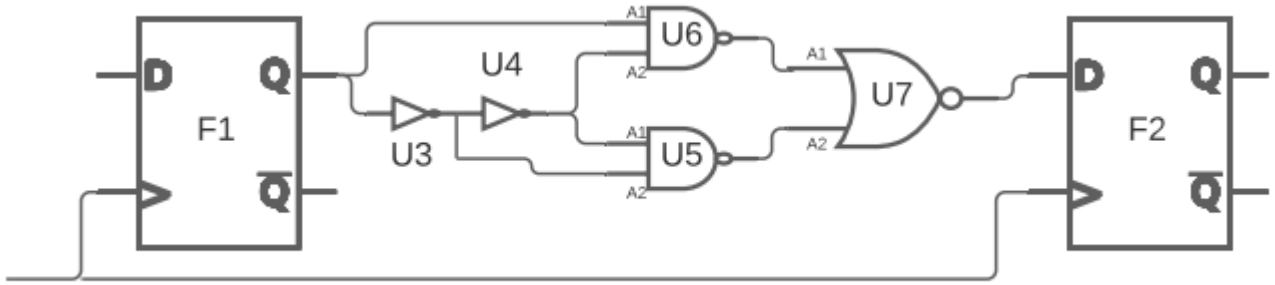


# Day5

# Understanding Slack Computation

- Consider the following picture
- How many paths do you see F1:CK →F2:D?
    1. F1:CK→U3→U4→U6:A2→U7:A1→F2:D
    2. F1:CK→U6→U4→U5:A1→U7:A2→F2:D
    3. F1:CK→U6:A1→U7:A1→F2:D
    4. F1:CK→U6→U5:A2→U7:A2→F2:D
- Type ‘leafpad out.txt’ the slack reported for the path is -217.323
- Which of the 4 paths above it corresponds to

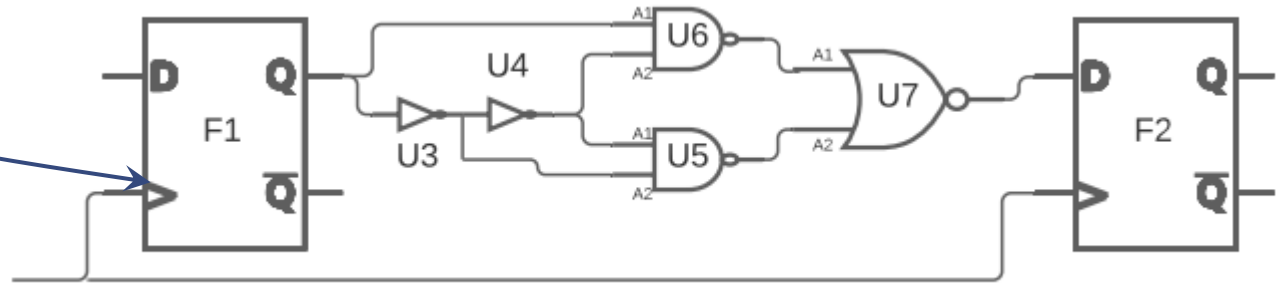


# Running the lab

- Type “cd lab3”
- Run ‘sta  run.tcl -noexit | tee out.txt’

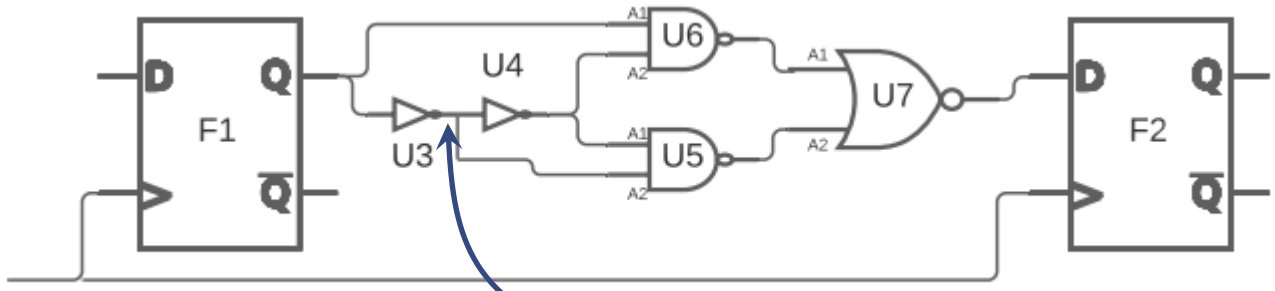
# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```



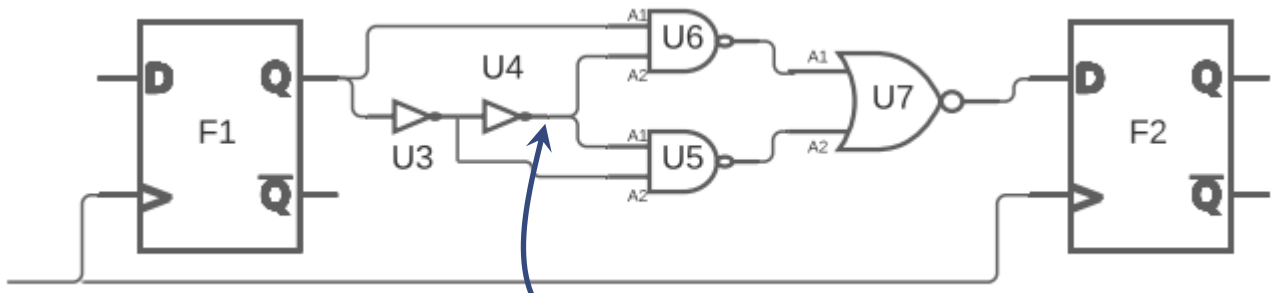
# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```



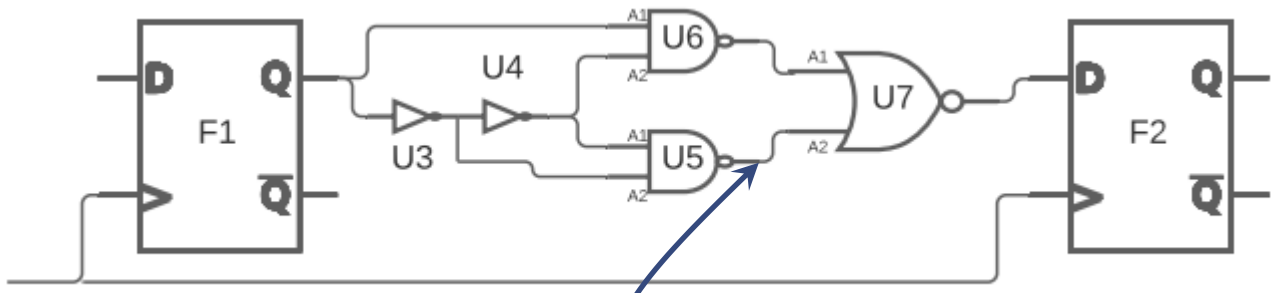
# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```



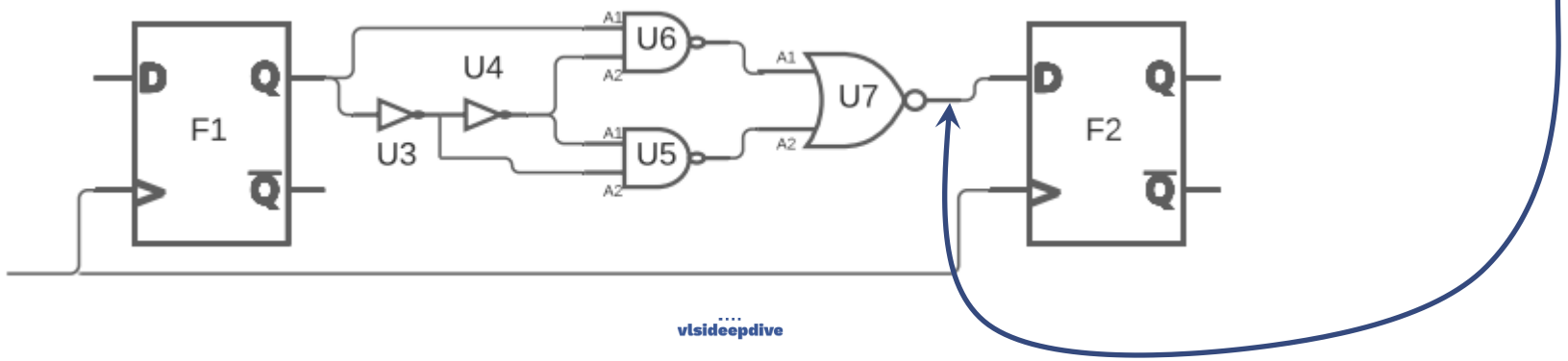
# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```



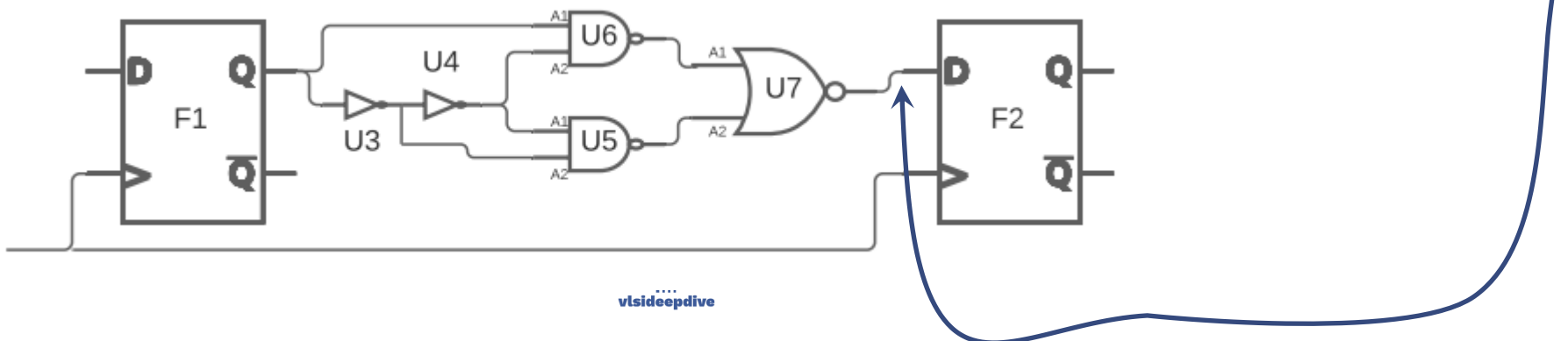
# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```



# Understanding Slack Computation

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```

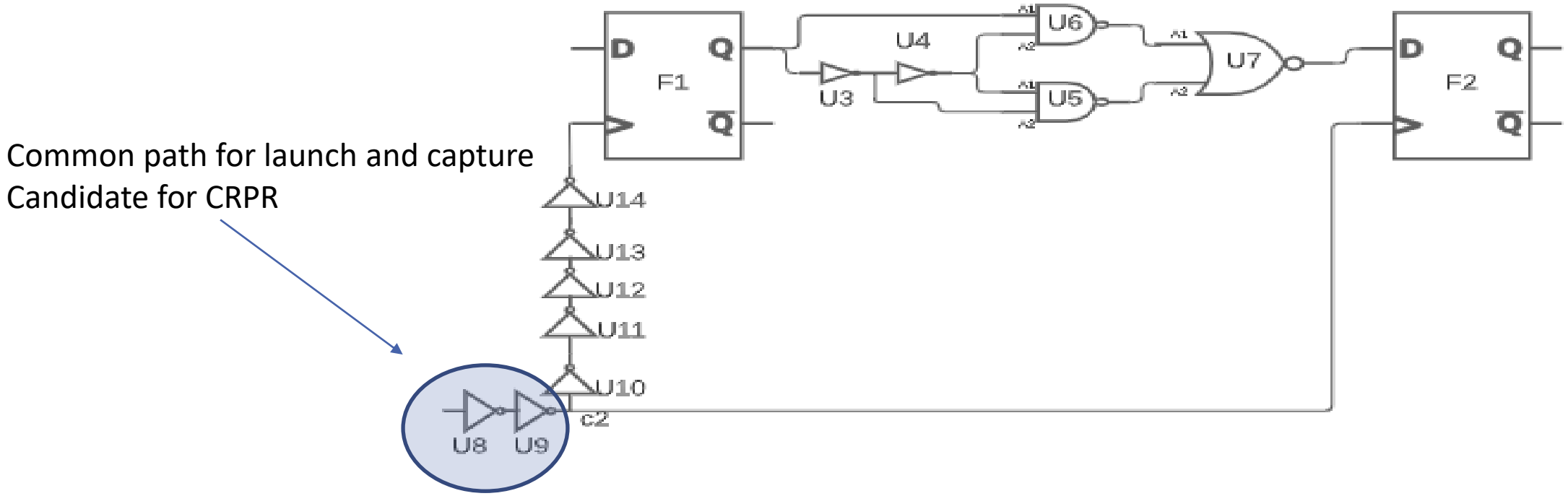


# Exercises

- Change the number of paths being reported to 100
  - report_checks –from F1/CK -endpoint_count 100
  - Analyze each path in detail and understand

# Common Path Pessimism Removal(CPPR)

- Type ‘cd lab4’
- Run ‘sta run.tcl –exit | out.txt’



# Common Path Pessimism Removal(CPPR)

- Now, get the timing of circuit

  % `report_checks -to F2/D`

  Worst Path: through U5/A1

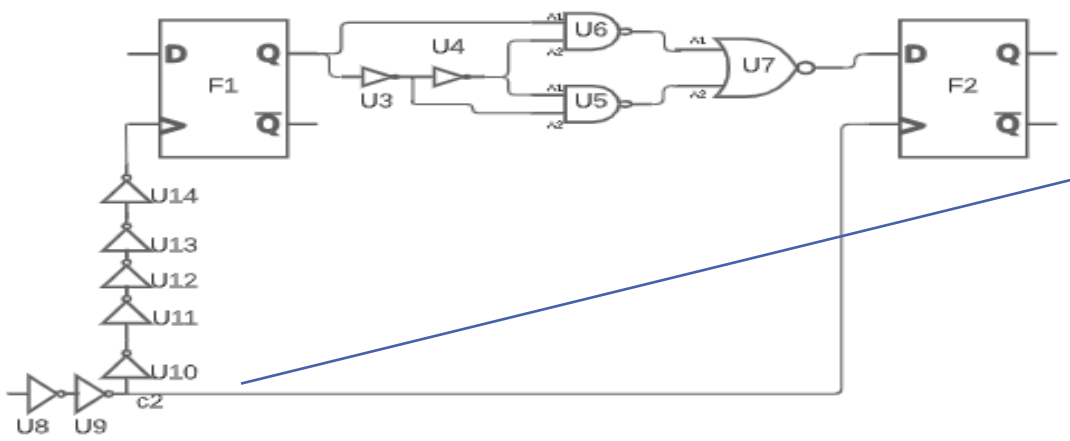
```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock source latency
   0.00    0.00 ^ clk_net (in)
  34.84   34.84 ^ U8/Z (CLKBUF_X2)
  35.15   69.99 ^ U9/Z (CLKBUF_X2)
  34.85  104.84 ^ U10/Z (CLKBUF_X2)
  34.84  139.68 ^ U11/Z (CLKBUF_X2)
  34.84  174.53 ^ U12/Z (CLKBUF_X2)
  34.84  209.37 ^ U13/Z (CLKBUF_X2)
  34.71  244.08 ^ U14/Z (CLKBUF_X2)
   0.00  244.08 ^ F1/CK (DFFR_X2)
 141.54  385.62 ^ F1/Q (DFFR_X2)
   8.51  394.12 v U3/ZN (INV_X1)
   7.82  401.94 ^ U4/ZN (INV_X1)
   6.63  408.57 v U5/ZN (NAND2_X2)
  23.62  432.19 ^ U7/ZN (NOR2_X1)
   0.00  432.19 ^ F2/D (DFFR_X2)
         432.19   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock source latency
   0.00    1.00 ^ clk_net (in)
  31.53   32.53 ^ U8/Z (CLKBUF_X2)
  31.80   64.32 ^ U9/Z (CLKBUF_X2)
   0.00   64.32 ^ F2/CK (DFFR_X2)
 -30.23   34.09   library setup time
          34.09   data required time
---------------------------------------------------------
          34.09   data required time
        -432.19   data arrival time
---------------------------------------------------------
```

# Common Path Pessimism Removal(CPPR)

- ‘c2’ is node which requires CPPR
- Now change (following from 0 to 1)
  - set sta_crpr_enabled 1
- Now, get the timing of circuit

  % `report_checks -to F2/D`

  Worst Path: through U5:A1




```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock source latency
   0.00    0.00 ^ clk_net (in)
  34.84   34.84 ^ U8/Z (CLKBUF_X2)
  35.15   69.99 ^ U9/Z (CLKBUF_X2)
  34.85  104.84 ^ U10/Z (CLKBUF_X2)
  34.84  139.68 ^ U11/Z (CLKBUF_X2)
  34.84  174.53 ^ U12/Z (CLKBUF_X2)
  34.84  209.37 ^ U13/Z (CLKBUF_X2)
  34.71  244.08 ^ U14/Z (CLKBUF_X2)
   0.00  244.08 ^ F1/CK (DFFR_X2)
 141.54  385.62 ^ F1/Q (DFFR_X2)
   8.51  394.12 v U3/ZN (INV_X1)
   7.82  401.94 ^ U4/ZN (INV_X1)
   6.63  408.57 v U5/ZN (NAND2_X2)
  23.62  432.19 ^ U7/ZN (NOR2_X1)
   0.00  432.19 ^ F2/D (DFFR_X2)
         432.19   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock source latency
   0.00    1.00 ^ clk_net (in)
  31.53   32.53 ^ U8/Z (CLKBUF_X2)
  31.80   64.32 ^ U9/Z (CLKBUF_X2)
   0.00   64.32 ^ F2/CK (DFFR_X2)
   6.67   70.99   clock reconvergence pessimism
 -30.23   40.76   library setup time
          40.76   data required time
---------------------------------------------------------
          40.76   data required time
        -432.19   data arrival time
---------------------------------------------------------
        -391.43   slack (VIOLATED)
```

# ECO – Engineering Change Order

- In the ECO cycle, we perform various analysis one by one for every check which we need to close but not closed till PnR stage.
- There are specialized signoff tools that help us to analyze the issue and also suggest the changes we need to do in order to close the issue.
- The suggested change is captured in an eco file.
- In this lab we will focus on ECO for timing purposes, this is done to fix setup and hold violations

# ECO insertion

- Type ‘cd lab5’
- Open ‘run.tcl’
- Notice the commands being used in run.tcl

```
### Inserting Timing ECOs
make_instance U16 CLKBUF_X3
make_net c6
disconnect_pin c5 U15/Z
connect_pin c6 U15/Z
connect_pin c6 U16/A
connect_pin c5 U16/Z
```

- Check for description of commands in openSTA pdf doc.
- Run sta run.tcl –exit | tee run.log
- Open Verilog file s27_eco.v, what differences you find compared to s27.v
  - Document the differences
- Observe the change in slack values at timing report