GOVERNMENT COLLEGE OF ENGINEERING, SALEM -11.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VGA CONTROLLER USING FPGA

CONTENT :

- ❑ INTRODUCTION
- ❑PROBLEM STATEMENT
- ❑ABSTRACT
- ❑OBJECTIVE
- ❑LITERATURE SURVEY
- ❑CONCLUSION

INTRODUCTION :

- In order to implement VGA controller using Field Programable Gate Array(FPGA) in VLSI.
- In this project , an efficient FPGA based video graphic array algorithm will be presented using Verilog hardware description language.
- VGA- It's a standard for connecting displays to computers, using a 15-pin connector and supporting resolutions up to 640x480 pixels.

PROBLEM STATEMENT:

- The objective is to design and implement a VGA controller using an FPGA to interface a digital system with a VGA display.
- The controller must generate precise horizontal and vertical synchronization signals and manage pixel data to ensure a stable and clear display
- It involves overcoming issues related to high memory bandwidth and power consumption while maintaining display quality and performance.

ABSTRACT:

In this project we design the controller which handles synchronization signals, pixel clock generation, and RGB data output. By leveraging the FPGA's programmable logic, the design can achieve precise timing control and flexibility in resolution settings. This VGA controller serves as a foundational component for graphics applications and educational purposes in digital design.

OBJECTIVE:

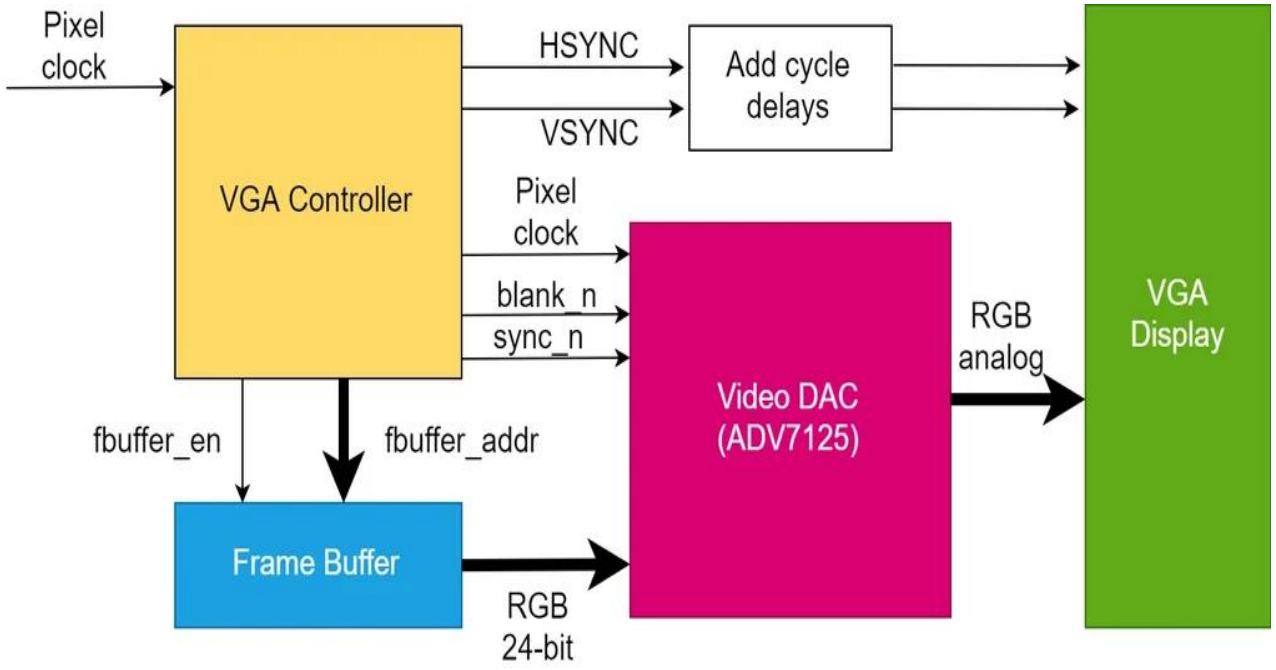
- The aim and objective is to develop an FPGA-based VGA controller to generate the necessary synchronization signals (horizontal and vertical sync) for proper display timing.
- Implementing a mechanism to fetch and transmit pixel data to the VGA display in accordance with the generated sync signals.
- Ensuring the controller which supports various screen resolutions and color depths, providing flexibility for different display requirements.

LITERATURE SURVEY:

S.NO	NAME OF THE PAPER / BOOK	NAME OF THE AUTHOR	IMPROVEMENT OVER PREVIOUS WORK	YEAR
1	Design and Implementation of FPGA-Based VGA Controller. IEEE International Symposium on VLSI Design, Automation and Test.	Pham, T. T., & Tran, N. T.	Establishes the core functionalities of a VGA controller on FPGA.	2019
2	Low-Power FPGA-Based VGA Controller Design. IEEE Transactions on VLSI Systems.	Kumar, S. R., & Verma, V. K.	Introduces techniques for reducing power consumption in the controller.	2021
3	Optimization Techniques for VGA Controller Implementation on FPGA. Journal of VLSI Design.	Lee, A. J., & Park, R. S.	Optimizes resource usage, performance, or combines design and low-power aspects.	2023

BUILDING BLOCKS OF A VGA CONTROLLER:

A typical VGA controller using FPGA consists of several key components:



CLOCK GENERATOR: Generates the necessary timing signals for horizontal and vertical scanning of the image on the monitor.

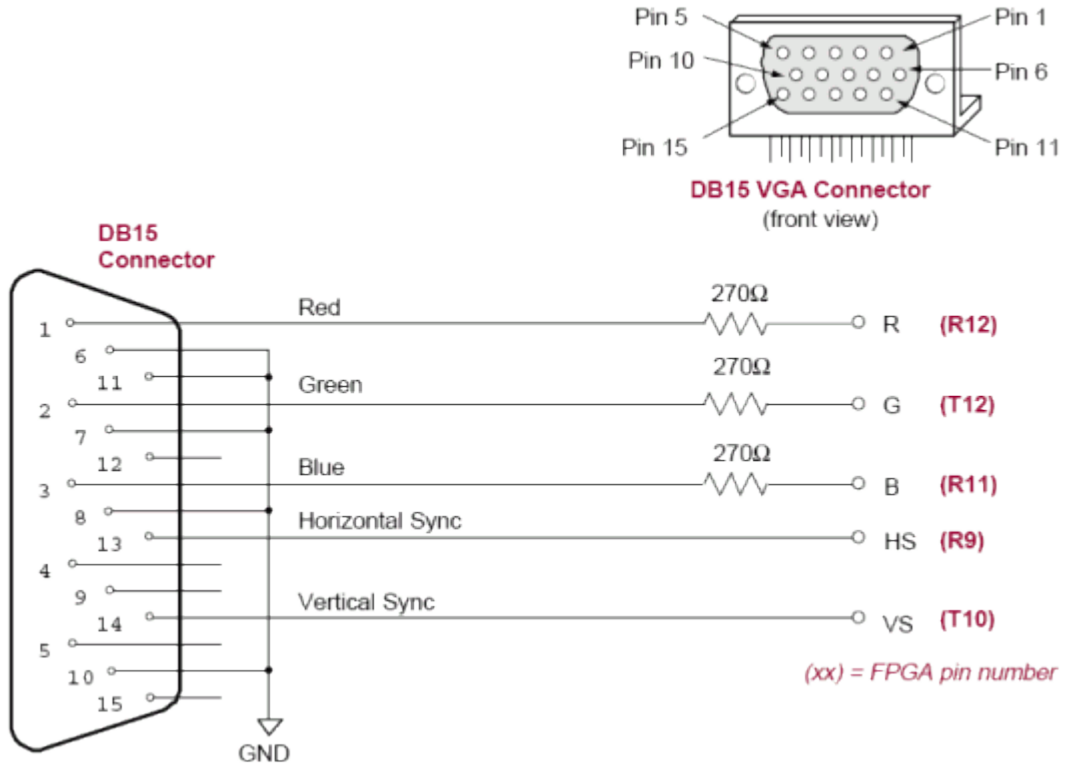
PIXEL BUFFER: Stores the digital data representing the image pixels before conversion to analog signals.

DAC (DIGITAL-TO-ANALOG CONVERTER): Converts the digital pixel data from the buffer into analog voltage levels for red, green, and blue color components.

VGA OUTPUT INTERFACE: Provides the formatted analog video signals (horizontal sync, vertical sync, and RGB) to the VGA monitor.

GENERATING VGA SIGNALS :

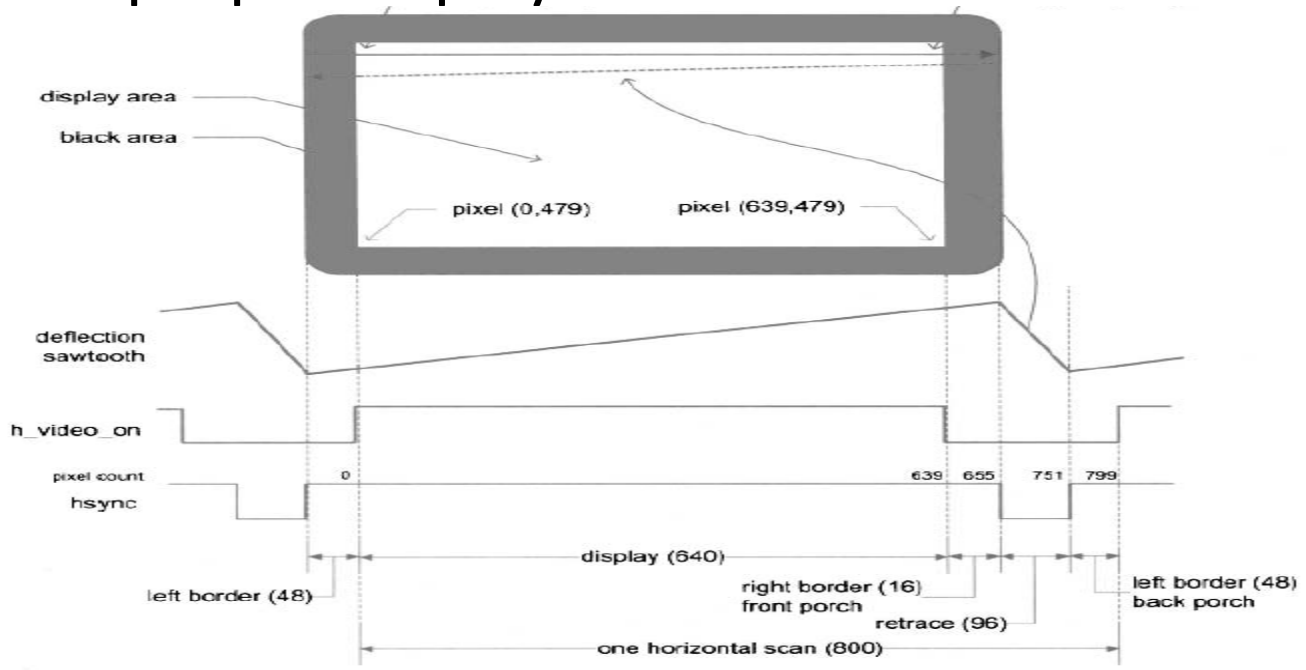
- Generating VGA signals involves creating precise horizontal and vertical synchronization signals along with corresponding pixel data for display.



TIMING DIAGRAM OF HORIZONTAL SYNC:

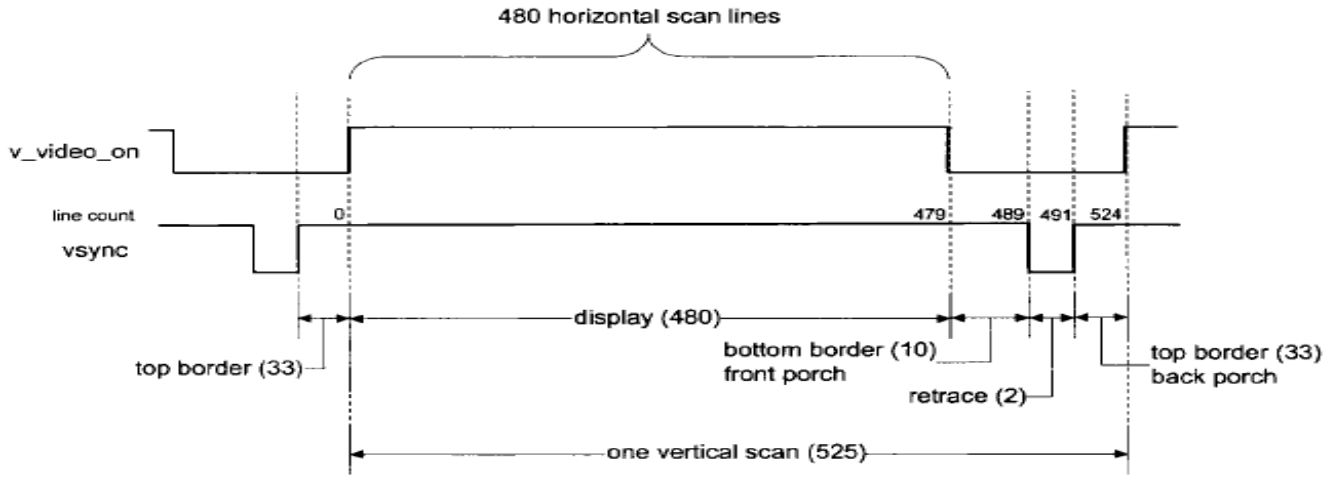
- The HSYNC (Horizontal Sync) timing diagram in VGA displays defines the timing intervals for synchronizing the horizontal scanning of a video signal, including the active video period, front porch, sync pulse, and back porch.

- This ensures the proper display of each horizontal line on a screen.



TIMING DIAGRAM OF VERTICAL SYNC:

- The timing diagram of VSYNC in VGA includes the VSYNC pulse, , which coordinates the refreshing of the display by indicating the start of a new frame, typically involving a VSYNC pulse, a back porch, a display interval, and a front porch.
- The correct timing ensures that the display is refreshed smoothly without flickering or tearing.

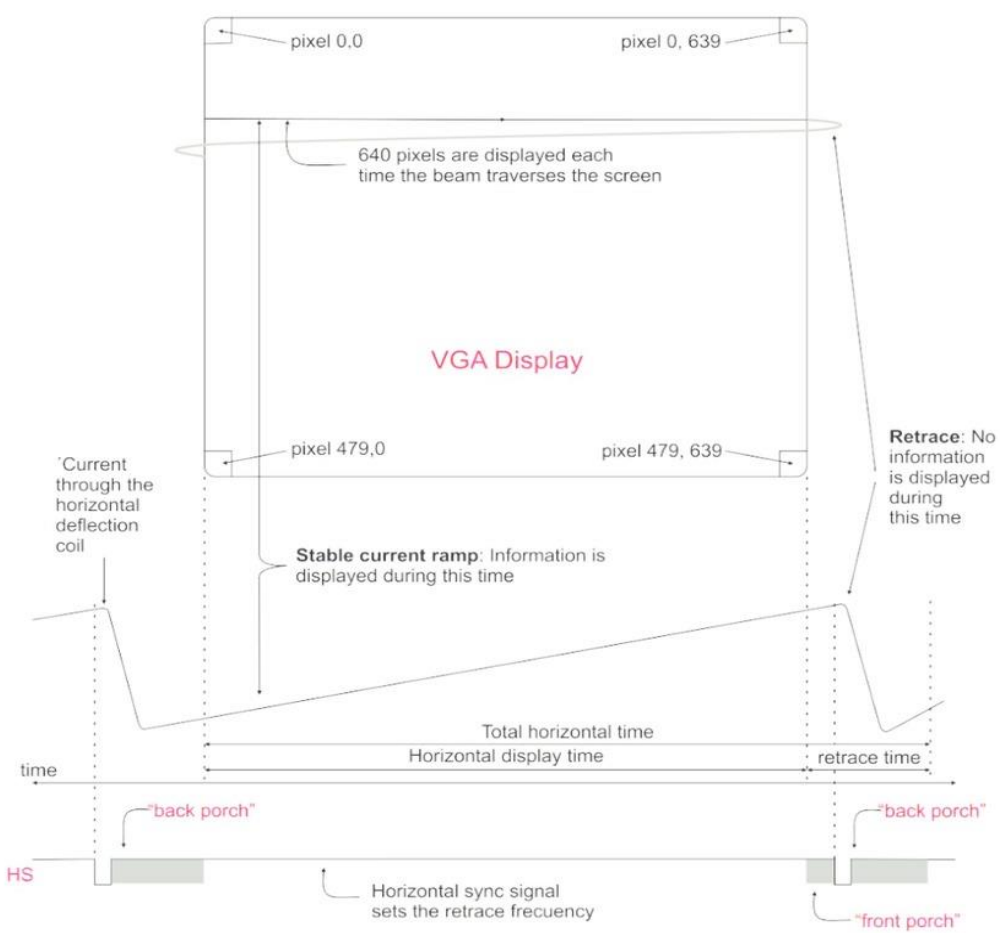


VGA DISPLAY OUTPUT:

- VGA display output transmits analog signals via a 15-pin connector, including separate RGB color signals and HSYNC/VSYNC for timing.

- It supports various resolutions and refresh rates, providing clear and detailed images on compatible monitors.

Resolution	Refresh Rate	Pixel Clock (MHz)	Display (H)	Inactive Area (H)	Display (V)	Inactive Area (V)
640×480	60	25.175	640	160	480	120



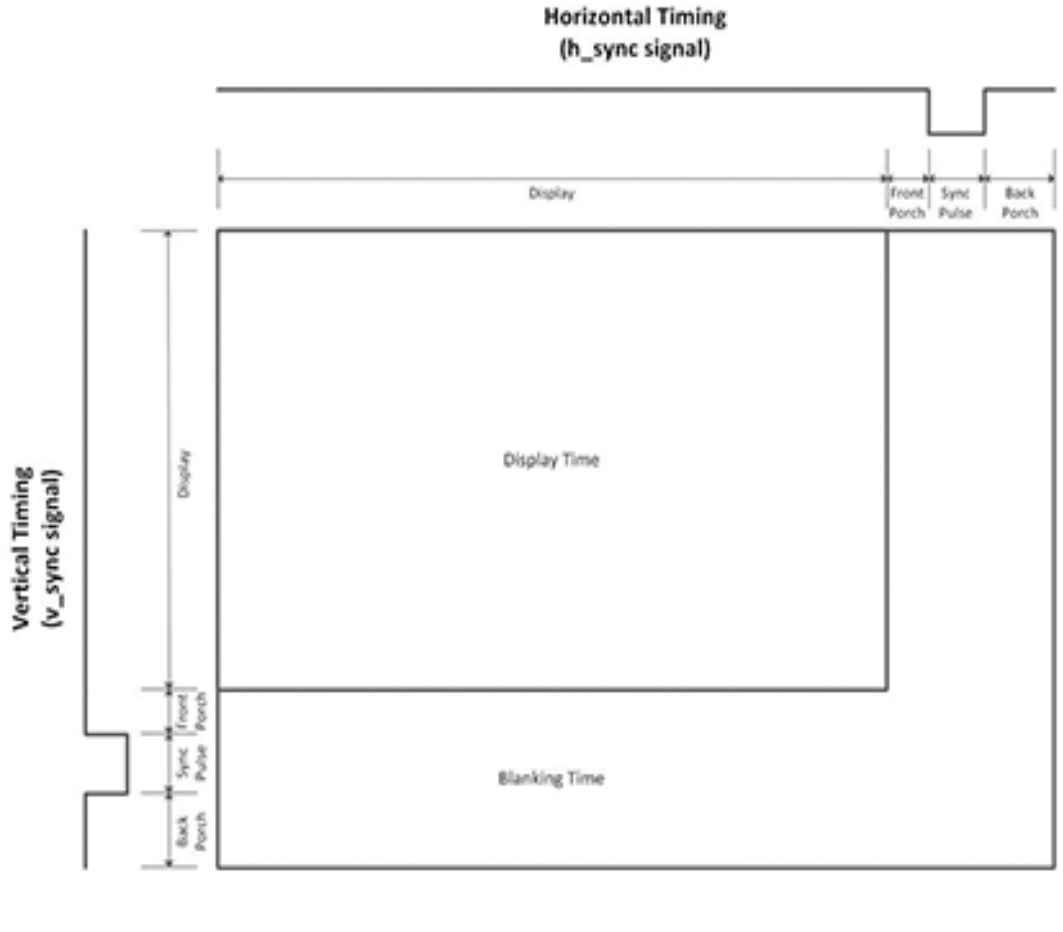
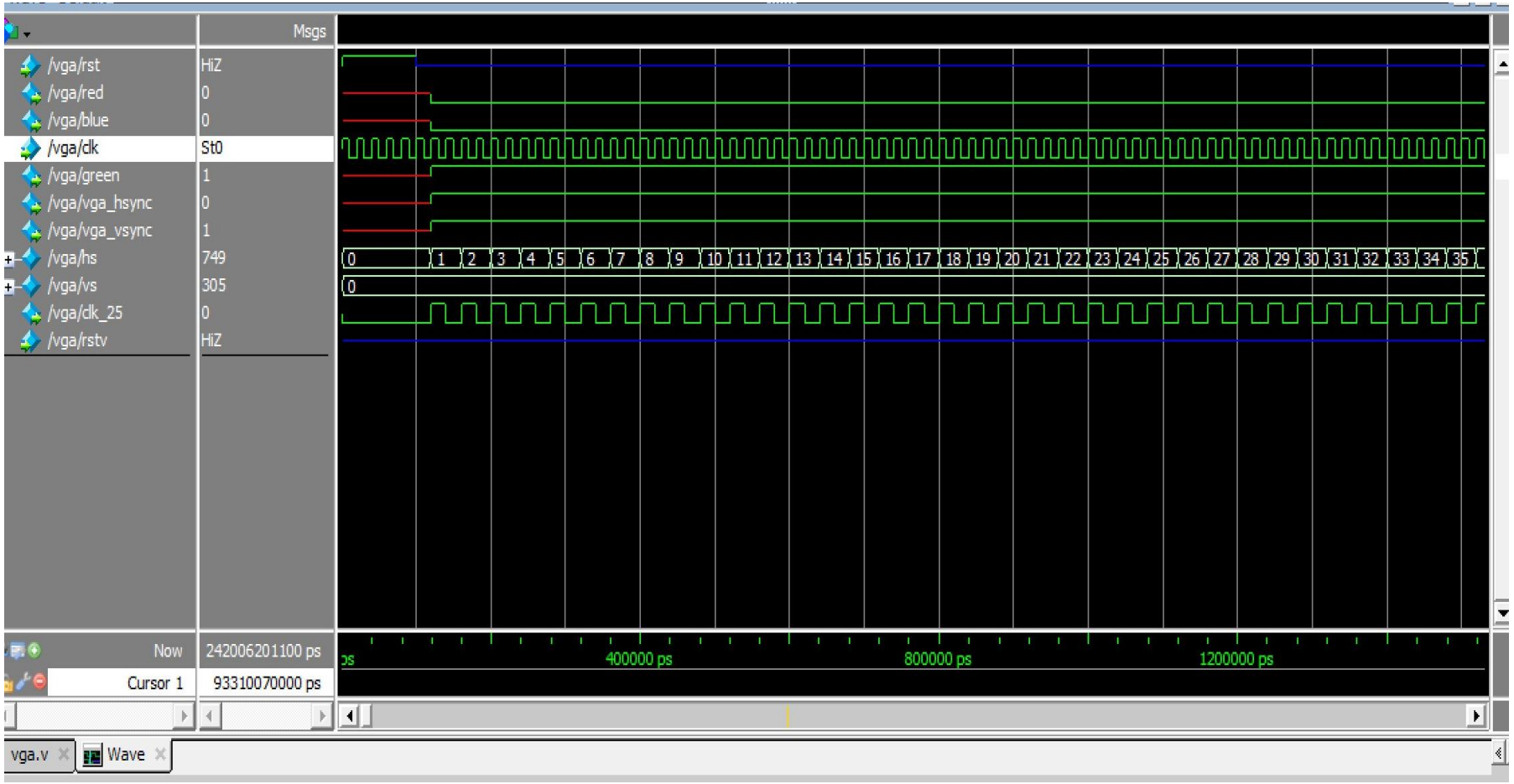


Fig: VGA DISPLAY OUTPUT

SIMULATION OF VGA CONTROLLER:



CONCLUSION:

- FPGAs provide a powerful platform for designing custom VGA controllers.
- Their flexibility, customization options, and parallel processing capabilities make them well-suited for this task.
- By implementing a VGA controller using FPGAs, we gain control over the video display generation process and can potentially achieve specialized functionalities.

THANKYOU