

Edition 2021-22

Digital Logic

PEN-Drive / G-Drive Course / VOD & Tablet Users

Workbook

Computer Science Engineering
Information Technology

GATE / ESE / PSUs



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Digital Logic

PEN-Drive / G-Drive Course / VOD & Tablet Users

Workbook

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GATE ACADEMY ®

A/114-115, Smriti Nagar, Bhilai - 490 020 (C.G.)

Phone : 0788 - 4034176, 0788 - 3224176

Help Desk No. - +91-97131-13156

For Feedback & Suggestions...

info@gateacademy.co.in

GATE Syllabus

Boolean algebra

Combinational and sequential circuits

Minimization

Number representations

Computer arithmetic (fixed and floating point)

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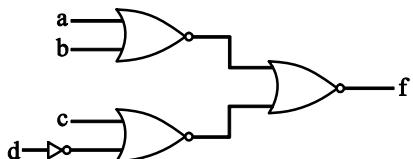
1

Logic Gates

Classroom Practice Questions :

- Q.1** The Boolean function $Y = AB + CD$ is to be realized using only 2-input NAND gates. The minimum number of gates required is _____.

Q.2 Which one of the following is the correct output (f) of the below circuit ?

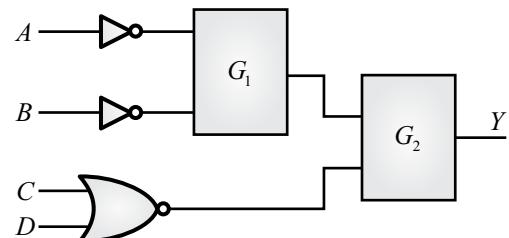


- (A) $(a + b)(c + \bar{d})$ (B) $(\bar{a} + \bar{b})(c + \bar{d})$
 (C) $(a + \bar{b})(c + \bar{d})$ (D) $(a + b)(\bar{a} + \bar{d})$

- Q.3** The Boolean expression $Y(A, B, C) = A + BC$ is to be realized using 2-input gates of only one type. What is the minimum number of gates required for the realization ?
_____.

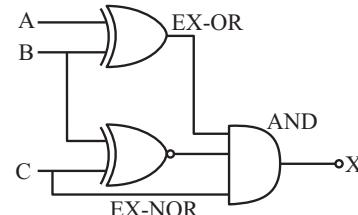
- Q.4** The minimum number of 2-input NAND gates required to implement the Boolean function $Z = A\bar{B}C$, assuming that A , B and C are available is [GATE 1998, IIT Delhi]

- Q.5** In the figure shown, the output Y is required to be $Y = AB + \overline{C}\overline{D}$. The gates G_1 and G_2 must be, [GATE 2015, IIT Kanpur]



- (A) NOR, OR (B) OR, NAND
(C) NAND, OR (D) AND, NAND

- Q.6**



For the logic circuit shown in the above figure, what is the required input condition (A, B, C) to make output X = 1 ?

- (A) 1, 0, 1 (B) 0, 0, 1
(C) 1, 1, 1 (D) 0, 1, 1

- Q.7** Match the logic gates in Column A with their equivalents in Column B.

[GATE 2010, IIT Guwahati]

	Column A	Column B
P.		
Q.		
R.		
S.		

Codes : P Q R S

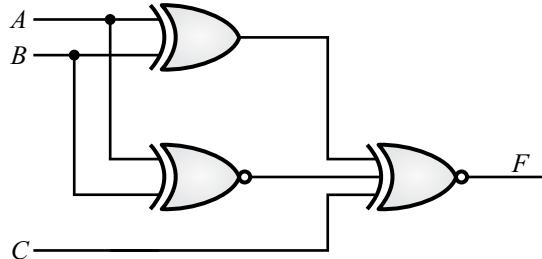
- (A) 2 4 1 3
- (B) 4 2 1 3
- (C) 2 4 3 1
- (D) 4 2 3 1

Q.8 Which one of the following expressions does NOT represent exclusive NOR of x and y ? [GATE 2013, IIT Bombay]

- (A) $xy + x'y'$
- (B) $x \oplus y'$
- (C) $x' \oplus y$
- (D) $x' \oplus y'$

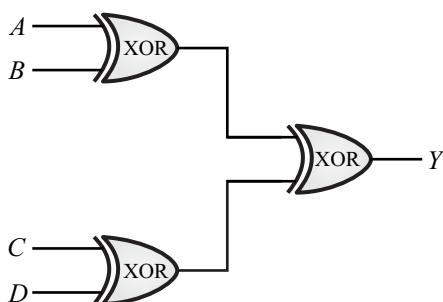
Q.9 For the output F to be 1 in the logic circuit shown, the input combination should be

[GATE 2010, IIT Guwahati]



- (A) $A = 1, B = 1, C = 0$
- (B) $A = 1, B = 0, C = 0$
- (C) $A = 0, B = 1, C = 0$
- (D) $A = 0, B = 0, C = 1$

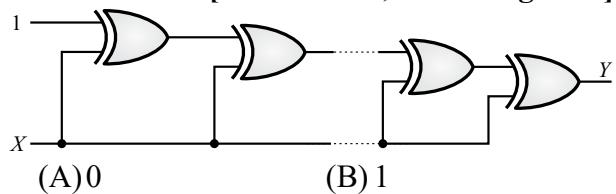
Q.10 A, B, C and D are input bits and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct? [GATE 2007, IIT Kanpur]



- (A) S is always either zero or odd.
- (B) S is always either zero or even.
- (C) $S = 1$ only if the sum of A, B, C and D is even.
- (D) $S = 1$ only if the sum of A, B, C and D is odd.

Q.11 If the input to the digital circuit consisting of a cascade of 20 X-OR gates is X , then the output Y is equal to

[GATE 2002, IISc Bangalore]



- (A) 0
- (B) 1
- (C) \bar{X}
- (D) X

Q.12 Let $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and \oplus is the XOR operator.

Which one of the following must always be TRUE? [GATE 2016, IISc Bangalore]

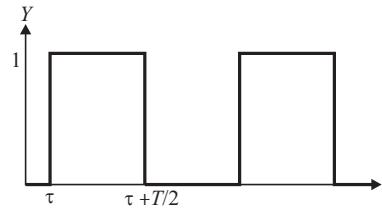
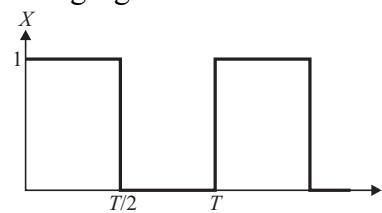
- (A) $x_1 x_2 x_3 x_4 = 0$
- (B) $x_1 x_3 + x_2 = 0$
- (C) $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
- (D) $x_1 + x_2 + x_3 + x_4 = 0$

Q.13 A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles

[GATE 2013, IIT Bombay]

- (A) an AND gate
- (B) an OR gate
- (C) an XOR gate
- (D) a NAND gate

Q.14 Two square wave of equal period T , but with a time delay τ are applied to a digital circuit whose truth table is shown in the following figure.

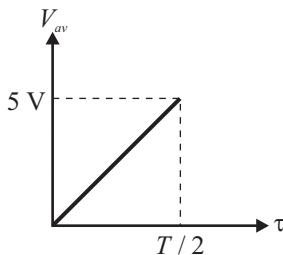


Truth table shown below,

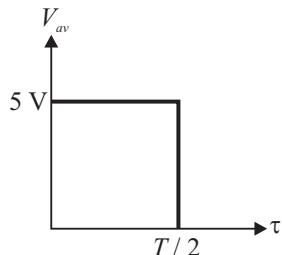
X	Y	Output
0	0	1
0	1	0
1	0	0
1	1	1

The high and the low levels of the output of the digital circuit are 5 V and 0 V, respectively. Which one of the following figures shows the correct variation of the average value of the output voltage of τ for $0 < t < (T/2)$? [GATE 2007, IIT Kanpur]

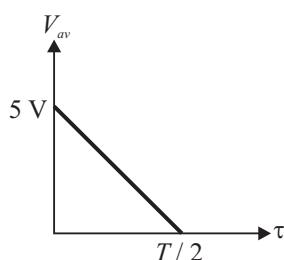
(A)



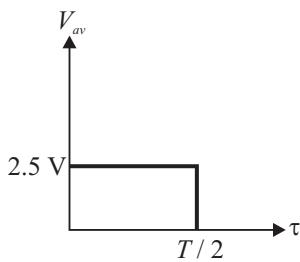
(B)



(C)



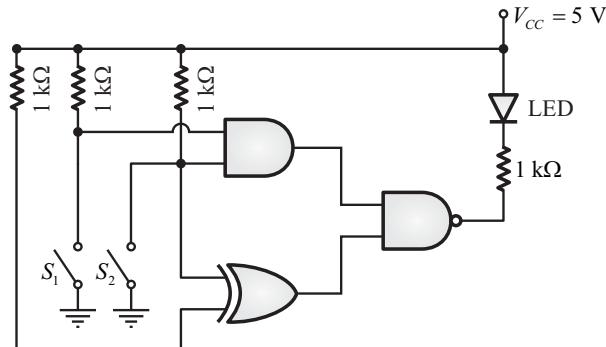
(D)



Q.15 Assume that only x and y logic input are available, and their complements \bar{x} and \bar{y} are not available. What is the minimum number of 2-input NAND gates required to implement $x \oplus y$? _____.

Q.16 In the given figure, the LED

[GATE 2001, IIT Kanpur]



(A) Emits light when both S_1 and S_2 are closed.

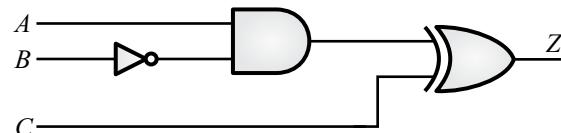
(B) Emits light when both S_1 and S_2 are opened.

(C) Emits light when S_1 is opened and S_2 is closed.

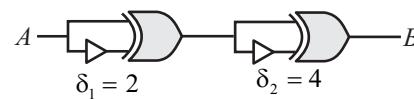
(D) Doesn't emit light, irrespective of the switch positions.

Q.17 All the logic gates shown in the figure have a propagation delay of 20 ns. Let $A = C = 0$ and $B = 1$ unit time $t = 0$. At $t = 0$, all the inputs flip (i.e. $A = C = 1$ and $B = 0$) and remain in that state. For $t > 0$, output $Z = 1$ for a duration (in ns) of _____.

[GATE 2015, IIT Kanpur]



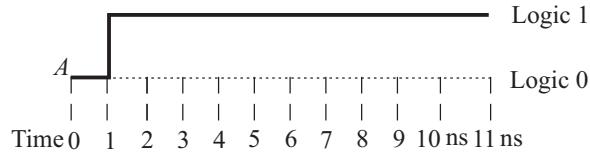
Q.18 Consider the following circuit composed of XOR gates as non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2$ ns and $\delta_2 = 4$ ns as shown in the figure. Both XOR gates and all wires have

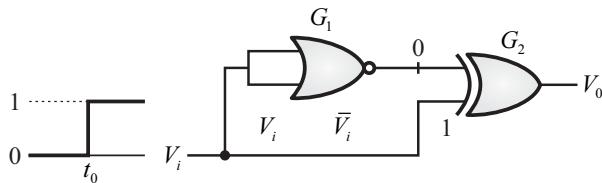
zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?

[GATE 2003, IIT Madras]



Q.19 The gates G_1 and G_2 in figure have propagation delays of 10 nsec and 20 nsec respectively. If the input V_i makes an abrupt change from logic 0 to 1 at time $t = t_0$, then the output waveform V_o is

[GATE 2002, IISc Bangalore]



$$z(t_1 = t_0 + 10 \text{ nsec}, t_2 = t_0 + 20 \text{ nsec},$$

$$t_3 = t_0 + 30 \text{ nsec})$$

-

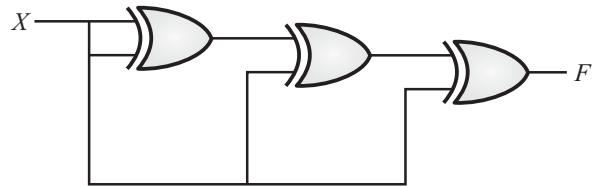
Self-Practice Questions :

Q.1 Consider the logic circuit with input signal TEST shown in the figure. All gates in the figure shown have identical non-zero delay. The signal TEST which was at logic LOW is switched to logic HIGH. The output



- (A) Stays HIGH throughout
 - (B) Stays LOW throughout
 - (C) Pulses from LOW to HIGH to LOW
 - (D) Pulses from HIGH to LOW to HIGH

Q.2 For the circuit shown below the output F is given by



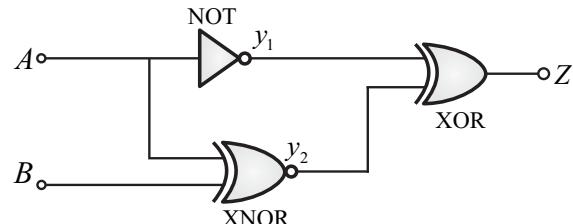
- (A) $F = 1$ (B) $F = 0$
 (C) $F \equiv X$ (D) $F = \bar{X}$

Q.3 Minimum number of 2-input NAND gates required to implement the function, $F = (\bar{X} + \bar{Y})(Z + W)$ is

Q.4 Indicate which of the following logic gates can be used to realize all possible combinational Logic functions.

- (A) OR gates only
 - (B) NAND gates only
 - (C) EX-OR gates only
 - (D) NOR gates only

Q.5 For the combinational circuit shown in figure,



Which of the following truth table is correct?

(A)	A	B	Z
	0	0	0
	0	1	1
	1	0	0
	1	1	1

(B)	A	B	Z
	0	0	1
	0	1	0
	1	0	0
	1	1	1

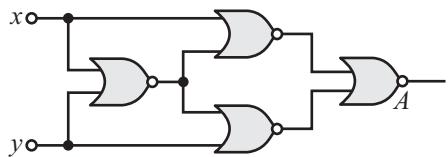
(C)	A	B	Z
	0	0	0
	0	1	1
	1	0	1
	1	1	0

(D)	A	B	Z
	0	0	1
	0	1	0
	1	0	1
	1	1	0

Q.6 Boolean expression for the output of XNOR (equivalence) logic gate with inputs A and B is

- (A) $A\bar{B} + \bar{A}B$
- (B) $\bar{A}\bar{B} + AB$
- (C) $(\bar{A} + B)(A + \bar{B})$
- (D) $(\bar{A} + \bar{B})(A + B)$

Q.7 Identify the logic function performed by the circuit shown in figure



- (A) Exclusive OR
- (B) Exclusive NOR
- (C) NAND
- (D) NOR

Q.8 The output of a logic gate is ‘1’ when all its inputs are at logic ‘0’. The gate is either

- (A) a NAND or an EX-OR gate.
- (B) a NOR or an EX-NOR gate.
- (C) an OR or an EX-NOR gate.
- (D) an AND or an EX-OR gate.

Q.9 Any Boolean function can be realized using only

- (A) NAND gate
- (B) AND gate
- (C) OR gate
- (D) NOT gate

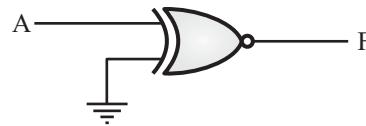
Q.10 The minimum number of NAND gates required to implement the Boolean function $A + A\bar{B} + A\bar{B}C$ is equal to

- (A) Zero
- (B) 1
- (C) 4
- (D) 7

Q.11 If A and B are the inputs to a logic gate, then match the logic with its output

- | | |
|----------|--|
| (a) NAND | (i) $\overline{\bar{A} + \bar{B}}$ |
| (b) NOR | (ii) $\bar{A} + \bar{B}$ |
| (c) XNOR | (iii) $\overline{\bar{A}\bar{B}} + AB$ |
| (d) AND | (iv) $\bar{A} \cdot \bar{B}$ |
- (A)a-ii, b-i, c-iii, d-iv
 (B)a-ii, b-iv, c-iii, d-i
 (C)a-i, b-iv, c-ii, d-iii
 (D)a-iii, b-ii, c-iv, d-i

Q.12 The output of the logic gate in figure is



- (A) 0
- (B) 1
- (C) \bar{A}
- (D) A

Q.13 What happens when a bit –string is XORed with itself n – times as shown :

$$[B \oplus (B \oplus (B \oplus (B \dots n \text{ times})))]$$

- (A) Complements when n is even
- (B) Complements when n is odd
- (C) Divides by 2^n always
- (D) Remains unchanged when n is even

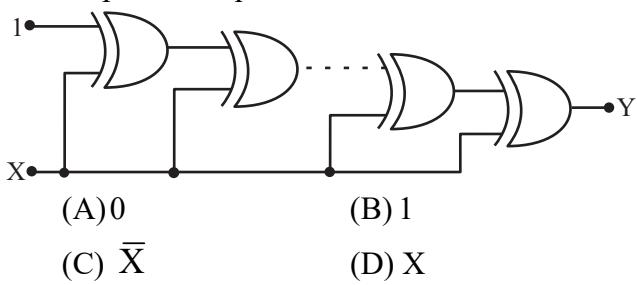
Q.14 Which of the following expression is not equivalent to \bar{x} ?

- (A) $x \text{ NAND } x$
- (B) $x \text{ NOR } x$
- (C) $x \text{ NAND } 1$
- (D) $x \text{ NOR } 1$

Q.15 The output of a logic gate is “1” when all its inputs are at logic “0”. The gate is either

- (A) A NAND or an EX-OR gate.
- (B) A NOR or an EX-OR gate.
- (C) An AND or an EX-NOR gate.
- (D) A NOR or an EX-NOR gate.

- Q.16** If the input to the digital circuit consisting of a cascade of 20 X-OR gates is X, then the output Y is equal to



- Q.17** The expression $Y = \overline{AB}$ is equivalent to

- (A) $\overline{A} + \overline{B}$ (B) $AB + A$
 (C) $A + B$ (D) AB

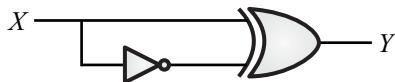
- Q.18** The Boolean function $Y = AB + CD$ is to be realized using only 2-input NAND gates. The minimum number of gates required is

- (A) 2 (B) 3
 (C) 4 (D) 5

- Q.19** The complete set of only those Logic Gates designated as Universal Gates is

- (A) NOT, OR and AND Gates.
 (B) XNOR, NOR and NAND Gates.
 (C) NOR and NAND Gates.
 (D) XOR, NOR and NAND Gates.

- Q.20** The output Y of the logic circuit given below is

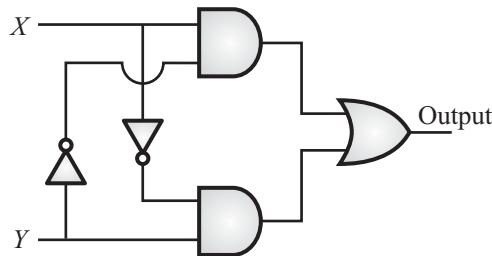


- (A) 1 (B) 0
 (C) X (D) \bar{X}

- Q.21** Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?

- (A)
 (B)
 (C)
 (D)

- Q.22** The logic evaluated by the circuit at the output is

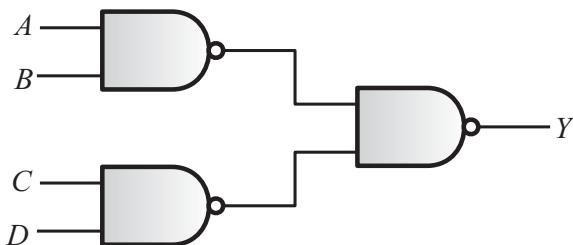


- (A) $X\bar{Y} + Y\bar{X}$
 (B) $(\overline{X+Y})XY$
 (C) $(\overline{XY})XY$
 (D) $\bar{X}Y + X\bar{Y} + X + Y$

- Q.23** The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

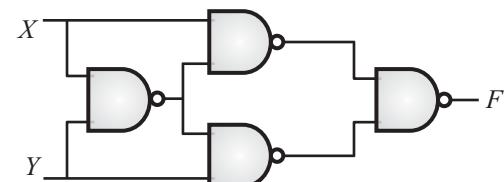
- (A) 4 (B) 5
 (C) 6 (D) 7

- Q.24** In the logic circuit shown in the figure, Y is given by



- (A) $Y = ABCD$
 (B) $Y = (A+B)(C+D)$
 (C) $Y = A+B+C+D$
 (D) $Y = AB+CD$

- Q.25** The Boolean function $F(X,Y)$ realized by the given circuit is



- (A) $\bar{X}\bar{Y} + X\bar{Y}$ (B) $\bar{X}\bar{Y} + XY$
 (C) $X+Y$ (D) $\bar{X} \cdot \bar{Y}$



Answer Keys

Classroom Practice Questions									
1.	3	2.	A	3.	3	4.	C	5.	A
6.	D	7.	D	8.	D	9.	D	10.	B
11.	B	12.	C	13.	C	14.	C	15.	4
16.	D	17.	40	18.	D	19.	B		
Self-Practice Questions									
1.	D	2.	B	3.	B	4.	B, D	5.	A
6.	B, C	7.	B	8.	B	9.	A	10.	A
11.	B	12.	C	13.	D	14.	D	15.	D
16.	B	17.	A	18.	B	19.	C	20.	A
21.	D	22.	A	23.	A	24.	D	25.	A

2

Boolean Algebra

Classroom Practice Questions :

Q.1 For the identity $AB + \bar{A}C + BC = AB + \bar{A}C$, the dual form is

[GATE 1998, IIT Delhi]

- (A) $(A+B)(\bar{A}+C)(B+C)$
 $= (A+B)(\bar{A}+C)$
- (B) $(\bar{A}+\bar{B})(A+\bar{C})(\bar{B}+\bar{C})$
 $= (\bar{A}+\bar{B})(A+\bar{C})$
- (C) $(A+B)(\bar{A}+C)(B+C)$
 $= (\bar{A}+\bar{B})(A+\bar{C})$
- (D) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C} = \bar{A}\bar{B} + A\bar{C}$

Q.2 The Boolean function $x'y' + xy + x'y$ is equivalent to

[GATE 2004, IIT Delhi]

- (A) $x' + y'$ (B) $x + y$
 (C) $x + y'$ (D) $x' + y$

Q.3 If x and y are Boolean variables which one of the following is the equivalent of $x \oplus y \oplus xy$ is

- (A) $x + \bar{y}$ (B) $x + y$
 (C) 0 (D) 1

Q.4 The Boolean expression

$\bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z + XY\bar{Z} + X\bar{Y}Z + XYZ$ can be simplified to

[GATE 2003, IIT Madras]

(A) $X\bar{Z} + \bar{X}Z + YZ$

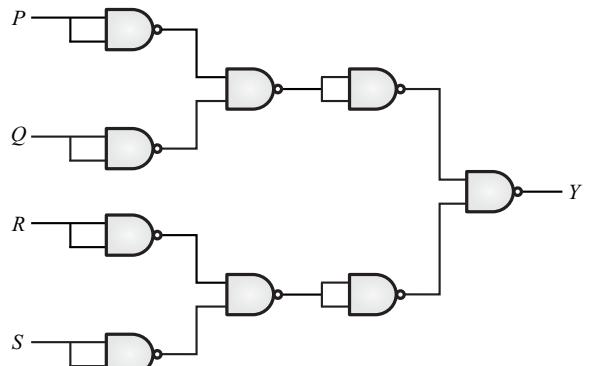
(B) $XY + \bar{Y}Z + Y\bar{Z}$

(C) $\bar{X}Y + YZ + XZ$

(D) $\overline{XY} + Y\bar{Z} + \bar{X}Z$

Q.5 For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is

[GATE 2002, IISc Bangalore]



(A) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$

(B) $P + Q + R + S$

(C) $(\bar{P} + \bar{Q}) + (\bar{R} + \bar{S})$

(D) $(P + Q) + (R + S)$

Q.6 Let \oplus denote the exclusive OR(XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q

$$F(P, Q) = (1 \oplus P) \oplus (P \oplus Q) \oplus (P \oplus Q)$$

$$\oplus (Q \oplus 0)$$

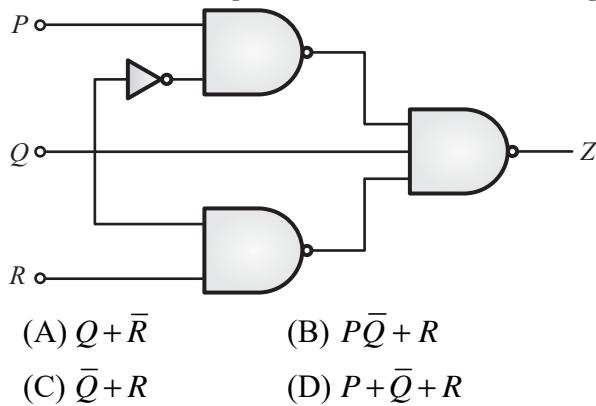
The equivalent expression for F is

[GATE 2014, IIT Kharagpur]

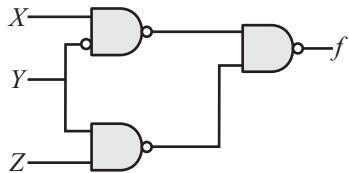
- (A) $P + Q$ (B) $\overline{P+Q}$
 (C) $P \oplus Q$ (D) $\overline{P \oplus Q}$

Q.7 For a three-input logic circuit shown below, the output 'Z' can be expressed as

[GATE 2017, IIT Roorkee]



Q.8 Consider the following circuit.



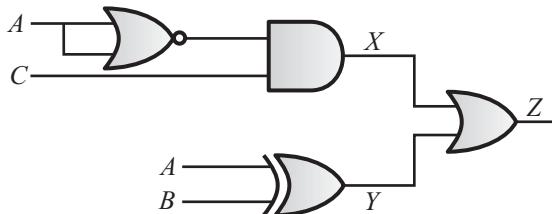
Which one of the following is TRUE?

[GATE 2005, IIT Bombay]

- (A) F is independent of X
 (B) F is independent of Y
 (C) F is independent of Z
 (D) None of X, Y, Z is redundant

Q.9 For the logic circuit shown in figure write the expression for Z.

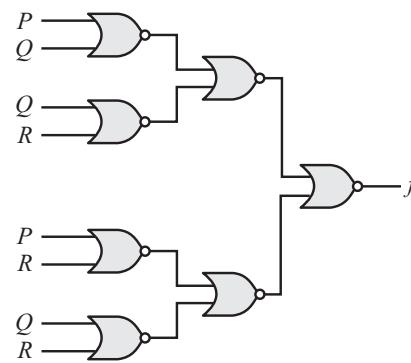
[GATE 1998, IIT Delhi]



- (A) $\overline{AC} + A\overline{B} + \overline{AB}$
 (B) $\overline{AC} + A\overline{B}$
 (C) $AC + AB$
 (D) $AC + BC + AB$

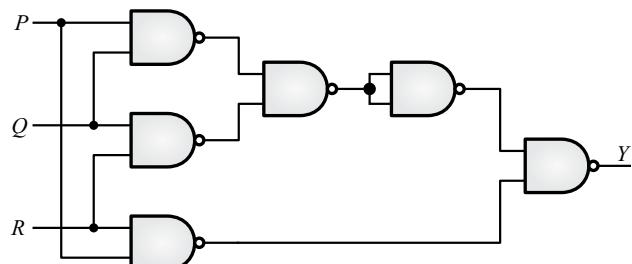
Q.10 What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below ?

[GATE 2010, IIT Guwahati]



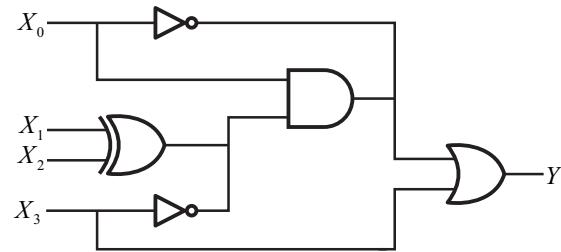
- (A) $Q + R$ (B) $\overline{P+Q}$
 (C) $\overline{P+R}$ (D) $\overline{P+Q+R}$

Q.11 The output Y in the circuit below is always "1" when [GATE 2011, IIT Madras]



- (A) two or more of the input P, Q, R are "0".
 (B) two or more of the inputs P, Q, R are "1".
 (C) any odd number of the inputs P, Q, R is "0".
 (D) any odd number of the inputs P, Q, R is "1".

Q.12 The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.



The number of distinct values of $X_3X_2X_1X_0$ (out of the 16 possible values) that give $Y=1$ is _____.

[GATE 2018, IIT Guwahati]

Q.13 The Boolean expression

$$F(X, Y, Z) = \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} \\ + XY\bar{Z} + XYZ$$

converted into canonical product of sum (POS) form is [GATE 2015, IIT Kanpur]

- (A) $(X+Y+Z)(X+Y+\bar{Z})(X+\bar{Y}+\bar{Z})$
 $(\bar{X}+Y+\bar{Z})$
- (B) $(X+\bar{Y}+Z)(\bar{X}+Y+\bar{Z})(\bar{X}+\bar{Y}+Z)$
 $(\bar{X}+\bar{Y}+\bar{Z})$
- (C) $(X+Y+Z)(\bar{X}+Y+\bar{Z})(X+\bar{Y}+Z)$
 $(\bar{X}+\bar{Y}+\bar{Z})$
- (D) $(X+\bar{Y}+\bar{Z})(\bar{X}+Y+Z)(\bar{X}+\bar{Y}+Z)$
 $(X+Y+Z)$

Q.14 The product of sum expression of a Boolean function $F(A, B, C)$ of three variables is given by

$$F(A, B, C) = (A+B+\bar{C}).(A+\bar{B}+\bar{C}) \\ .(\bar{A}+B+C).(\bar{A}+\bar{B}+\bar{C})$$

The canonical sum of product expression of $F(A, B, C)$ is given by

[GATE 2018, IIT Guwahati]

- (A) $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$
- (B) $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$
- (C) $A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$
- (D) $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$

Q.15 A function of Boolean variables X, Y and Z is expressed in terms of the minterms as

$$F(X, Y, Z) = \sum m(1, 2, 5, 6, 7)$$

Which one of the product of sums given below is equal to the function $F(X, Y, Z)$?

[GATE 2015, IIT Kanpur]

- (A) $(\bar{X}+\bar{Y}+\bar{Z})(\bar{X}+Y+Z)(X+\bar{Y}+\bar{Z})$
- (B) $(X+Y+Z)(X+\bar{Y}+\bar{Z})(\bar{X}+Y+Z)$

- (C) $(\bar{X}+\bar{Y}+Z)(\bar{X}+Y+\bar{Z})$
 $(X+\bar{Y}+Z)(X+Y+\bar{Z})(X+Y+Z)$
- (D) $(X+Y+\bar{Z})(\bar{X}+Y+Z)$
 $(\bar{X}+Y+\bar{Z})(\bar{X}+\bar{Y}+Z)(\bar{X}+\bar{Y}+\bar{Z})$

Q.16 The minterm expansion of

$$f(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$$

[GATE 2010, IIT Guwahati]

- (A) $m_2 + m_4 + m_6 + m_7$
- (B) $m_0 + m_1 + m_3 + m_5$
- (C) $m_0 + m_1 + m_6 + m_7$
- (D) $m_2 + m_3 + m_4 + m_5$

Q.17 The simplified SOP (Sum of Product) form of the Boolean expression

$$(P + \bar{Q} + \bar{R}).(P + \bar{Q} + R).(P + Q + \bar{R})$$

is _____.

[GATE 2011, IIT Madras]

- (A) $(\bar{P}.Q + \bar{R})$ (B) $(P + \bar{Q}.\bar{R})$
- (C) $(\bar{P}.Q + R)$ (D) $(P.Q + R)$

Q.18 From the table, choose the correct logical expression for Q .

[GATE 2000, IIT Kharagpur]

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
Q	0	0	0	1	0	1	1	1

- (A) $AB + BC + CA$ (B) $A + B + C$
 (C) $A\bar{B} + B\bar{C} + C\bar{A}$ (D) $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$

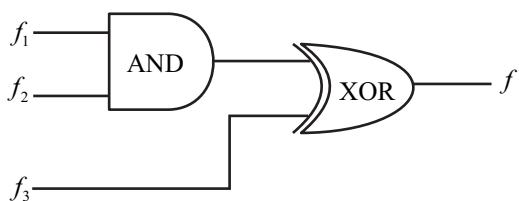
Q.19 A Boolean function f of two variables x and y is defined as follows

$$f(0, 0) = f(0, 1) = f(1, 1) = 1; f(1, 0) = 0$$

Assuming complements of x and y are not available, the minimum cost solution for realizing f using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

[GATE 2004, IIT Delhi]

For the following circuit with one AND gate and one XOR gate, the output function f can be expressed as:



[GATE 2019, IIT Madras]

- (A) $\Sigma(7,8,11)$
- (B) $\Sigma(2,7,8,11,14)$
- (C) $\Sigma(2,14)$
- (D) $\Sigma(0,2,3,5,6,7,8,11,14,15)$

Q.28 Which one of the following is Not a valid identity? [GATE 2019, IIT Madras]

- (A) $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
- (B) $(x + y) \oplus z = x \oplus (y \oplus z)$
- (B) $x \oplus y = x + y$, if $xy = 0$
- (C) $x \oplus y = (xy + x'y)'$

Q.29 The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates.

$$(ab).c + (\bar{a}.c).d + (b.c).d + a.d$$

What is the function finally realized?

[GATE 2007, IIT Kanpur]

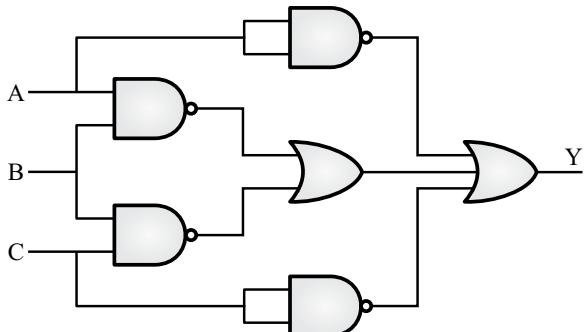
- (A) 1
- (B) $\bar{a} + \bar{b} + \bar{c} + \bar{d}$
- (C) $\bar{a} + b + \bar{c} + \bar{d}$
- (D) $\bar{a} + \bar{b} + c + \bar{d}$

Self-Practice Questions :

Q.1 The number of Boolean functions that can be generated by n variables is equal to

- (A) $2^{2^{n-1}}$
- (B) 2^{2^n}
- (C) 2^{n^1}
- (D) 2^n

Q.2 For the logic circuit shown in figure, the output is equal to

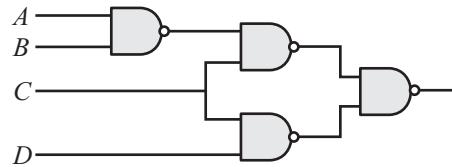


- (A) \overline{ABC}
- (B) $\bar{A} + \bar{B} + \bar{C}$
- (C) $\overline{AB} + \overline{BC} + \bar{A} + \bar{C}$
- (D) $\overline{AB} + \overline{BC}$

Q.3 The Boolean expression $\overline{A+B+C}$ is equal to

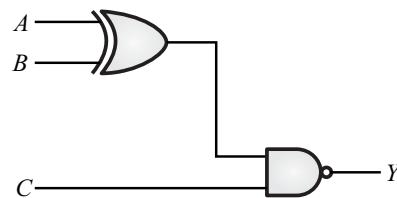
- (A) $\bar{A} + \bar{B} + \bar{C}$
- (B) $\bar{A} \cdot \bar{B} \cdot \bar{C}$
- (C) $\overline{A+B+C}$
- (D) $A \cdot (B+C)$

Q.4 The logic expression for the output of the circuit shown in figure 1 is



- (A) $\overline{AC} + \overline{BC} + CD$
- (B) $A\bar{C} + B\bar{C} + \bar{C}D$
- (C) $ABC + \overline{CD}$
- (D) $\overline{AB} + \overline{BC} + \overline{CD}$

Q.5 The Boolean expression of the output of the logic circuit shown in figure is



- (A) $Y = \bar{A}\bar{B} + AB + \bar{C}$
- (B) $Y = \bar{A}\bar{B} + AB + C$
- (C) $Y = \bar{A}B + \bar{A}B + C$
- (D) $Y = \bar{A}B + \bar{A}\bar{B} + C$

Q.6 The Boolean function $A + BC$ is a reduced form of

- (A) $AB + BC$
 (B) $(A + B) \cdot (A + C)$
 (C) $\bar{A}B + A\bar{B}C$
 (D) $(A + C) \cdot B$

Q.7 Let * be defined as $x^*y = \bar{x} + y$,

Let $z = x^*y$.

Value z^*x is

- (A) $\bar{x} + y$ (B) x
 (C) 0 (D) 1

Q.8 Which of the following operations is commutative but not associative?

- (A) AND (B) OR
 (C) NAND (D) EXOR

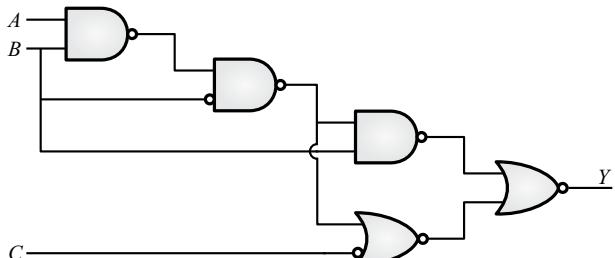
Q.9 The logical expression $y = A + \bar{A}B$ is equivalent to

- (A) $y = AB$ (B) $y = \bar{A}B$
 (C) $y = \bar{A} + B$ (D) $y = A + B$

Q.10 The logic function $f = \overline{(x.y)} + (\bar{x}.y)$ is the same as

- (A) $f = (x + y)(\bar{x} + \bar{y})$
 (B) $f = \overline{(\bar{x} + \bar{y})(x + y)}$
 (C) $f = \overline{(x.y)}(\bar{x}.\bar{y})$
 (D) None of the above

Q.11 For the logic circuit shown in figure, the simplified Boolean expression for the output Y is

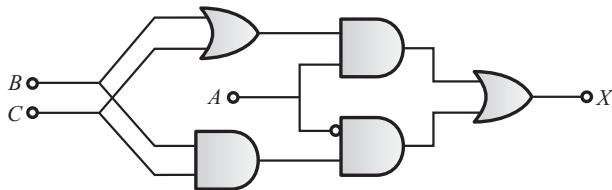


- (A) $A + B + C$ (B) A
 (C) B (D) C

Q.12 The expression $A + \bar{A}B$ is equivalent to

- (A) $A + B$ (B) $AB + A$
 (C) $A + \bar{B}$ (D) AB

Q.13 In the logic circuit shown in figure, the output X is



- (A) $A\bar{B} + B\bar{C} + C\bar{A}$
 (B) $A + B + C$
 (C) $AB + BC + CA$
 (D) $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$

Q.14 Let $f(A,B) = A' + B$. Simplified expression for function $f(f(x+y, y), z)$ is

- (A) $(x' + z)$
 (B) $x y z$
 (C) $xy' + z$
 (D) None of the above

Q.15 The number of distinct Boolean expression of 4 variables is

- (A) 16 (B) 256
 (C) 1024 (D) 65536

Q.16 If the function W, X, Y and Z are as follows

$$\begin{aligned} W &= R + \bar{P}Q + \bar{R}S \\ X &= P\bar{Q}\bar{R}\bar{S} + \bar{P}\bar{Q}\bar{R}S + P\bar{Q}RS \\ Y &= RS + \overline{PR + P\bar{Q} + \bar{P}\bar{Q}} \\ Z &= R + S + \overline{PQ + \bar{P}\bar{Q}\bar{R} + P\bar{Q}\bar{S}} \end{aligned}$$

Then

- (A) $W = Z, X = \bar{Z}$
 (B) $W = Z, X = Y$
 (C) $W = Y$
 (D) $W = Y = \bar{Z}$

Q.17 The Boolean expression $AC + B\bar{C}$ is equivalent to

- (A) $\bar{A}C + B\bar{C} + AC$
 (B) $\bar{B}C + AC + B\bar{C} + \bar{A}C\bar{B}$
 (C) $AC + B\bar{C} + \bar{B}C + ABC$
 (D) $ABC + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}C$

Q.18 The simplified form of the Boolean expression $Y = (\bar{A}BC + D)(\bar{A}D + \bar{B}\bar{C})$ can be written as

- (A) $\bar{A}D + \bar{B}\bar{C}D$
- (B) $AD + B\bar{C}D$
- (C) $(\bar{A} + D)(\bar{B}C + \bar{D})$
- (D) $A\bar{D} + BC\bar{D}$

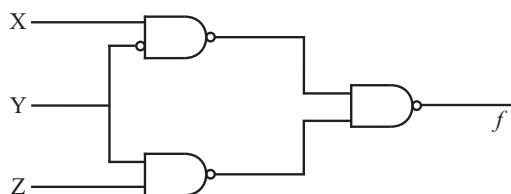
Q.19 The simplest form of the Boolean expression

$$AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$$

is

- | | |
|----------------|----------|
| (A) AD | (B) BC |
| (C) \bar{AB} | (D) AB |

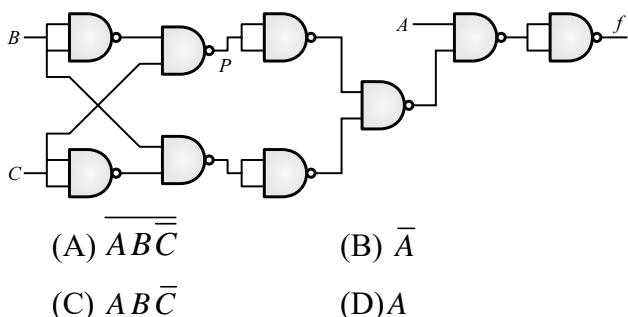
Q.20 Consider the following circuit.



Which one of the following is TRUE?

- (A) f is independent of X
- (B) f is independent of Y
- (C) f is independent of Z
- (D) None of X, Y, Z is redundant

Q.21 The point P in the following figure is stuck at 1. The output f will be



- (A) \overline{ABC}
- (B) \bar{A}
- (C) $AB\bar{C}$
- (D) A

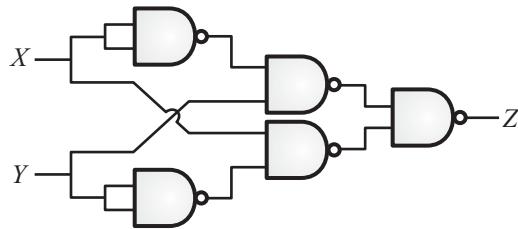
Q.22 If $X = 1$ in the logic equation

$$\left[X + Z \{ \bar{Y} + (\bar{Z} + X\bar{Y}) \} \right] \{ \bar{X} + \bar{Z}(X + Y) \} = 1$$

Then

- (A) $Y = Z$
- (B) $Y = \bar{Z}$
- (C) $Z = 1$
- (D) $Z = 0$

Q.23 The logic gate circuit shown in the figure realizes the function



- (A) XOR
- (B) XNOR
- (C) Half adder
- (D) Full adder

Q.24 The simplified SOP (Sum of product) form of the Boolean expression

$$(P + \bar{Q} + \bar{R})(P + \bar{Q} + R)(P + Q + \bar{R})$$

- (A) $(\bar{P}.Q + \bar{R})$
- (B) $(P + \bar{Q}.\bar{R})$
- (C) $(\bar{P}.Q + R)$
- (D) $(P.Q + R)$

Q.25 The truth table

X	Y	f(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

Represents the Boolean function

- (A) X
- (B) $X + Y$
- (C) $X \oplus Y$
- (D) Y

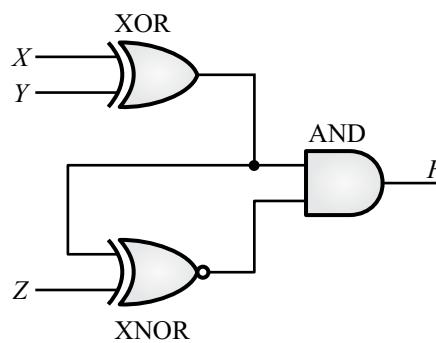
Q.26 The Boolean expression

$$(X + Y)(X + \bar{Y}) + \overline{(X\bar{Y}) + \bar{X}}$$

simplifies to

- (A) X
- (B) Y
- (C) XY
- (D) $X + Y$

Q.27 The output F in the digital logic circuit shown in the figure is



$$(A) F = \bar{X}YZ + X\bar{Y}Z$$

$$(B) F = \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z}$$

(A) $wx + w(x+y) + x(x+y) = x + wy$

(B) $\overline{wx}(\overline{y+z}) + \overline{wx} = \overline{w} + x + \overline{yz}$

(C) $(\overline{wx}(\overline{y+xz}) + \overline{wx})y = xy$

(D) $(w+y)(wxy + wyz) = wxy + wyz$

- Q.38** A function $F(A, B, C)$ defined by three Boolean variables A , B and C when expressed as sum of products is given by

$$F = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C}$$

where, \overline{A} , \overline{B} and \overline{C} are the complements of the respective variables. The product of sum (POS) form of the function F is

(A) $F = (A+B+C)$

(\overline{A}+\overline{B}+C)(\overline{A}+B+C)

(B) $F = (\overline{A}+\overline{B}+\overline{C})$

$$(\overline{A}+B+\overline{C})(A+\overline{B}+\overline{C})$$

(C) $F = (A+B+\overline{C})(A+\overline{B}+\overline{C})$

$$(\overline{A}+B+\overline{C})(\overline{A}+\overline{B}+C)$$

$$(\overline{A}+\overline{B}+\overline{C})$$

(D) $F = (\overline{A}+\overline{B}+C)(\overline{A}+B+C)$

$$(\overline{A}+\overline{B}+C)(A+\overline{B}+\overline{C})$$

$$(A+B+C)$$

- Q.39** The equivalent Boolean expression of $(R + \overline{T})(\overline{R} + T)(S + T) = F(R, S, T)$ is

(A) $R T + \overline{R} S \overline{T}$ (B) $R \overline{T} + R \overline{T} + ST$

(C) $R \overline{T} + R \overline{S} T$ (D) None of these

- Q.40** The Boolean expression $AB + \overline{A}C$ is equivalent to _____.

(A) $ABC + AB\overline{C} + \overline{A}BC$

(B) $ABC + AB\overline{C} + \overline{A}BC + \overline{A}\overline{B}C$

(C) $\overline{A}BC + AB\overline{C} + \overline{A}\overline{B}C$

(D) None of these

- Q.41** Minimize the logic expression

$$C + D + \overline{AB} + \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C}$$

(A) $C + \overline{A}B + \overline{C}D$ (B) $A\overline{B} + C\overline{D} + C$

(C) $C + D + \overline{A}B$ (D) None of these

- Q.42** If A and B are Boolean variables, which one of the following is equivalent to $A \oplus B \oplus AB$

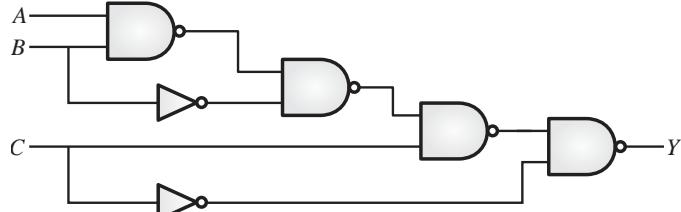
(A) 0

(B) $A + B$

(C) AB

(D) $A + \overline{B}$

- Q.43** For the circuit given below, the output Y is



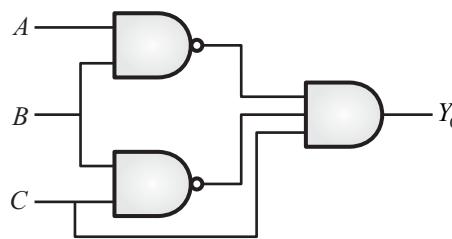
(A) $A + B + C$

(B) C

(C) B

(D) $\overline{AB} + \overline{BC}$

- Q.44** Which of the following is correct?



(A) Y_0 is independent of ' B '

(B) Y_0 is independent of A

(C) Y_0 is dependent of A and B

(D) None of the A, B, C is dependent



Answer Keys

Classroom Practice Questions									
1.	A	2.	D	3.	B	4.	B	5.	B
6.	D	7.	C	8.	A	9.	A	10.	A
11.	B	12.	8	13.	A	14.	B	15.	B
16.	A	17.	B	18.	A	19.	D	20.	A
21.	D	22.	A	23.	A	24.	C	25.	B
26.	A	27.	A	28.	B	29.	C		
Self-Practice Questions									
1.	B	2.	B, C	3.	B	4.	A	5.	A
6.	B	7.	B	8.	C	9.	D	10.	B
11.	C	12.	A	13.	C	14.	C	15.	D
16.	A	17.	D	18.	A	19.	D	20.	D
21.	D	22.	D	23.	A	24.	B	25.	A
26.	A	27.	A	28.	A	29.	C	30.	A
31.	C	32.	D	33.	C	34.	B	35.	A
36.	C	37.	C	38.	C	39.	A	40.	B
41.	C	42.	C	43.	B	44.	B		

3 K - Maps

Classroom Practice Questions :

- Q.1** The output expression for the Karnaugh map shown below is

[GATE 2016, IISc Bangalore]

		BC	00	01	11	10
		A	0	1	0	1
0	0	1	0	0	1	
	1	1	1	1	1	

- (A) $A + \bar{B}$ (B) $A + \bar{C}$
 (C) $\bar{A} + \bar{C}$ (D) $\bar{A} + C$

- Q.2** The output expression for the Karnaugh map shown below is

[GATE 2017, IIT Roorkee]

		CD	00	01	11	10
		AB	00	0	0	0
00	01	1	0	0	1	
	11	1	0	1	1	
01	10	0	0	0	0	
	11	0	0	0	0	

- (A) $B\bar{D} + BCD$ (B) $B\bar{D} + AB$
 (C) $\bar{B}\bar{D} + ABC$ (D) $\bar{B}\bar{D} + ABC$

- Q.3** Consider the following Boolean function with four variables

$$F(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14).$$

The function is [GATE 2007, IIT Kanpur]

- (A) Independent of one variables
 (B) Independent of two variables
 (C) Independent of three variables
 (D) Dependent on all variables

- Q.4** The Boolean expression for the truth table shown below is

[GATE 2005, IIT Bombay]

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- (A) $B(A+C)(\bar{A}+\bar{C})$
 (B) $B(A+\bar{C})(\bar{A}+C)$
 (C) $\bar{B}(A+C)(\bar{A}+C)$
 (D) $\bar{B}(A+C)(\bar{A}+\bar{C})$

- Q.5** The SOP (sum of products) form of a Boolean functions is $\Sigma(0,1,3,7,11)$, where inputs are A, B, C, D , (A is MSB, and D is LSB). The equivalent minimized expression of the function is

[GATE 2014, IIT Kharagpur]

- (A) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{B})(\bar{C}+D)$
 (B) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+D)$
 (C) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+\bar{D})$
 (D) $(\bar{B}+C)(A+\bar{B})(\bar{A}+\bar{B})(\bar{C}+D)$

- Q.6** The Boolean function $x'y' + xy + x'y$ is equivalent to [GATE 2004, IIT Delhi]
- (A) $x' + y'$ (B) $x + y$
 (C) $x + y'$ (D) $x' + y$

- Q.7** For the Boolean expression

$$f = \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}\bar{c} + ab\bar{c} + abc$$

the minimized Product of sum (POS) expression is [GATE 2011, IIT Madras]

- (A) $f = (b + \bar{c})(a + \bar{c})$
 (B) $f = (\bar{b} + c)(\bar{a} + c)$
 (C) $f = (\bar{b} + c)(a + \bar{c})$
 (D) $f = \bar{c} + abc$

- Q.8** From the table, choose the correct logical expression for Q .

[GATE 2000, IIT Kharagpur]

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
Q	0	0	0	1	0	1	1	1

- (A) $AB + BC + CA$ (B) $A + B + C$
 (C) $A\bar{B} + B\bar{C} + C\bar{A}$ (D) $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$

- Q.9** The simplified SOP (Sum of Product) form of the Boolean expression

$$(P + \bar{Q} + \bar{R})(P + \bar{Q} + R)(P + Q + \bar{R})$$

is _____.

[GATE 2011, IIT Madras]

- (A) $(\bar{P} \cdot Q + \bar{R})$ (B) $(P + \bar{Q} \cdot \bar{R})$
 (C) $(\bar{P} \cdot Q + R)$ (D) $(P \cdot Q + R)$

- Q.10** Consider the following Boolean expression for

$$F : (P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$$

The minimal sum-of-products form of F is _____.

[GATE 2014, IIT Kharagpur]

- (A) $PQ + QR + QS$ (B) $P + Q + R + S$
 (C) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$ (D) $\bar{P}R + \bar{P}RS + P$

- Q.11** $f(A, B, C, D) = \prod M(0, 1, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15)$ is a maxterm representation of Boolean function $f(A, B, C, D)$ where A is the MSB and D is the LSB. The equivalent minimized representation of this function is

[GATE 2015, IIT Kanpur]

- (A) $(A + \bar{C} + D)(\bar{A} + B + D)$
 (B) $A\bar{C}D + \bar{A}BD$
 (C) $\bar{A}C\bar{D} + A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D}$
 (D) $(B + \bar{C} + D)(A + \bar{B} + \bar{C} + D)(\bar{A} + B + C + D)$

- Q.12** The number of min-terms after minimizing the following Boolean expression is _____.

$$[D' + AB' + A'C + AC'D + A'C'D]'$$

[GATE 2015, IIT Kanpur]

- Q.13** In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

[GATE 2008, IISc Bangalore]

		ab	00	01	11	10
		cd	00	01	11	10
00	00		1	1		1
	01	X				
	11	X				
	10	1	1			X

$$(A) \bar{b}\bar{d} + \bar{a}\bar{d} \quad (B) \bar{a}\bar{b} + \bar{b}\bar{d} + \bar{a}\bar{b}\bar{d}$$

$$(C) \bar{b}\bar{d} + \bar{a}\bar{b}\bar{d} \quad (D) \bar{a}\bar{b} + \bar{b}\bar{d} + \bar{a}\bar{d}$$

- Q.14** Given the following Karnaugh map, which one of the following represents the minimal Sum - Of - Products of the map?

[GATE 2001, IIT Kanpur]

wx \ yz	00	01	11	10
00	0	x	0	x
01	x	1	x	1
11	0	x	1	0
10	0	1	x	0

Which of these expressions are equivalents of the expression $Y = A \oplus B \oplus C \oplus D$?

- (A) 1 and 2 (B) 1 and 4
 (C) 2 and 3 (D) 1 and 3

- Q.23** A logic circuit implements the Boolean function $f = \bar{x} \cdot y + x \cdot \bar{y} \cdot \bar{z}$. It is found that the input combination $x = y = 1$ can never occur. Taking this into account, a simplified expression for f is given by

[GATE 2007, IIT Kanpur]

- (A) $\bar{x} + \bar{y}.\bar{z}$ (B) $x + z$
 (C) $x + y$ (D) $y + x.\bar{z}$

- Q.24** The minimal sum-of-products expression for the logic function f represented by the given Karnaugh map is

[GATE 2009, IIT Roorkee]

RS	PQ	00	01	11	10
00	0	1	0	0	
01	0	1	1	1	
11	1	1	1	0	
10	0	0	1	0	

- (A) $QS + \overline{PRS} + PQR + \overline{PRS} + \overline{PQR}$
 (B) $\overline{QS} + \overline{PRS} + \overline{PQR} + \overline{PRS} + \overline{PQR}$
 (C) $\overline{PRS} + \overline{PQR} + \overline{PRS} + \overline{PQR}$
 (D) $P\overline{RS} + PQR + \overline{PRS} + \overline{PQR}$

- Q.25** Consider the Karnaugh map given below, where X represents “don’t care” and blank represents 0 [GATE 2017, IIT Roorkee]

ba	00	01	11	10
dc	00	x	x	
01	1			x
11	1			1
10		x	x	

Assume for all inputs (a, b, c, d), the respective complements ($\bar{a}, \bar{b}, \bar{c}, \bar{d}$) are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is

- Q.26** Following is the K-map of a Boolean function of five variables P, Q, R, S and X . The minimum sum-of-product (SOP) expression for the function is

[GATE 2016, IISc Bangalore]

		PQ	00	01	11	10
RS		00	0	0	0	0
		01	1	0	0	1
		11	1	0	0	1
		10	0	0	0	0

$$X = 0$$

RS	PQ	00	01	11	10
00		0	1	1	0
01		0	0	0	0
11		0	0	0	0
10		0	1	1	0

X=1

- (A) $\bar{P}\bar{Q}S\bar{X} + P\bar{Q}S\bar{X} + Q\bar{R}\bar{S}X + QR\bar{S}X$
 (B) $\bar{Q}S\bar{X} + Q\bar{S}X$
 (C) $\bar{Q}S X + Q\bar{S}\bar{X}$
 (D) $\bar{O}S + O\bar{S}$

- Q.27** The K-map for a Boolean function is shown in figure below. The number of essential prime implicants for this function is

		CD				
		AB	00	01	11	10
00			1	0	1	1
01			0	1	0	0
11			0	1	1	0
10			1	0	0	1

- Q.28** In the sum of products function $f(X, Y, Z) = \Sigma m(2, 3, 4, 5)$, the prime implicants are [GATE 2012, IIT Delhi]

- (A) $\bar{X}Y, X\bar{Y}$
 (B) $\bar{X}Y, X\bar{Y}\bar{Z}, X\bar{Y}Z$
 (C) $\bar{X}YZ, \bar{X}YZ, X\bar{Y}$
 (D) $\bar{X}YZ, \bar{X}YZ, X\bar{Y}\bar{Z}, X\bar{Y}Z$

- Q.29** The total number of prime implicants of the function

$$f(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 10)$$

is _____. [GATE 2015, IIT Kanpur]

- Q.30** Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

[GATE 2004, IIT Delhi]

- (A) $a'c$ and ac' (B) $a'c$ and $b'c$
 (C) $a'c$ only (D) ac' and bc'

- Q.31** Consider the Boolean function,

$$\begin{aligned} F(w, x, y, z) = & w'y + xy + \bar{w}xz \\ & + \bar{w}\bar{x}y + xz + \bar{x}\bar{y}\bar{z} \end{aligned}$$

Which one of the following is the complete set of essential prime implicants?

[GATE 2014, IIT Kharagpur]

- (A) $w, y, xz, \bar{x}\bar{z}$ (B) w, y, xz
 (C) $y, \bar{x}\bar{y}\bar{z}$ (D) $y, xz, \bar{x}\bar{z}$

- Q.32** For an n -variable Boolean function, the maximum number of prime implicants is

[GATE 2014, IIT Kharagpur]

- (A) $2(n-1)$ (B) $n/2$
 (C) 2^n (D) $2^{(n-1)}$

- Q.33** By inspecting the Karnaugh map plot of the switching function

$$F(x_1, x_2, x_3) = \Sigma(1, 3, 6, 7)$$

one can say that the redundant prime implicant is

- (A) \bar{x}_1x_3 (B) x_2x_3
 (C) x_1x_2 (D) x_3

- Q.34** What is the minimum number of 2-input NOR gates required two implement a 4-variable function expressed in sum-of-minterms form as $f = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$? Assume that all the inputs and their complements are available. Answer : _____.

[GATE 2019, IIT Madras]

- Q.35** Consider the minterm list form of a Boolean function F given below.

$$F(P, Q, R, S) = \Sigma m(0, 2, 5, 7, 9, 11)$$

$$+ d(3, 8, 10, 12, 14)$$

Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is _____.

[GATE 2018, IIT Guwahati]

Self-Practice Questions :

- Q.1** Find the minimum product of sums of the following expression $f = ABC + \bar{A}\bar{B}\bar{C}$.

- Q.2** A combination circuit has inputs A, B and C and its Karnaugh map is given in figure. The output of the circuit is

		AB	00	01	11	10
		C	0	1		1
0	0	1				
	1	1			1	

- (A) $(\bar{A}B + A\bar{B})C$ (B) $(\bar{A}B + A\bar{B})\bar{C}$
 (C) $A \oplus B \oplus C$ (D) $\bar{A}\bar{B}\bar{C}$

- Q.3** What is the equivalent Boolean expression in product-of-Sums form for the Karnaugh map given in fig?

		AB	00	01	11	10
		CD	00	1	1	
00	0	1				
	1	1				1
01	0	1				
	1					1
11	0	1				
	1					1
10	0			1	1	
	1					

- (A) $B\bar{D} + \bar{B}D$
 (B) $(B + \bar{C} + D)(\bar{B} + C + \bar{D})$
 (C) $(B + D)(\bar{B} + \bar{D})$
 (D) $(B + \bar{D})(\bar{B} + D)$

- Q.4** The minimal sum of products form of $f = A\bar{B}CD + \bar{A}BC + BCD + \bar{A}\bar{B}C$ is

- (A) $\bar{A}C + BD$ (B) $\bar{A}C + CD$
 (C) $AC + \bar{B}D$ (D) $A\bar{B} + C\bar{D}$

- Q.5** The minimized form of the logical expression $(\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C})$ is

(A) $\bar{A}\bar{C} + B\bar{C} + \bar{A}B$ (B) $A\bar{C} + \bar{B}C + \bar{A}B$
 (C) $\bar{A}C + \bar{B}C + \bar{A}B$ (D) $A\bar{C} + \bar{B}C + A\bar{B}$

- Q.6** Which of the following functions implements the Karnaugh map shown below?

$\begin{matrix} CD \\ \backslash \\ AB \end{matrix}$	00	01	11	10
00	0	0	1	0
01	X	X	1	X
11	0	1	1	0
10	0	1	1	0

(A) $\bar{A}B + CD$ (B) $D(C + A)$
 (C) $AD + \bar{A}B$
 (D) $(C + D)(\bar{C} + D)(A + B)$

- Q.7** Which function does NOT implement the Karnaugh map given below?

wz →	00	01	11	10
xy ↓				
00	0	x	0	0
01	0	x	1	1
11	1	1	1	1
10	0	x	0	0

(A) $(w+x)y$ (B) $x'y + yw$
 (C) $(w+x)(\bar{w}+y)(\bar{x}+y)$
 (D) None of the above

- Q.8** Minimum SOP for $f(w, x, y, z)$ shown in Karnaugh – map below is

$\begin{matrix} wx \\ \backslash \\ yz \end{matrix}$	00	01	11	10
00	0	1	1	0
01	x	0	0	1
11	x	0	0	1
10	0	1	1	x

(A) $xz + y'z$ (B) $xz' + zx'$
 (C) $x'y + zx'$ (D) None

- Q.9** The Karnaugh map for a four variable Boolean function is given below. The correct Boolean sum of product is

	PQ	00	01	11	10
RS		0	0	0	0
00		1	0	0	1
01		1	0	0	1
11		0	1	0	0
10		0	1	0	0

(A) $PQRS + \bar{Q}S$ (B) $\bar{P}QRS + \bar{Q}S$
 (C) $PQR + Q\bar{S}$ (D) $PQRS + \bar{Q}$

- Q.10** The switching expression corresponding to $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$ is

(A) $BC'D' + A'C'D + AB'D$
 (B) $ABC' + ACD + B'C'D$
 (C) $ACD' + A'BC' + AC'D'$
 (D) $A'BD + ACD' + BCD'$

- Q.11** Min-term (Sum of products) expression for a Boolean function is given as follows.

$$f(A, B, C) = \sum m(0, 1, 2, 3, 5, 6)$$

Where A is the MSB and C is the LSB. The minimized expression for the function is

(A) $A + (B \oplus C)$ (B) $(A \oplus B) + C$
 (C) $\bar{A} + (B \oplus C)$ (D) \overline{ABC}

- Q.12** The Boolean expression $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D}$ can be minimized to

(A) $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C} + A\bar{C}D$
 (B) $Y = \bar{A}\bar{B}\bar{C}D + BC\bar{D} + A\bar{B}\bar{C}D$
 (C) $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + A\bar{B}\bar{C}D$
 (D) $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$

- Q.13** The minimum sum of products form of the Boolean expression

$$y = \overline{P}\overline{Q}\overline{R}\overline{S} + \overline{P}\overline{Q}\overline{R}\bar{S} + P\overline{Q}\overline{R}\overline{S} + P\overline{Q}RS + P\overline{Q}R\bar{S} + \overline{P}\overline{Q}R\bar{S}$$

(A) $y = \overline{P}\overline{Q} + \overline{Q}\overline{S}$ (B) $y = \overline{P}\overline{Q} + \overline{Q}RS$
 (C) $y = P\overline{Q} + \overline{Q}\overline{R}\overline{S}$ (D) $y = \overline{Q}\overline{S} + P\overline{Q}R$

**Statement for Linked Answer
Questions 14 & 15**

The following Karnaugh map represents a function F

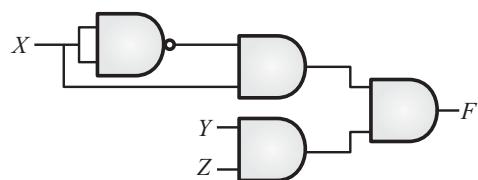
		X	YZ	00	01	11	10
		0	1	1	1	0	
		1	0	0	1	0	

Q.14 A minimized form of the function F is

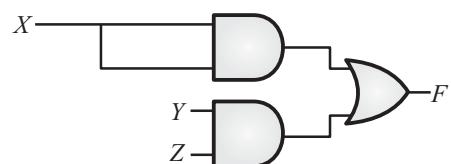
- (A) $F = \bar{X}Y + YZ$ (B) $F = \bar{X}\bar{Y} + YZ$
 (C) $F = \bar{X}\bar{Y} + Y\bar{Z}$ (D) $F = \bar{X}Y + \bar{Y}Z$

Q.15 Which of the following circuits is a realization of the above functions F ?

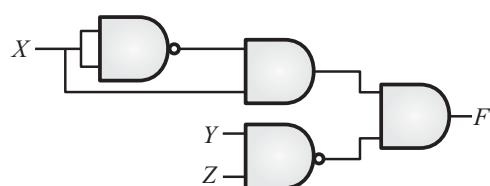
(A)



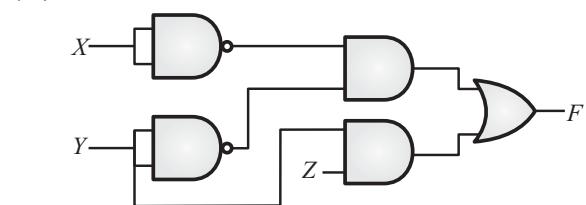
(B)



(C)



(D)



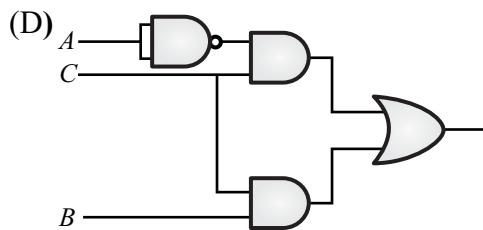
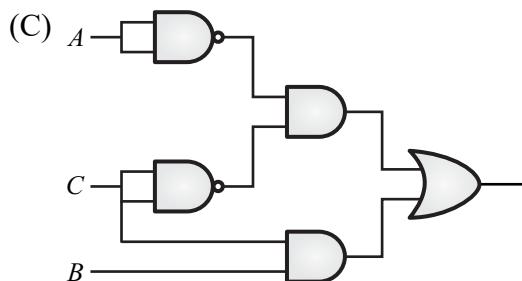
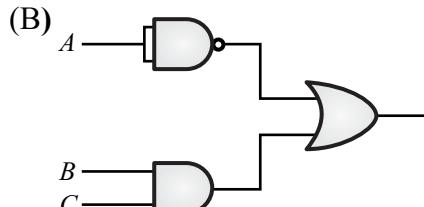
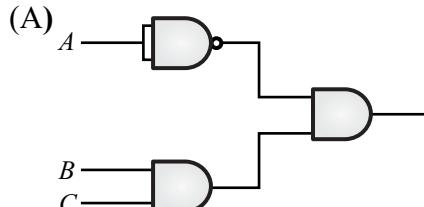
Q.16 What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term.

		ab	00	01	11	10
		cd	00	X	X	1
		01	X			1
		11				
		10	1			X

- (A) $\bar{b}\bar{d}$ (B) $\bar{b}\bar{d} + \bar{b}\bar{c}$
 (C) $\bar{b}\bar{d} + ab\bar{c}d$ (D) $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

Q.17 Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure

		AB	00	01	11	10
		C	0	1	1	
		1		1	1	



Q.18 The total number of prime implicants of the function $f(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 10)$ is _____.

- Q.19** Which one of the following gives the simplified sum of products expression for the Boolean function

$$F = m_0 + m_2 + m_3 + m_5$$

where, m_0, m_2, m_3 and m_5 are minterms corresponding to the inputs A, B and C with A as the MSB and C as the LSB?

- (A) $\bar{A}\bar{B} + \bar{A}\bar{B}\bar{C} + A\bar{B}C$
 (B) $\bar{A}\bar{C} + \bar{A}\bar{B} + A\bar{B}C$
 (C) $\bar{A}\bar{C} + A\bar{B} + A\bar{B}C$
 (D) $\bar{A}BC + \bar{A}\bar{C} + A\bar{B}C$

- Q.20** Given

$$f(w, x, y, z) = \sum_m (0, 1, 2, 3, 7, 8, 10) + \sum_d (5, 6, 11, 15)$$

where d represents the don't-care condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w, x, y, z)$?

- (A) $f = (\bar{w} + \bar{z})(\bar{x} + z)$
 (B) $f = (\bar{w} + z)(x + z)$
 (C) $f = (w + z)(\bar{x} + z)$
 (D) $f = (w + \bar{z})(\bar{x} + z)$

- Q.21** The Boolean expression equivalent to $ABC + A\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$ is

- (A) $A\bar{C} + BC$ (B) $AB + A\bar{C}$
 (C) $AB + B\bar{C}$ (D) $AC + B\bar{C}$

- Q.22** A Boolean function is given by $\Sigma m(0, 1, 2, 4, 5, 7)$, the number essential prime implicants is

- (A) 2 (B) 3
 (C) 4 (D) 5

- Q.23** Find the number of Prime implicants and Essential prime implicants in the given K-map.

		RS			
		00	01	11	10
PQ	00	1			
	01		1		1
11	1				
10		1			1

- (A) 4.5 (B) 0.6
 (C) 6.0 (D) 6.6

- Q.24** The simplified form of SOP form $f(PQRS) = \sum m(0, 1, 2, 3, 5, 8, 10, 11, 13, 15) + d(4, 6, 7, 12, 14)$ is

- (A) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
 (B) $\bar{P} + Q + R + \bar{S}$
 (C) $P + Q + R + S$
 (D) $P + \bar{Q} + \bar{R} + S$

- Q.25** What is the minimized expression of given

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5) + \sum d(10, 11, 12, 13, 14, 15)$$

- (A) $\bar{A} + \bar{B}\bar{C}$ (B) $A + BC$
 (C) $\bar{A}(\bar{B} + \bar{C})$ (D) $A(B + C)$

- Q.26** A function is represented by

$$f(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$$

The number of prime implicant and essential prime implicant are respectively

- (A) 4 and 3 (B) 4 and 4
 (C) 4 and 2 (D) 2 and 2



Answer Keys

Classroom Practice Questions									
1.	B	2.	D	3.	B	4.	A	5.	A
6.	D	7.	A	8.	A	9.	B	10.	A
11.	C	12.	1	13.	A	14.	A	15.	A
16.	B	17.	B	18.	A	19.	D	20.	A
21.	C	22.	D	23.	D	24.	D	25.	1
26.	B	27.	4	28.	A	29.	3	30.	A
31.	D	32.	D	33.	B	34.	3	35.	3
Self-Practice Questions									
1.	*	2.	C	3.	C	4.	B	5.	A
6.	B	7.	D	8.	B	9.	B	10.	A
11.	C	12.	D	13.	A	14.	B	15.	D
16.	B	17.	C	18.	3	19.	B	20.	A
21.	D	22.	B	23.	D	24.	B	25.	C
26.	C								

*1. $f = (\bar{B} + C)(\bar{A} + B)(A + \bar{C})$

4

Number System, Binary Codes & Complement Form

Classroom Practice Questions :

Number System and Binary Codes

- Q.1** The decimal equivalent of binary number 10110.11 is
(A) 16.75 (B) 20.75
(C) 16.50 (D) 22.75
- Q.2** Hexadecimal conversion of decimal number 227 will be
(A) A3 (B) E3
(C) CC (D) C3
- Q.3** The octal equivalent of HEX number AB·CD is
(A) 253.314 (B) 253.632
(C) 526.314 (D) 526.632
- Q.4** The number of digit 1 present in the binary representation of $3 \times 512 + 7 \times 64 + 5 \times 8 + 3$ is _____.
- Q.5** How many 1's are present in the binary Representation of $(4 \times 1096) + (9 \times 256) + (7 \times 16) + 5$?
_____.
- Q.6** If $(2.3)_{\text{base}4} + (1.2)_{\text{base}4} = (y)_{\text{base}4}$; What is the value of y? _____.
- Q.7** Given $(135)_{\text{base}x} + (144)_{\text{base}x} = (323)_{\text{base}x}$. What is the value of base x? _____.
- Q.8** The base of the number system for the addition operation $24 + 14 = 41$ is _____.
[GATE 2011, IIT Madras]

- Q.9** When $\sqrt{(224)_r} = (13)_r$, what is the value of the radix r ? _____.
- Q.10** Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____.
[GATE 2011, IIT Madras]
- Q.11** Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____.
[GATE 2015, IIT Kanpur]
- Q.12** Decimal 43 in Hexadecimal and BCD number system is respectively
[GATE 2005, IIT Bombay]
(A) B2, 01000011 (B) 2B, 01000011
(C) 2B, 0011 0100 (D) B2, 01000100
- Q.13** Which of the following is an invalid state in 8 4 2 1 Binary Coded Decimal counter
[GATE 2014, IIT Kharagpur]
(A) 1000 (B) 1001
(C) 0011 (D) 1100
- Q.14** A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this numbering system, the BCP code 100010011001 corresponds to the following number in base-5 system
[GATE 2006, IIT Kharagpur]

- (A) 423 (B) 1324
 (C) 2201 (D) 4231

Q.15 The base (or radix) of the number system such that the following equation holds is

$$\frac{312}{20} = 13.1.$$

[GATE 2014, IIT Kharagpur]

Complement Form

Q.1 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

[GATE 2004, IIT Madras]

- (A) 25, 9 and 57 respectively.
 (B) -6, -6 and -6 respectively.
 (C) -7, -7 and -7 respectively.
 (D) -25, -9 and -57 respectively.

Q.2 A number in 4-bit two's complement representation is $X_3 X_2 X_1 X_0$. This number when stored using 8 – bits will be

[GATE 1999, IIT Bombay]

- (A) $0000X_3 X_2 X_1 X_0$
 (B) $1111X_3 X_2 X_1 X_0$
 (C) $X_3 X_2 X_1 X_0 X_3 X_2 X_1 X_0$
 (D) $\overline{X}_3 \overline{X}_2 \overline{X}_1 \overline{X}_0 X_3 X_2 X_1 X_0$

Q.3 A number N is stored in a 4-bit 2's complement representation as

a_3	a_2	a_1	a_0
-------	-------	-------	-------

It is copied into a 6-bit register and after a few operations the final bit pattern is

a_3	a_2	a_1	a_0	1
-------	-------	-------	-------	---

The value of the bit pattern in 2's complement representation is given terms of the original number is N as

[GATE 2006, IIT Kharagpur]

- (A) $32a_3 + 2N + 1$ (B) $32a_3 - 2N + 1$
 (C) $2N - 1$ (D) $2N + 1$

Q.4 Let $A = 1111\ 1010$ and $B = 0000\ 1010$ be two 8 – bit 2's complement numbers. Their product in 2's complement is

[GATE 2004, IIT Madras]

- (A) 1100 0100 (B) 1001 1100
 (C) 1010 0101 (D) 1101 0101

Q.5 Assuming all numbers are in 2's complement representation, which of the following numbers is divisible by 11111011? [GATE 2003, IIT Madras]

- (A) 11100111 (B) 11100100
 (C) 11010111 (D) 11011011

Q.6 An 8085 microprocessor executes the following instructions :

Two numbers are represented in signed 2's complement form as

$$P = 11101101 \text{ and } Q = 11100110$$

If Q is subtracted from P , the value obtained in signed 2's complement form is

- (A) 100000111 (B) 00000111
 (C) 11111001 (D) 011111001

Q.7 The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is

[GATE 2016, IISc Bangalore]

Q.8 Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation. Then $X - Y$ is _____

[GATE 2016, IISc Bangalore]

Q.9 Two 2's complement numbers having sign bits 'x' and 'y' are added and the sign bit of the result is 'z'. Then, the occurrence of overflow is indicated by the Boolean function [GATE 1998, IIT Delhi]

- (A) $x y z$ (B) $\overline{x} \overline{y} \overline{z}$
 (C) $\overline{x} \overline{y} z + x y \overline{z}$ (D) $xy + yz + zx$

Q.10 When two 8-bit numbers $A_7.....A_0$ and $B_7.....B_0$ in 2's complement

representation (with A_0 and B_0 as the least significant bits) are added using a ripple-carry adder, the sum bits obtained are $S_7.....S_0$ and the carry bits are $C_7.....C_0$. An overflow is said to have occurred if [GATE 2017, IIT Roorkee]

- (A) The carry bit C_7 is 1
- (B) All the carry bits ($C_7.....C_0$) are 1
- (C) $(A_7.B_7.\bar{S}_7 + \bar{A}_7.B_7.S_7)$ is 1
- (D) $(A_0.B_0.\bar{S}_0 + \bar{A}_0.B_0.S_0)$ is 1

Q.11 Assuming all numbers in 2's complement form, which of the following additions will result in overflow?

- (A) $1100 + 1100$
- (B) $0011 + 0111$
- (C) $1111 + 0111$
- (D) All of the above

Q.12 Consider three registers R1, R2, and R3 that store numbers in IEEE-754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0×42200000 and $0\times C1200000$,

respectively. If $R3 = \frac{R1}{R2}$, what is the value stored in R3? [GATE 2020, IIT Delhi]

- (A) 0×40800000
- (B) $0\times C0800000$
- (C) 0×83400000
- (D) $0\times C8500000$

Q.13 P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of 8^*P is [GATE 2010, IIT Guwahati]

- (A) $(C3D8)_{16}$
- (B) $(187B)_{16}$
- (C) $(F878)_{16}$
- (D) $(987B)_{16}$

Q.14 The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in [GATE 2006, IIT Kharagpur]

- (A) 0001 and an overflow
- (B) 1001 and no overflow
- (C) 0001 and no overflow
- (D) 1001 and an overflow

Q.15 Consider the unsigned 8-bit fixed point binary number representation below,

$$b_7\ b_6, b_5, b_4, b_3.b_2\ b_1\ b_0$$

Where the position of the binary point is between b_3 and b_2 . Assume b_7 is the most significant bit. Some of the decimal numbers listed cannot be represented exactly in the above representation :

- (i) 31.500
- (ii) 0.875
- (iii) 12.100
- (iv) 3.001

Which one of the following statements is true? [GATE 2018, IIT Guwahati]

- (A) None of (i), (ii), (iii), (iv) can be exactly represented
- (B) Only (ii) cannot be exactly represented
- (C) Only (iii) and (iv) cannot be exactly represented
- (D) Only (i) and (ii) cannot be exactly represented

Self-Practice Questions :

Q.1 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is

- (A) 0
- (B) 1
- (C) 32,767
- (D) 65,535

Q.2 The result of $(45)_{10} - (45)_{16}$ expressed in 2's complement representation is

- (A) 011000
- (B) 100111
- (C) 101000
- (D) 101001

Q.3 A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should

- (A) copy the original byte to the less significant byte of the word and fill the more significant byte with zeros.
- (B) copy the original byte to the more significant byte of the word and fill the less significant byte with zeros.

- (C) copy the original byte to the less significant byte of the word and make each bit of the more significant byte equal to the most significant bit of the original byte.
- (D) copy the original byte to the less significant bytes well as the more significant byte of the word.
- Q.4** Zero has two representations in :
- (A) Sign magnitude
(B) 1's complement
(C) 2's complement
(D) None of the above
- Q.5** The number 43 in 2's complement representation is
- (A) 01010101 (B) 11010101
(C) 00101011 (D) 10101011
- Q.6** The 2's complement representation of -17 is
- (A) 101110 (B) 101111
(C) 111110 (D) 110001
- Q.7** 4-bit 2's complement representation of a decimal number is 1000. The number is
- (A) +8 (B) 0
(C) -7 (D) -8
- Q.8** The 2's complement representation of the decimal value -15 is
- (A) 1111 (B) 11111
(D) 111111 (C) 10001
- Q.9** The range of signed decimal numbers that can be represented by 6-bit 1's complement number is
- (A) -31 to +31 (B) -63 to +63
(C) -64 to +63 (D) -32 to +31
- Q.10** If 73_x (in base - x number system) is equal to 54_y (in base - y number system), the possible values of x and y are
- (A) 8, 16 (B) 10, 12
(C) 9, 13 (D) 8, 11
- Q.11** An 8-bit 2's complement representation of an integer is FA (Hex). Its decimal equivalent is
- (A) -10 (B) -6
(C) +6 (D) +10
- Q.12** The range of integers that can be represented by an n bit 2's complement number system is
- (A) -2^{n-1} to $(2^{n-1} - 1)$
(B) $-(2^{n-1} - 1)$ to $(2^{n-1} - 1)$
(C) -2^{n-1} to 2^{n-1}
(D) $-(2^{n-1} + 1)$ to $(2^{n-1} - 1)$
- Q.13** The hexadecimal representation of 657_8 is
- (A) IAF (B) D78
(C) D71 (D) 32F
- Q.14** The binary representation of the decimal number 1.375 is
- (A) 1.111 (B) 1.010
(C) 1.011 (D) 1.001
- Q.15** $(1217)_8$ is equivalent to
- (A) $(1217)_{16}$ (B) $(028F)_{16}$
(C) $(2297)_{10}$ (D) $(0B17)_{16}$
- Q.16** The smallest integer that can be represented by an 8 - bit number in 2's complement form is
- (A) -256 (B) -128
(C) -127 (D) 0
- Q.17** The representation of the decimal number $(27.625)_{10}$ in base-2 number system is
- (A) 11011.110 (B) 11101.101
(C) 11011.101 (D) 10111.110
- Q.18** The number of 1 in 8-bits representation of -127 in 2's complement form is m and that in 1's complement form is n. What is the value of m:n?
- (A) 2 : 1 (B) 1 : 2
(C) 3 : 1 (D) 1 : 3
- Q.19** A gray code is a/an :
- (A) Binary weighted code
(B) Arithmetic code
(C) Code which exhibits a single bit change between two successive codes
(D) Alphanumeric code

- Q.20** Which of the following is a self-complementing code ?
 (A) 8421 code (B) Excess 3 code
 (C) Pure binary code (D) Gray code
- Q.21** If $(11X1Y)_8 = (12C9)_{16}$ then the values X and Y are
 (A) 5 and 1 (B) 5 and 7
 (C) 7 and 5 (D) 1 and 5
- Q.22** What are the values respectively of R_1 and R_2 in the expression $(235)_{R_1} = (565)_{10} = (865)_{R_2}$?
 (A) 8, 16 (B) 16, 8
 (C) 6, 16 (D) 12, 8
- Q.23** Consider the following multiplication :
 $(10w1z)_2 \times (15)_{10} = (y01011001)_2$
 Which one of the following gives appropriate values of w, y and z?
 (A) w = 0, y = 0, z = 1
 (B) w = 0, y = 1, z = 1
 (C) w = 1, y = 1, z = 1
 (D) w = 1, y = 1, z = 0
- Q.24** The maximum positive and negative numbers that can be represented in 1's complement using n-bits are respectively
 (A) $+(2^{n-1} - 1)$ and $-(2^{n-1} - 1)$
 (B) $+(2^{n-1} - 1)$ and $-(2^{n-1})$
 (C) $+(2^{n-1})$ and $-(2^{n-1} - 1)$
 (D) $+(2^{n-1} + 1)$ and $-(2^{n-1})$
- Q.25** The maximum positive and negative number that can be represented in 2's complement using n-bits are respectively
 (A) $+(2^{n-1} - 1)$ and $-(2^{n-1} - 1)$
 (B) $+(2^{n-1} - 1)$ and $-(2^{n-1})$
 (C) $+(2^{n-1})$ and $-(2^{n-1} - 1)$
 (D) $+(2^{n-1} + 1)$ and $-(2^{n-1})$
- Q.26** The range of numbers that can be represented in 2's complement mode with four binary digits is
- Q.27** 2's complement number is 1001. Its equivalent representation in 8 bit format is _____.
 (A) 00001001 (B) 10011001
 (C) 11111001 (D) None
- Q.28** The range of signed decimal numbers that can be represented by 8 bit 1's complement number is _____.
 (A) -127 to +127 (B) -128 to +128
 (C) -256 to +256 (C) -256 to +127
- Q.29** $(98)_{10} + (1D)_{16} + (72)_8 + (1011)_2 =$
 (A) $(314)_8$ (B) $(B4)_{16}$
 (C) $(194)_{10}$ (D) None of these
- Q.30** If $(212)_x = (153)_8$ then the base x is _____.
Q.31 The minimum of bits required to represent -32 in 2's complement representation is _____.
Q.32 The 2's complement representation of $(-89)_{10}$ is
 (A) 10100110 (B) 01011101
 (C) 10100010 (D) 10100111
- Q.33** The two numbers represented in signed 2's complement form are $A = 11101001$ and $B = 11100101$. If B is subtracted from A, the value obtained in signed 2's complement form is
 (A) 11111001 (B) 00000100
 (C) 11000100 (D) 10000100
- Q.34** A number system is represented by $(54)_b = (13)_b \times (4)_b$ the base of the number is _____.
Q.35 The addition of 4 bit two's complement binary number 1111 and 0010 results
 (A) 0001 and an overflow
 (B) 1001 and no overflow
 (C) 0001 and no overflow
 (D) 1001 and an overflow

- Q.36** The addition of two number 24 and 13, in base 5 is _____.
- Q.37** The base of the number system for the addition $34+14=103$ is _____.
- Q.38** Convert given hexadecimal code into octal code $(CAF8)_{16}$?

❖❖❖❖

Answer Keys

Classroom Practice Questions									
Number System and Binary Codes									
1.	D	2.	B	3.	*	4.	9	5.	8
6.	10.1	7.	6	8.	7	9.	5	10.	3
11.	5	12.	B	13.	D	14.	D	15.	5
Complement Form									
1.	C	2.	C	3.	D	4.	A	5.	A
6.	B	7.	-11	8.	1	9.	C	10.	C
11.	B	12	B	13.	A	14.	C	15.	C
Self-Practice Questions									
1.	B	2.	C	3.	C	4.	A, B	5.	C
6.	B	7.	D	8.	D	9.	A	10.	D
11.	B	12.	A	13.	A	14.	C	15.	B
16.	B	17.	C	18.	A	19.	C	20.	B
21.	*	22.	B	23.	C	24.	A	25.	B
26.	C	27.	C	28.	A	29.	D	30.	7
31.	6	32.	D	33.	B	34.	8	35.	C
36.	42	37.	5	38.	$(145373)_8$				

5

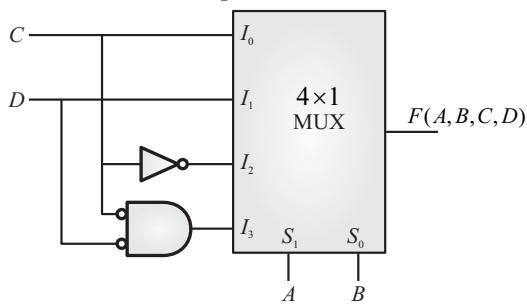
Combinational Circuits

Classroom Practice Questions :

Multiplexer :

Q.1 The Boolean function realized by the logic circuit shown is

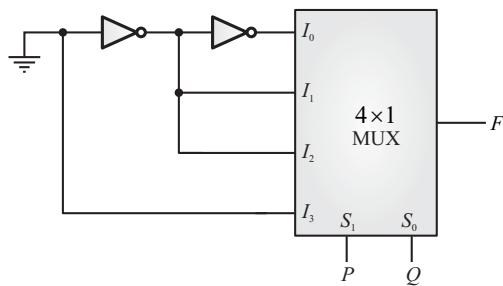
[GATE 2010, IIT Guwahati]



- (A) $F = \sum m(0, 1, 3, 5, 9, 10, 14)$
- (B) $F = \sum m(2, 3, 5, 7, 8, 12, 13)$
- (C) $F = \sum m(1, 2, 4, 5, 11, 14, 15)$
- (D) $F = \sum m(2, 3, 5, 7, 8, 9, 12)$

Q.2 The logic function implemented by the circuit below is (ground implies a logic “0”)

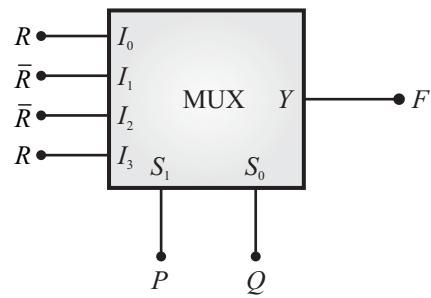
[GATE 2011, IIT Madras]



- (A) $F = \text{AND}(P, Q)$
- (B) $F = \text{OR}(P, Q)$
- (C) $F = \text{XNOR}(P, Q)$
- (D) $F = \text{XOR}(P, Q)$

Q.3 The output F of the multiplexer circuit shown below expressed in terms of the input P, Q and R is

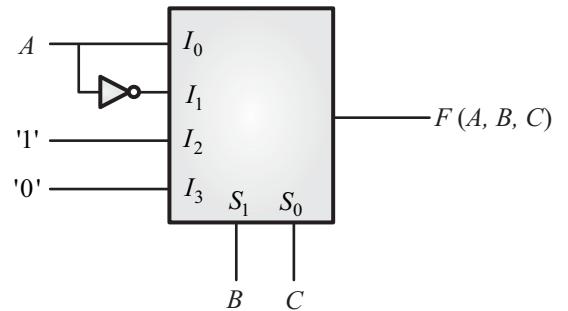
[GATE 2008, IISc Bangalore]



- (A) $F = P \oplus Q \oplus R$
- (B) $F = PQ + QR + RP$
- (C) $F = (P \oplus Q)R$
- (D) $F = (P \oplus Q)\bar{R}$

Q.4 A 4×1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean functions $F(A, B, C)$ implemented is

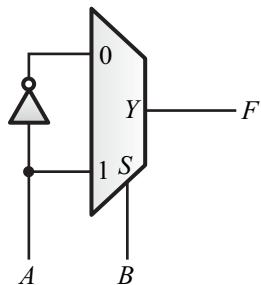
[GATE 2006, IIT Kharagpur]



- (A) $F(A, B, C) = \sum(1, 2, 4, 6)$
- (B) $F(A, B, C) = \sum(1, 2, 6)$
- (C) $F(A, B, C) = \sum(2, 4, 5, 6)$
- (D) $F(A, B, C) = \sum(1, 5, 6)$

- Q.5** Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is

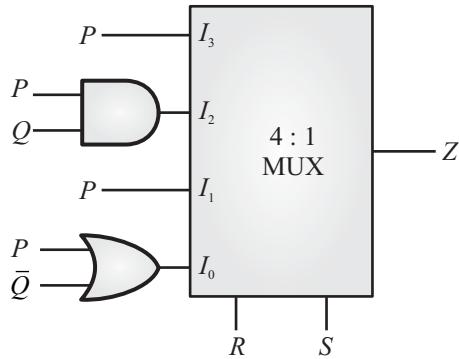
[GATE 2016, IISc Bangalore]



- (A) $A \oplus B$ (B) $\overline{A+B}$
 (C) $A+B$ (D) $\overline{A \oplus B}$

- Q.6** For the circuit shown in the following figure, $I_0 - I_3$ are inputs to the 4 : 1 multiplexer. R (MSB) and S are control bits.

[GATE 2008, IISc Bangalore]

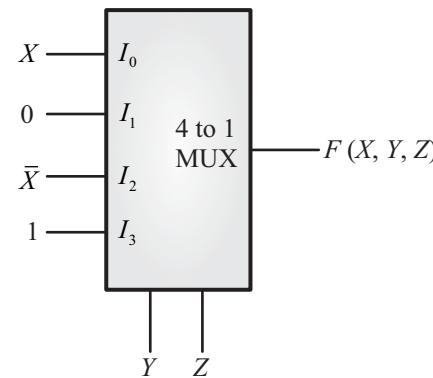


The output Z can be represented by,

- (A) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$
 (B) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
 (C) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
 (D) $PQ\bar{R} + PQRS + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$

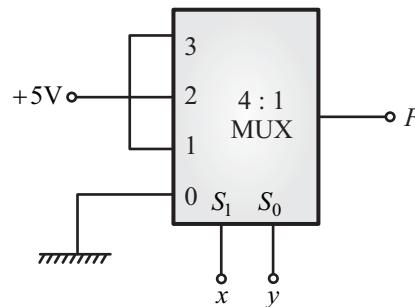
- Q.7** A 4 to 1 multiplexer to realize a Boolean function $F(X, Y, Z)$ is shown in the figure blow. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for $F(X, Y, Z)$ is

[GATE 2016, IISc Bangalore]



- (A) $\sum m(2, 3, 4, 7)$ (B) $\sum m(1, 3, 5, 7)$
 (C) $\sum m(0, 2, 4, 6)$ (D) $\sum m(2, 3, 5, 6)$

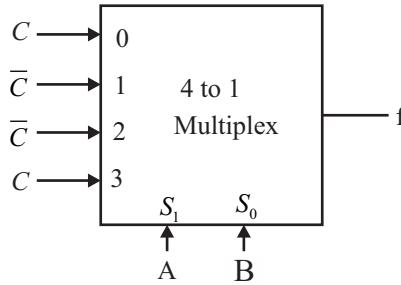
- Q.8** The output F of the 4 to 1 MUX shown in figure is [GATE 2001, IIT Kanpur]



- (A) $\overline{x\bar{y}} + x$ (B) $x + y$
 (C) $\bar{x} + \bar{y}$ (D) $xy + \bar{x}$

- Q.9** Consider the circuit in figure shown. It implements

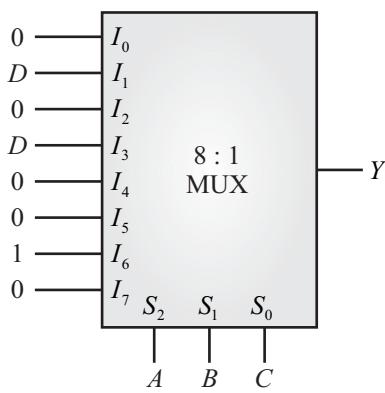
[GATE 1996, IISc Bangalore]



- (A) $\overline{ABC} + \overline{ABC} + ABC$
 (B) $A + B + C$
 (C) $A \oplus B \oplus C$
 (C) $AB + BC + CA$

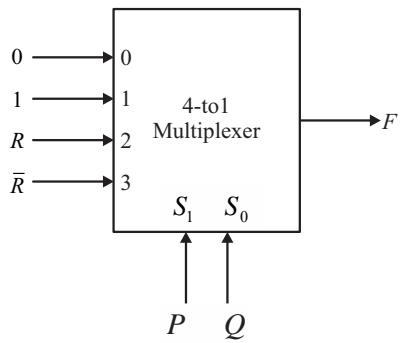
- Q.10** An 8 to 1 multiplexer is used to implement a logical function Y as shown in the figure. The output Y is given by

[GATE 2014, IIT Kharagpur]



- (A) $Y = A\bar{B}C + A\bar{C}D$
 (B) $Y = \bar{A}BC + A\bar{B}D$
 (C) $Y = AB\bar{C} + \bar{A}CD$
 (D) $Y = \bar{A}\bar{B}C + A\bar{B}C$

Q.11 Consider the 4-to-1 multiplexer with two select lines S_1 and S_0 given below



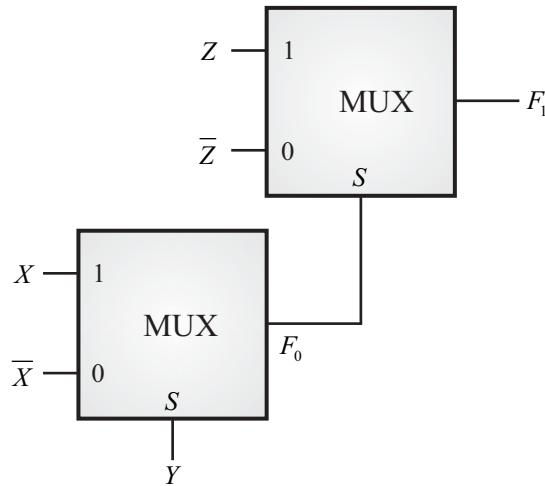
The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

[GATE 2014, IIT Kharagpur]

- (A) $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
 (B) $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
 (C) $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$
 (D) PQR

Q.12 A MUX circuit shown in the figure below implements a logic function. The correct expression for F_1 is

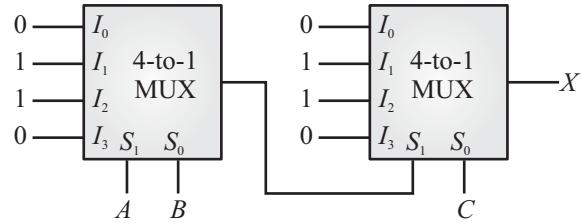
[GATE 2007, IIT Kanpur]



- (A) $(\bar{X} \oplus Y) \oplus Z$
 (B) $(\bar{X} \oplus Y) \oplus \bar{Z}$
 (C) $(X \oplus Y) \oplus \bar{Z}$
 (D) $(X \oplus Y) \oplus Z$

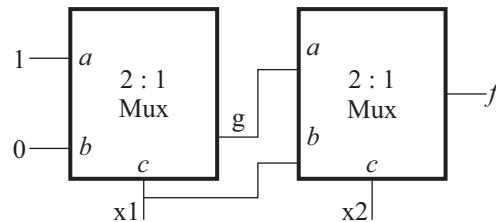
Q.13 In the following circuit, X is given by

[GATE 2007, IIT Kanpur]



- (A) $X = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$
 (B) $X = \bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$
 (C) $X = AB + BC + AC$
 (D) $X = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

Q.14 Consider the circuit shown below. The output of a 2: 1 Mux is given by the function $(ac' + bc)$.

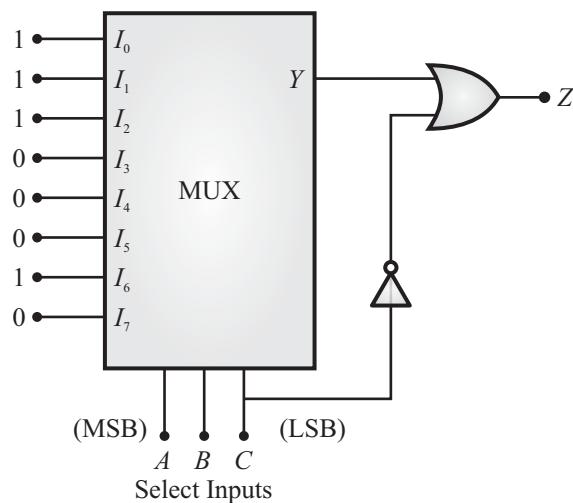


Which of the following is true?

[GATE 2001, IIT Kanpur]

- (A) $f = x_1' + x_2$
 (B) $f = x_1' x_2 + x_1 x_2'$
 (C) $f = x_1 x_2 + x_1' x_2'$
 (D) $f = x_1 + x_2'$

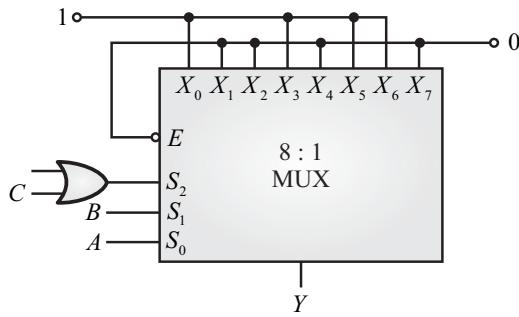
- Q.15** A combinational circuit using an 8 to 1 multiplexer is shown in the following figure. The minimized expression for the output (Z) is [GATE 2006, IIT Kharagpur]



- (A) $C(\bar{A} + \bar{B})$ (B) $C(A + B)$
 (C) $\bar{C} + \bar{A}\bar{B}$ (D) $\bar{C} + AB$

- Q.16** In the TTL circuit shown, S_2 to S_0 are selection lines and X_7 to X_0 input lines. S_0 and X_0 are LSBs. The output Y is

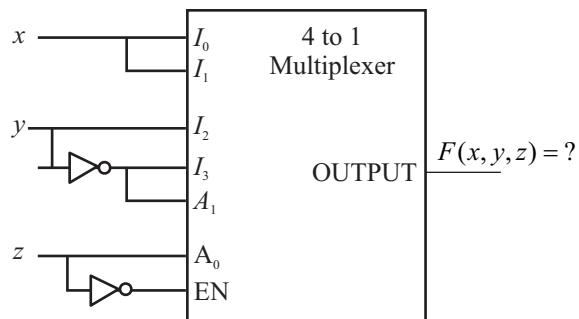
[GATE 2001, IIT Kanpur]



- (A) Indeterminate
 (B) $A \oplus B$
 (C) $A \odot B$
 (D) $\bar{C}(A \oplus B) + C(A \oplus B)$

- Q.17** Consider the following multiplexer where I_0, I_1, I_2, I_3 , are four data input lines selected by two address line combinations $A_1 A_0 = 00, 01, 10, 11$ respectively and f is the output of the multiplex (or). EN is the Enable input.

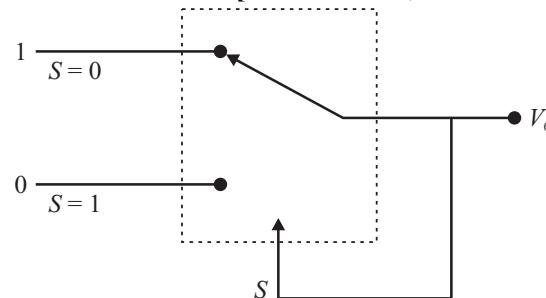
[GATE 2002, IISc Bangalore]



The function $f(x, y, z)$ implemented by the above circuit is

- (A) $xy\bar{z}$ (B) $xy + z$
 (C) $x + y$ (D) None of the above

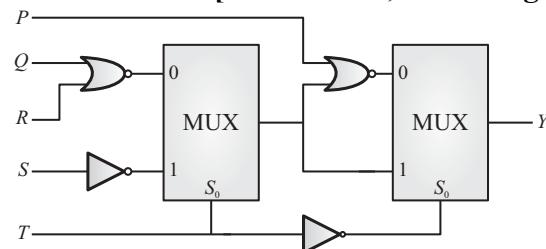
- Q.18** A 2-to-1 digital multiplexer having a switching delay of 1 μs is connected as shown in figure. The output of the multiplexer is tied to its own select input S . The inputs which gets selected when $S = 0$ is tied to 1 and the input that goes selected when $S = 1$ is tied to 0. The output V_0 will be [GATE 2003, IIT Madras]



- (A) 0 (B) 1
 (C) pulse train of frequency 0.5 MHz
 (D) pulse train of frequency 1.0 MHz

- Q.19** For the circuit shown in the figure, the delays of NOR gates, multiplexers and inverters are 2 ns, 1.5 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.

[GATE 2016, IISc Bangalore]



- Q.20** What are the minimum number of 2 to 1 multiplexers required to generate a 2-input AND gate and a 2-input EX-OR gate?

[GATE 2009, IIT Kanpur]

- | | |
|-------------|-------------|
| (A) 1 and 2 | (B) 1 and 3 |
| (C) 1 and 1 | (D) 2 and 2 |

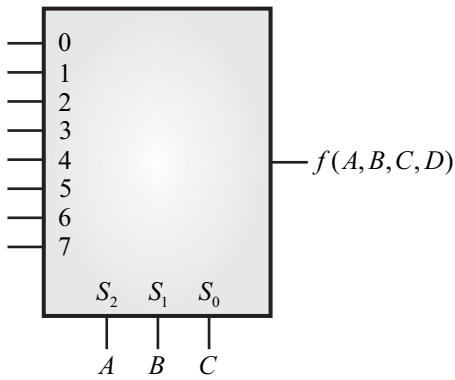
- Q.21** Without any additional circuitry, an 8:1 MUX can be used to obtain

[GATE 2009, IIT Kanpur]

- (A) some but not all Boolean functions of 3 variables.
- (B) all functions of 3 variables but none of 4 variables.
- (C) all functions of 3 variables and some but not all of 4 variables.
- (D) all functions of 4 variables.

- Q.22** A Boolean function $f(A, B, C, D) = \prod M(1, 5, 12, 15)$ is to be implemented using an 8×1 multiplexer (A is MSB). The inputs ABC are connected to the select input $S_2 S_1 S_0$ of the multiplexer respectively. Which one of the following options gives the correct inputs to pins 0, 1, 2, 3, 4, 5, 6, 7 in order?

[GATE 2015, IIT Kanpur]



- (A) $D, 0, D, 0, 0, 0, \bar{D}, D$
- (B) $\bar{D}, 1, \bar{D}, 1, 1, 1, D, \bar{D}$
- (C) $D, 1, D, 1, 1, 1, \bar{D}, D$
- (D) $\bar{D}, 0, \bar{D}, 0, 0, 0, D, \bar{D}$

- Q.23** Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

[GATE 2007, IIT Kanpur]

- (A) 2^n line to 1 line
- (B) 2^{n+1} line to 1 line
- (C) 2^{n-1} line to 1 line
- (D) 2^{n-2} line to 1 line

- Q.24** Consider a multiplexer with X and Y as data inputs and Z as control input. If $z = 0$ selects input x , and $z = 1$ selects input Y . What are the connections required to realize the 2-variable Boolean function $f = T + R$ without using any additional Hardware?

[GATE 2004, IIT Delhi]

- (A) R to X , 1 to Y , T to Z
- (B) T to X , R to Y , T to Z
- (C) T to X , R to Y , O to Z
- (D) R to X , O to Y , T to Z

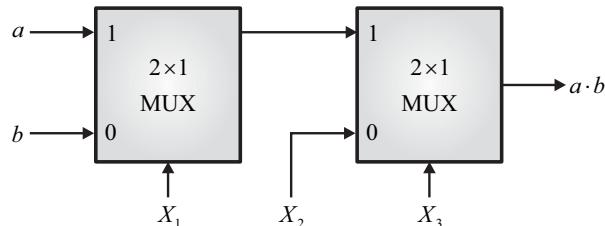
- Q.25** The minimum number of 2 to 1 multiplexers required to realize a 4 to 1 multiplexer is

[GATE 2004, IIT Delhi]

- (A) 1
- (B) 2
- (C) 3
- (D) 4

- Q.26** The following circuit implements a two-input AND gate using two 2×1 multiplexers.

[GATE 2007, IIT Kanpur]

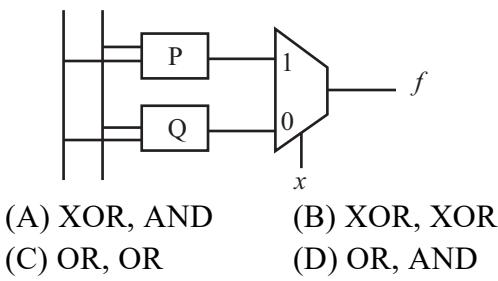


What are the values of X_1, X_2, X_3 ?

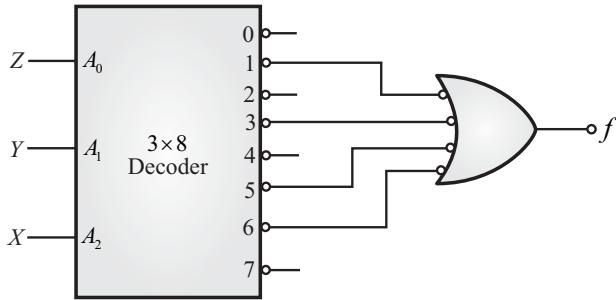
- (A) $X_1 = b, X_2 = 0, X_3 = a$
- (B) $X_1 = b, X_2 = 1, X_3 = b$
- (C) $X_1 = a, X_2 = b, X_3 = 1$
- (D) $X_1 = a, X_2 = 0, X_3 = b$

- Q.27** The majority function is a Boolean function $f(x, y, z)$ that takes the value 1 whenever a majority of the variables x, y, z and 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled P and Q are, respectively

[GATE 2006, IIT Kharagpur]

**Decoder :**

- Q.1** A 3 line to 8 line decoder, with active low outputs, is used to implement a 3 variable Boolean functions as shown in the figure.

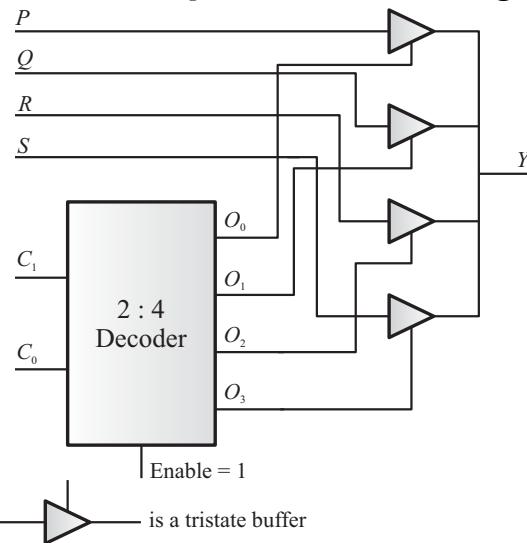


The simplified form of Boolean function $F(X,Y,Z)$ implemented in 'Product of Sum' form will be

[GATE 2008, IISc Bangalore]

- (A) $(X+Z)(\bar{X}+\bar{Y}+\bar{Z})(Y+Z)$
 (B) $(\bar{X}+\bar{Z})(X+Y+Z)(\bar{Y}+\bar{Z})$
 (C) $(\bar{X}+\bar{Y}+Z)(\bar{X}+Y+Z)$.
 $(X+\bar{Y}+Z)(X+Y+\bar{Z})$
 (D) $(\bar{X}+\bar{Y}+Z)(\bar{X}+Y+\bar{Z})$.
 $(X+\bar{Y}+Z)(X+\bar{Y}+\bar{Z})$

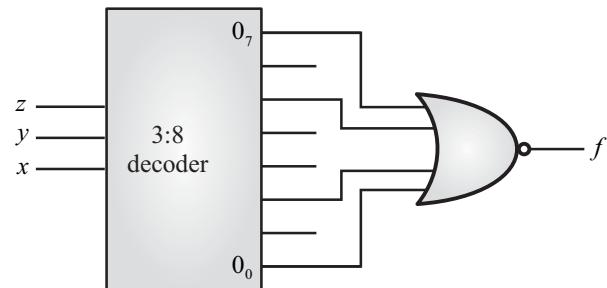
- Q.2** The functionality implemented by the circuit below is [GATE 2016, IISc Bangalore]



- (A) 2-to-1 multiplexer.
 (B) 4-to-1 multiplexer.
 (C) 7-to-1 multiplexer.
 (D) 6-to-1 multiplexer.

- Q.3** How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates? [GATE 2007, IIT Kanpur]
 (A) 7 (B) 8
 (C) 9 (D) 10

- Q.4** What Boolean function does the circuit below realize? [GATE 2008, IISc Bangalore]



- (A) $xz + \bar{x}\bar{z}$
 (B) $x\bar{z} + \bar{x}z$
 (C) $\bar{xy} + yz$
 (D) $xy + \bar{y}\bar{z}$

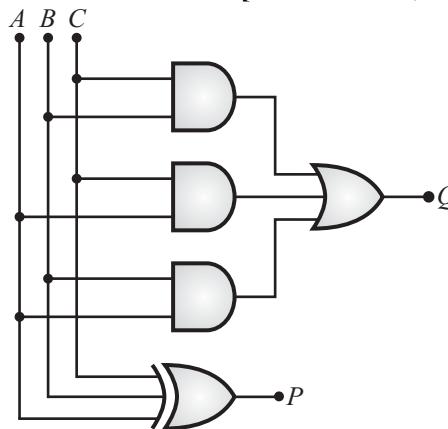
Adder :

- Q.1** In a half-subtractor circuit with X and Y as inputs, the Borrow (M) and Difference ($N = X - Y$) are given by

[GATE 2014, IIT Kharagpur]

- (A) $M = X \oplus Y$, $N = XY$
 (B) $M = XY$, $N = X \oplus Y$
 (C) $M = \bar{X}Y$, $N = X \oplus Y$
 (D) $M = X\bar{Y}$, $N = \overline{X \oplus Y}$

- Q.2** In the given circuit of figure, A , B and C are the inputs and P , Q are the two outputs. The circuit is a [GATE 2004, IIT Delhi]



- (A) Half adder where P is the sum and Q is the carry.
 (B) Half adder where P is the carry and Q is the sum.
 (C) Full adder where P is the sum and Q is the carry.
 (D) Full adder where P is the carry and Q is the sum.

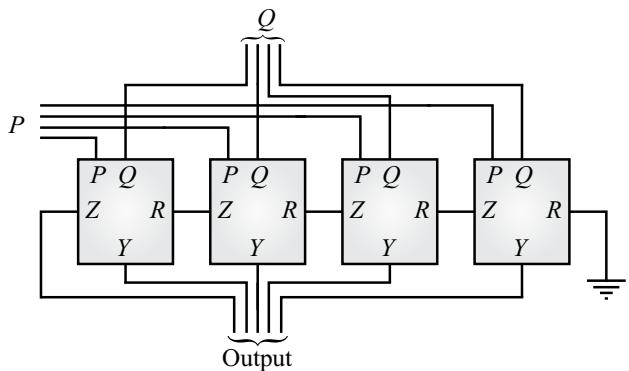
Q.3 The circuit shown in figure has 4 boxes each described by inputs P , Q , R and output Y , Z with

$$Y = P \oplus Q \oplus R$$

$$Z = RQ + R\bar{P} + Q\bar{P}$$

The circuit acts as a

[GATE 2003, IIT Madras]



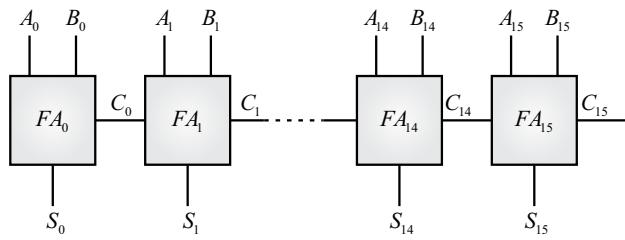
- (A) 4 bit adder giving $P + Q$
 (B) 4 bit subtractor giving $P - Q$
 (C) 4 bit subtractor giving $Q - P$
 (D) 4 bit adder giving $P + Q + R$

Q.4 A 1 bit full adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full adders are cascaded ?

- (A) 10^7 (B) 1.25×10^7
 (C) 6.25×10^6 (D) 10^5

Q.5 A 16 bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be _____.

[GATE 2016, IISc Bangalore]

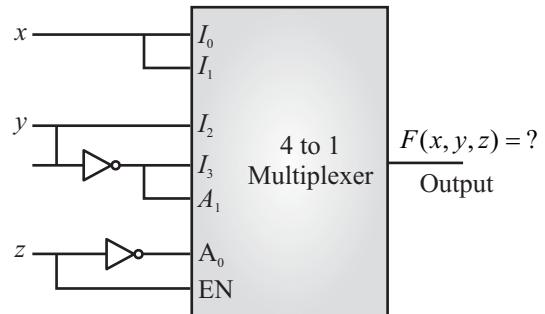


Q.6 A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple- carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

[GATE 2015, IIT Kanpur]

Q.7 Consider the following multiplexer where I_0, I_1, I_2, I_3 , are four data input lines selected by two address line combinations A_1 $A_0 = 00, 01, 10, 11$ respectively and f is the output of the multiplexer and EN is the Enable input.

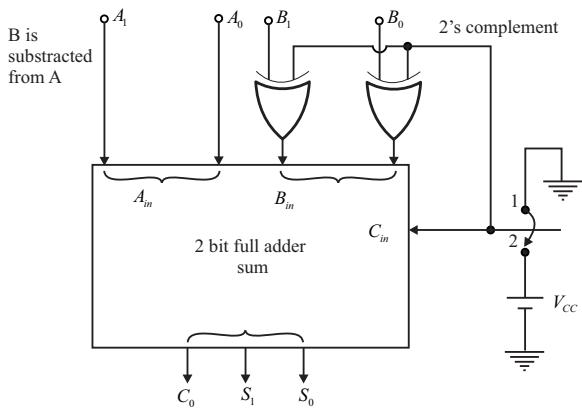
[GATE 2002, IISc Bangalore]



The function $f(x, y, z)$ implemented by the above circuit is

- (A) $xy\bar{z}$
 (B) $xy + z$
 (C) $x + y$
 (D) None of the above

Q.8 In the two bit full-adder/subtractor unit shown in figure, when the switch is in position 2, _____ using _____ arithmetic. [GATE 1990, IISc Bangalore]

**Code Converter :**

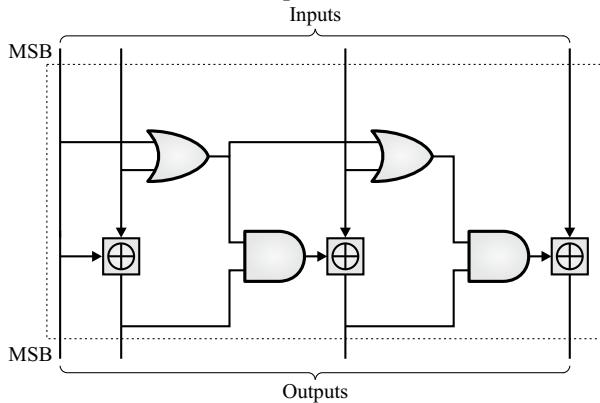
- Q.1** The minimal function that can detect a “divisible by 3” 8421 BCD code digit (representation is $D_8D_4D_2D_1$) is given by

[GATE 1990, IISc Bangalore]

- (A) $D_8D_1 + D_4D_2 + \bar{D}_8D_2D_1$
- (B) $D_8D_1 + D_4D_2\bar{D}_1 + \bar{D}_4D_2D_1 + \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1$
- (C) $D_8D_1 + D_4D_2 + \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1$
- (D) $D_4D_2\bar{D}_1 + D_4D_2D_1 + D_8\bar{D}_4D_2D_1$

- Q.3** The circuit shown in the figure converts

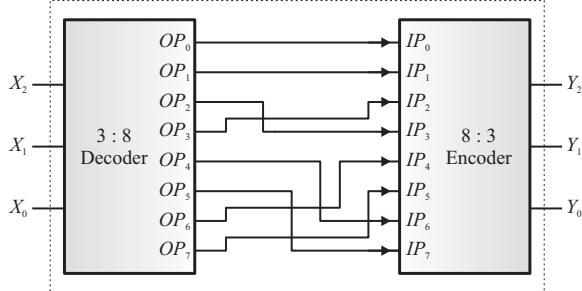
[GATE 2003, IIT Madras]



- (A) BCD to Binary code.
- (B) Binary to Excess -3 code.
- (C) Excess -3 to Gray code.
- (D) Gray to Binary code.

- Q.4** Identify the circuit below,

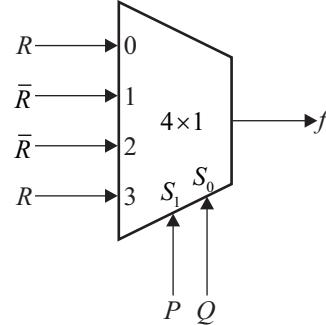
[GATE 2016, IISc Bangalore]



- (A) Binary to Gray code converter
- (B) Binary to XS3 converter
- (C) Gray to Binary converter
- (D) XS3 to Binary converter

Self-Practice Questions :

- Q.1** The Boolean expression for the output f of the multiplexer shown below is



- (A) $\overline{P \oplus Q \oplus R}$
- (B) $P \oplus Q \oplus R$
- (C) $P + Q + R$
- (D) $\overline{P + Q + R}$

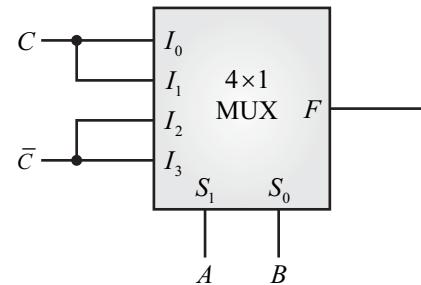
- Q.2** Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

- (A) XOR gates, NOT gates
- (B) 2 to 1 multiplexors
- (C) AND gates, XOR gates
- (D) Three – input gates that output $(A \cdot B) + C$ for the inputs A, B and C

- Q.3** The gray code equivalent of binary number $(1000001)_2$ is

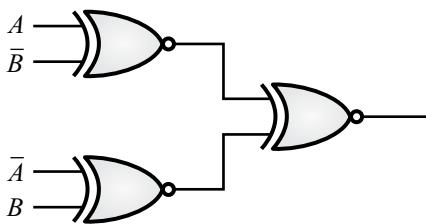
- (A) 1100001
- (B) 1100011
- (C) 1000001
- (D) 1111110

- Q.4** The logic realized by the circuit shown in figure is



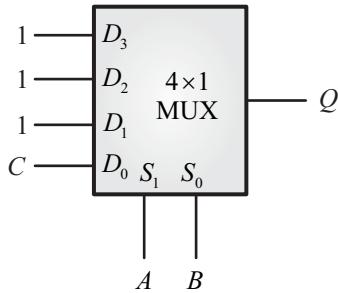
- (A) $F = A \odot C$
- (B) $F = A \oplus C$
- (C) $F = B \odot C$
- (D) $F = B \oplus C$

- Q.5** The output of the circuit shown in figure is equal to



- (A) 0
 (B) 1
 (C) $\bar{A}B + A\bar{B}$
 (D) $(\overline{A \oplus B}) \oplus (\overline{A \oplus B})$

Q.6 The combinatorial circuit shown in figure employs a 4 to 1 multiplexer. The output Q of the circuit is



- (A) $\bar{A}\bar{B}C$
 (B) $A+B+C$
 (C) $A \oplus B \oplus C$
 (D) $\bar{A}\bar{B}\bar{C}$

Q.7 Match the following :

Logic	Function
I. $\bar{X} + \bar{Y}$	P. Sum
II. $X Y$	Q. NAND
III. $\bar{X} \bar{Y}$	R. Carry

- (A) I-Q, II-R, III-S
 (B) I-S, II-R, III-Q
 (C) I-Q, II-P, III-S
 (D) I-S, II-P, III-Q

Q.8 A multiplexer with a 4 bit data select input is a

- (A) 4 : 1 Multiplexer
 (B) 2 : 1 Multiplexer
 (C) 16 : 1 Multiplexer
 (D) 8 : 1 Multiplexer

Q.9 For a binary half-subtractor having two inputs A and B , the correct set of logical expressions for the outputs D ($= A$ minus B) and X ($=$ borrow) are

- (A) $D = AB + \bar{A}B$, $X = \bar{A}B$
 (B) $D = AB + \bar{A}B$, $X = A\bar{B}$

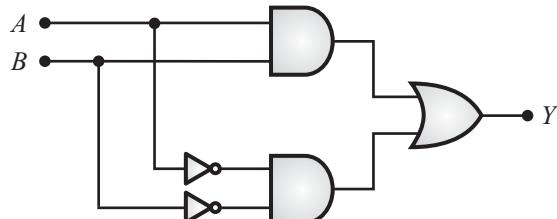
(C) $D = \bar{A}B + A\bar{B}$, $X = \bar{A}B$

(D) $D = \bar{A}B + A\bar{B}$, $X = A\bar{B}$

Q.10 The number of full and half – adders required to add 16 – bit numbers is

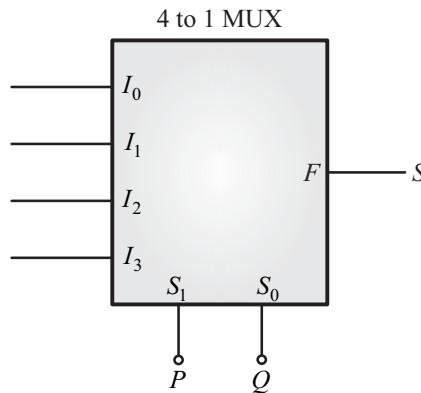
- (A) 8 half – adders, 8 full – adders
 (B) 1 half – adder, 15 full – adders
 (C) 16 half – adders, 0 full – adders
 (D) 4 half – adders, 12 full – adders

Q.11 The logic circuit given below is



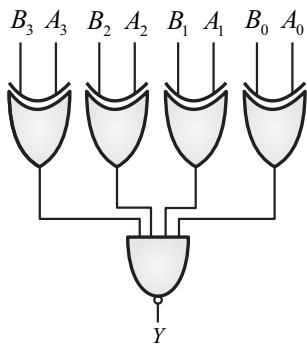
- (A) Half adder
 (B) XOR
 (C) Equality detector
 (D) Full adder

Q.12 Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1 bit full adder with input bits P and Q and the carry input C_{in} . Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S ?



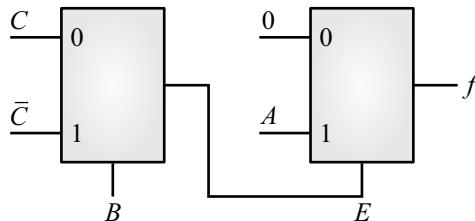
- (A) $I_0 = I_1 = C_{in}$; $I_2 = I_3 = \bar{C}_{in}$
 (B) $I_0 = I_1 = \bar{C}_{in}$; $I_2 = I_3 = C_{in}$
 (C) $I_0 = I_3 = C_{in}$; $I_1 = I_2 = \bar{C}_{in}$
 (D) $I_0 = I_3 = \bar{C}_{in}$; $I_1 = I_2 = C_{in}$

Q.13 A digital circuit which compares two numbers $A_3 A_2 A_1 A_0, B_3 B_2 B_1 B_0$ is shown in figure. To get output $Y = 0$, choose one pair of correct input numbers.



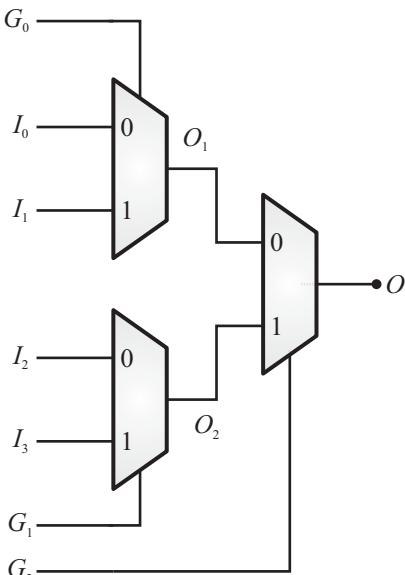
- (A) 1010, 1010 (B) 0101, 0101
 (C) 0010, 0010 (D) 1010, 0101

Q.14 The Boolean function ' f ' implemented in the figure using two input multiplexers is



- (A) $A\bar{B}C + A\bar{B}\bar{C}$ (B) $ABC + A\bar{B}\bar{C}$
 (C) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$ (D) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

Q.15 The cell of a field programmable Gate array is shown in the figure. It has three 2-to-1-multiplexers with their select lines G_0, G_1, G_2 and 4 digital signal input lines I_0, I_1, I_2 and I_3 . The logical function that relates the output O to the select and signal input lines is

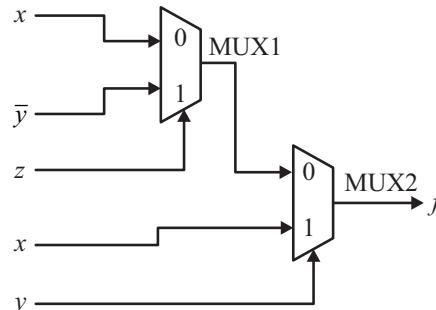


- (A) $\overline{G_0}\overline{G_1}I_2 + \overline{G_0}\overline{G_1}I_3 + \overline{G_2}\overline{G_1}I_0 + \overline{G_2}\overline{G_1}I_1$
 (B) $\overline{G_0}I_2 + \overline{G_0}G_1 + \overline{G_2}I_0 + \overline{G_2}G_1I_1 + G_0$

$$(C) \overline{G_0}\overline{G_2}I_0 + G_0\overline{G_2}I_1 + G_2\overline{G_1}I_2 + G_2G_1I_3$$

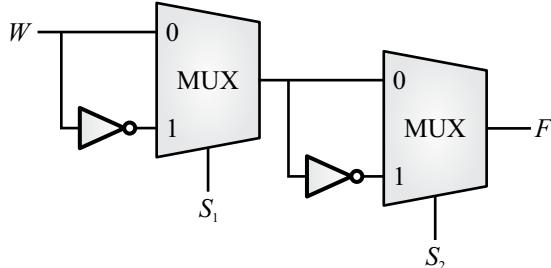
$$(D) G_2G_1\overline{I}_2 + \overline{G_2}\overline{G_1}\overline{I}_3 + G_2\overline{G_0}I_0 + G_0\overline{G_2}I_1$$

Q.16 Consider the circuit given. Which one of the following options correctly represents $f(x, y, z)$?



- (A) $xz + xy + \overline{yz}$ (B) $xz + xy + \overline{yz}$
 (C) $xz + xy + \overline{yz}$ (D) $xz + x\bar{y} + \overline{yz}$

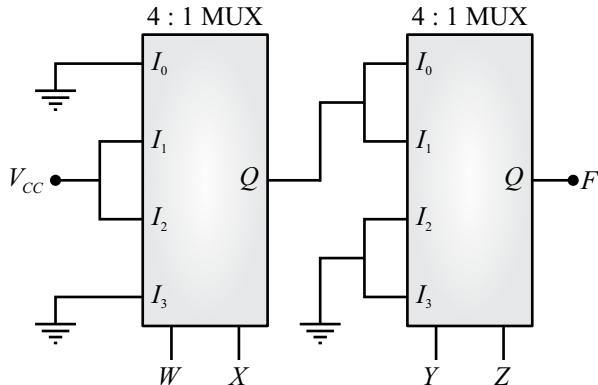
Q.17 Consider the multiplexer based logic circuit shown in the figure.



Which one of the following Boolean functions is realized by the circuit?

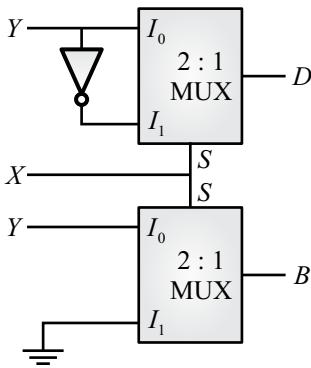
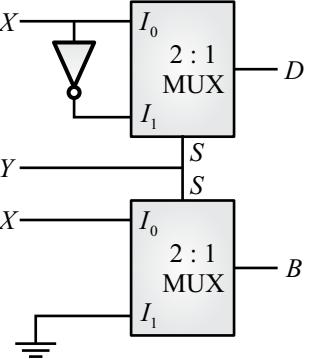
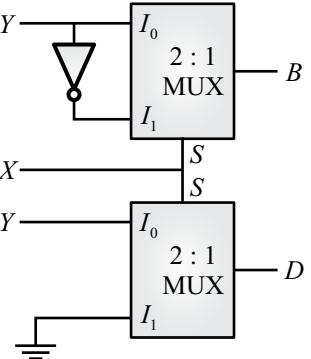
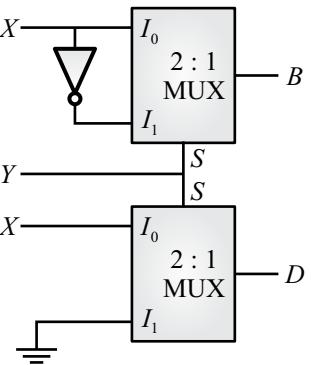
- (A) $F = W\overline{S_1}\overline{S_2}$
 (B) $F = WS_1 + WS_2 + S_1S_2$
 (C) $F = \overline{W} + S_1 + S_2$
 (D) $F = W \oplus S_1 \oplus S_2$

Q.18 In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by

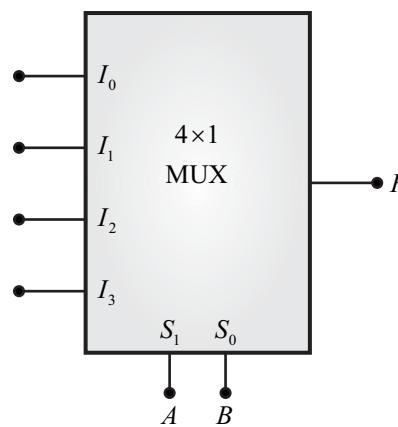


- (A) $F = W \bar{X} + \bar{W} X + \bar{Y} \bar{Z}$
 (B) $F = W \bar{X} + \bar{W} X + \bar{Y} Z$
 (C) $F = W \bar{X} \bar{Y} + \bar{W} X \bar{Y}$
 (D) $F = (\bar{W} + \bar{X}) \bar{Y} \bar{Z}$

Q.19 If X and Y are inputs and the Difference (D) = $X - Y$ and the Borrow (B) are the outputs, which one of the following diagrams implements a half-subtractor?

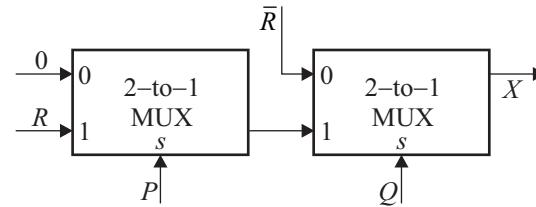
- (A) 
- (B) 
- (C) 
- (D) 

Q.20 In the 4×1 multiplexer, the output F is given by $F = A \oplus B$. Find the required input $I_3 I_2 I_1 I_0$.



- (A) 1010 (B) 0110
 (C) 1000 (D) 1110

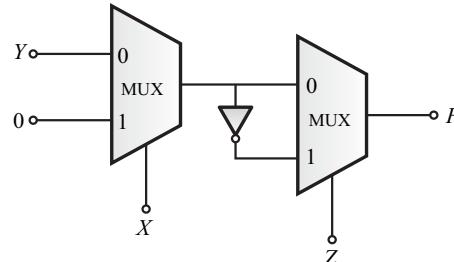
Q.21 Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



The minimal sum of products form of the output X is

- (A) $\overline{PQ} + PQR$ (B) $\overline{PQ} + QR$
 (C) $PQ + \overline{PQR}$ (D) $\overline{QR} + PQR$

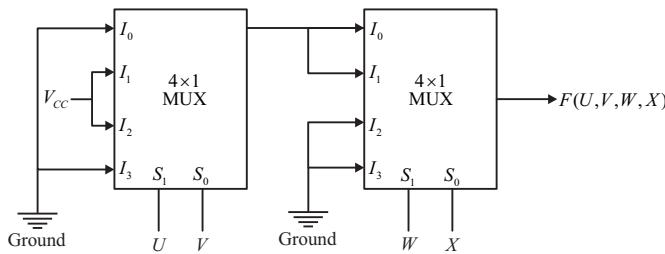
Q.22 Consider the circuit shown in the figure.



The Boolean expression F implemented by the circuit is

- (A) $\bar{X} \bar{Y} \bar{Z} + XY + \bar{Y} Z$
 (B) $\bar{X} Y \bar{Z} + XZ + \bar{Y} Z$
 (C) $\bar{X} Y \bar{Z} + XY + \bar{Y} Z$
 (D) $\bar{X} \bar{Y} \bar{Z} + XZ + \bar{Y} Z$

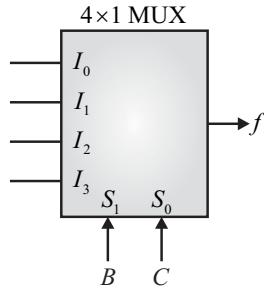
Q.23 A four-variable Boolean function is realized using 4×1 multiplexers as shown in the figure.



The minimized expression for $F(U, V, W, X)$ is

- (A) $(UV + \bar{U}\bar{V})\bar{W}$
- (B) $(UV + \bar{U}\bar{V})(\bar{W}\bar{X} + \bar{W}X)$
- (C) $(U\bar{V} + \bar{U}V)\bar{W}$
- (D) $(U\bar{V} + \bar{U}V)(\bar{W}\bar{X} + \bar{W}X)$

- Q.24** The Boolean function $F(A, B, C) = \Pi(0, 5, 6)$ is to be implemented using a 4×1 multiplexer shown in figure. Which one of the following choice of inputs to semi programmed multiplexer will realize the Boolean function?



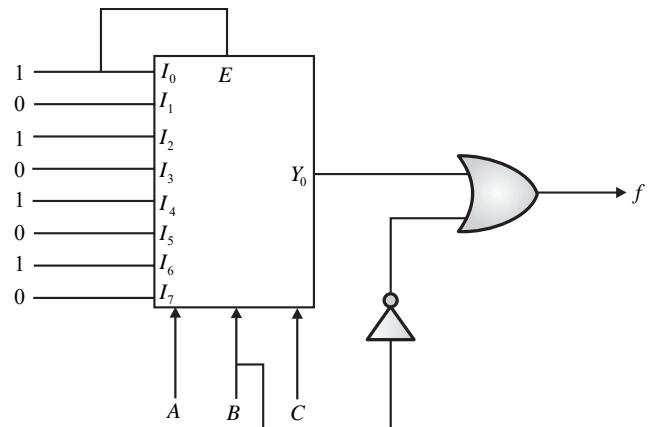
- (A) $I_0 = I_1 = 1, I_2 = I_3 = 0$
- (B) $I_0 = I_1 = A \text{ & } I_2 = I_3 = \bar{A}$
- (C) $I_0 = I_3 = A \text{ & } I_1 = I_2 = \bar{A}$
- (D) $I_0 = I_3 = \bar{A} \text{ & } I_1 = I_2 = A$

- Q.25** A number is represented in binary system 1010111. It's gray code equivalent is

- (A) 111100
- (B) 111011
- (C) 1010111
- (D) 111110

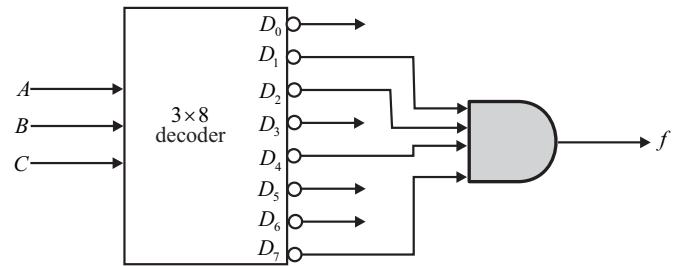
- Q.26** What is the minimum number of 2×1 Multiplexer required to realize a 16×1 Multiplexer?

- Q.27** Which of the following is the output Boolean expression for 'f'



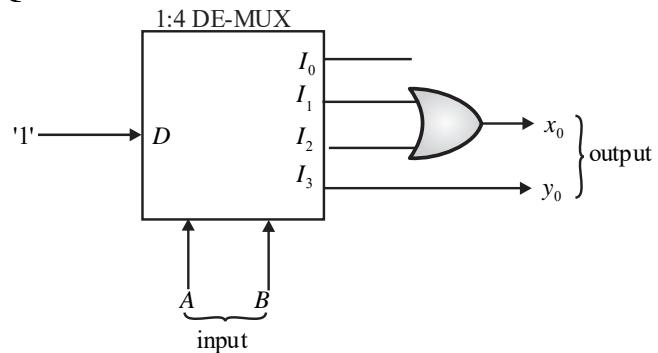
- (A) $\bar{B} + C$
- (B) \bar{C}
- (C) \bar{B}
- (D) \bar{BC}

- Q.28** The output expression of the digital circuit shown in figure.



- (A) $f = \sum m(0, 3, 5, 6)$
- (B) $f = \sum m(0, 5, 6)$
- (C) $f = \prod M(1, 2, 4, 7)$
- (D) $f = \sum m(1, 2, 4, 7)$

- Q.29** The circuit shown can act as



- (A) Half Adder
- (B) Comparator
- (C) Half subtractor
- (D) All of the above



Answer Keys

Classroom Practice Questions									
Multiplexer									
1.	D	2.	D	3.	A	4.	A	5.	D
6.	A	7.	A	8.	B	9.	D	10.	C
11.	A	12.	D	13.	A	14.	C	15.	C
16.	B	17.	A	18.	C	19.	6	20.	A
21.	C	22.	B	23.	C	24.	A	25.	C
26.	A	27.	D						
Decoder									
1.	A	2.	B	3.	C	4.	B		
Adder									
1.	C	2.	C	3.	B	4.	A	5.	195
6.	19.2	7.	A	8.	*				
Code Converter									
1.	B	3.	D	4.	A				
Self-Practice Questions									
1.	B	2.	B	3.	A	4.	B	5.	B
6.	B	7.	A	8.	A	9.	C	10.	B
11.	C	12.	C	13.	D	14.	A	15.	C
16.	A	17.	D	18.	C	19.	A	20.	B
21.	D	22.	B	23.	C	24.	C	25.	D
26.	15	27.	D	28.	D	29.	A		

* 8. **B** is substracted from **A** using 2's complement arithmetic.

6

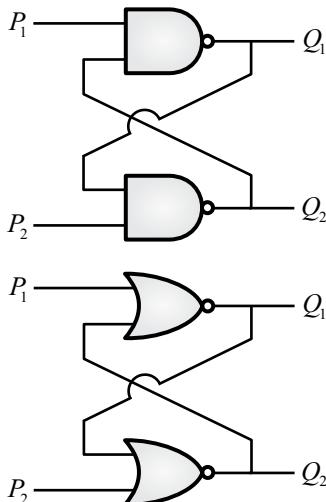
Sequential Circuits

Classroom Practice Questions :

Flip-Flops :

- Q.1** Refer to the NAND and NOR latches shown in the figure. The input (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable output (Q_1, Q_2) are

[GATE 2009, IIT Roorkee]



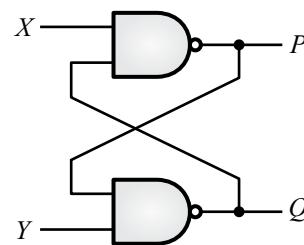
- (A) NAND: first (0, 1) then (0, 1) NOR : first (1, 0) then (0, 0).
(B) NAND: first (1, 0) then (1, 0) NOR : first (1, 0) then (1, 0).
(C) NAND: first (1, 0) then (1, 0) NOR : first (1, 0) then (0, 0).
(D) NAND: first (1, 0) then (1, 1) NOR : first (0, 1) then (0, 1).

- Q.2** The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below :

$$X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1,$$

The corresponding stable P, Q outputs will be

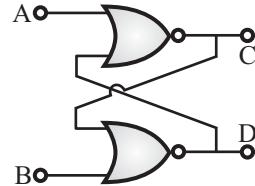
[GATE 2007, IIT Kanpur]



- (A) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$
(B) $P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$
(C) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$ or $P = 0, Q = 1$
(D) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$

- Q.3** In the circuit shown in figure, when input $A = B = 0$, the possible logic states of C and D are

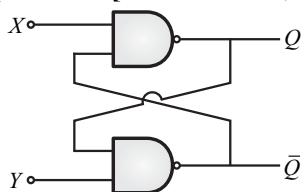
[GATE 2001, IIT Kanpur]



- (A) $C = 0, D = 1$ or $C = 1, D = 0$
(B) $C = 1, D = 1$ or $C = 0, D = 0$

- (C) $C=1, D=0$ (D) $C=0, D=1$

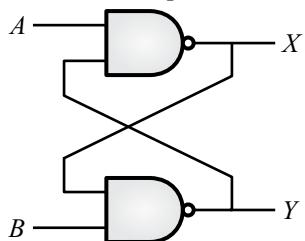
Q.4 For a flip-flop formed using two NAND gates as shown in figure. The unstable state corresponds to [GATE 1999, IIT Bombay]



- (A) $X=0, Y=0$ (B) $X=0, Y=1$
 (C) $X=1, Y=0$ (D) $X=1, Y=1$

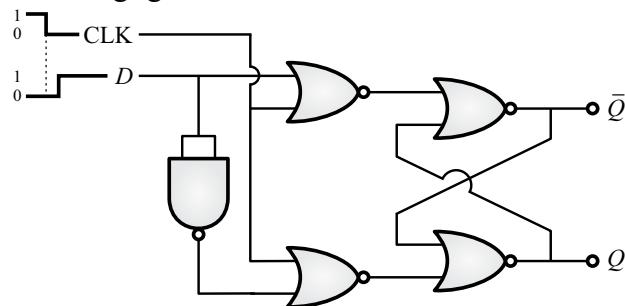
Q.5 In figure $A = 1$ and $B = 1$, the input B is now replaced by a sequence 101010 , the output X and Y will be

[GATE 1998, IIT Delhi]



- (A) fixed at 0 and 1 respectively
 (B) $X=1010 \dots$ while $Y=0101 \dots$
 (C) $X=1010 \dots$ while $Y=1010 \dots$
 (D) fixed at 1 and 0 respectively

Q.6 For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible.



Which of the following statement is true?

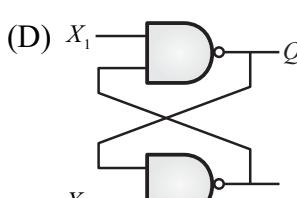
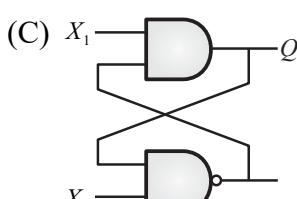
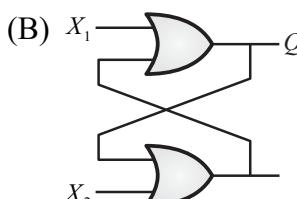
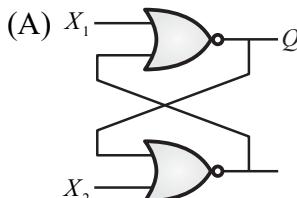
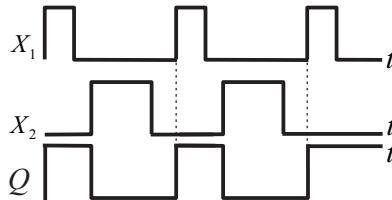
[GATE 2008, IISc Bangalore]

- (A) Q goes to 1 at the CLK transition and stays at 1.
 (B) Q goes to 0 at the CLK transition and stays at 0.
 (C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1.

(D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1.

Q.7 Select the circuit which will produce the given output Q for the input signals X_1 and X_2 given in the figure

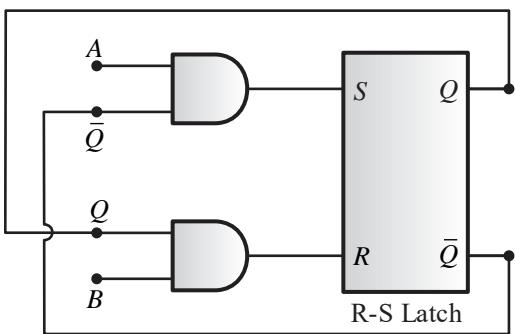
[GATE 2005, IIT Bombay]



Q.8

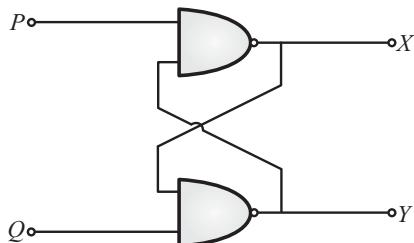
The two inputs A and B are connected to an R-S latch via two AND gates as shown in the figure. If $A=1$ and $B=0$, the output $Q\bar{Q}$ is

[GATE 2017, IIT Roorkee]



- (A) 00 (B) 10
 (C) 01 (D) 11

Q.9 In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is : $P = Q = '0'$. If the input condition is changed simultaneously to $P = Q = '1'$, the outputs X and Y are [GATE 2017, IIT Roorkee]



- (A) $X = '1'$, $Y = '1'$
 (B) Either $X = '1'$, $Y = '0'$ or $X = '0'$,
 $Y = '1'$
 (C) Either $X = '1'$, $Y = '1'$ or $X = '0'$,
 $Y = '0'$
 (D) $X = '0'$, $Y = '0'$

Q.10 An $X-Y$ flip-flop, whose characteristic table is given below is to be implemented using a $J-K$ flip-flop [GATE 2003, IIT Madras]

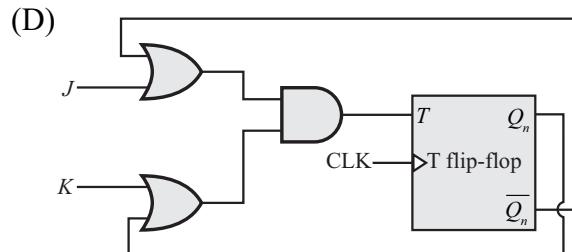
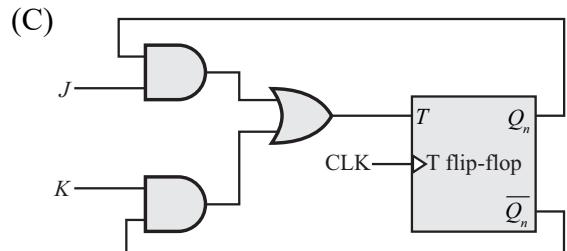
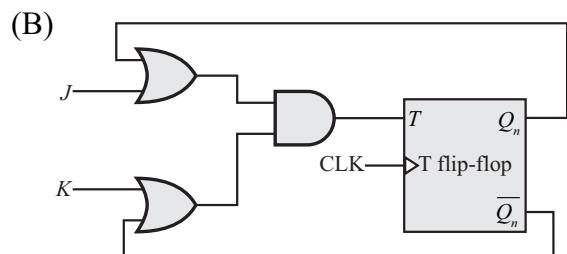
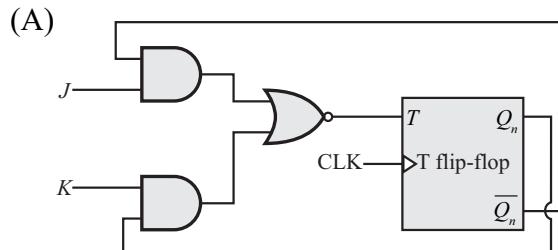
X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	\bar{Q}_n
1	1	0

This can be done by making

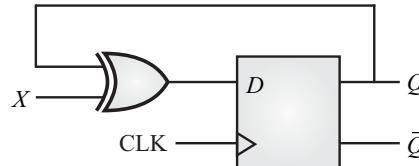
- (A) $J = X$, $K = \bar{Y}$ (B) $J = \bar{X}$, $K = Y$
 (C) $J = Y$, $K = \bar{X}$ (D) $J = \bar{Y}$, $K = X$

Q.11 A $J-K$ flip-flop can be implemented by T flip-flops. Identify the correct implementation.

[GATE 2014, IIT Kharagpur]

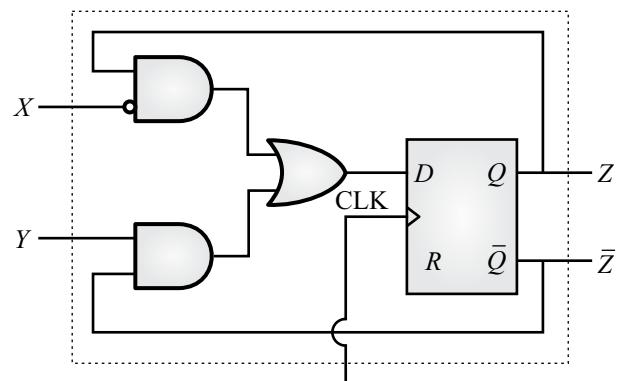


Q.12 The digital circuit shown in the figure works as [GATE 2005, IIT Bombay]



- (A) $J-K$ flip-flop
 (B) Clocked RS flip-flop
 (C) T flip-flop
 (D) Ring counter

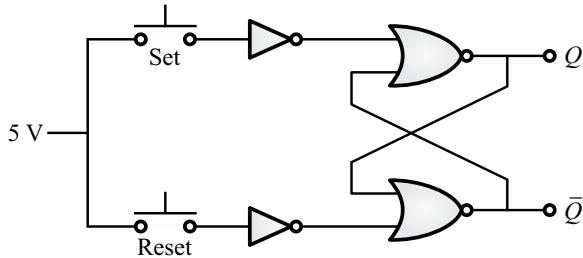
Q.13 A sequential circuit using D Flip-Flop and logic gates is shown in figure, where X and Y are the inputs and Z is the output. The circuit is [GATE 2000, IIT Kharagpur]



- (A) S-R Flip-Flop with inputs $X = R$ and $Y = S$.
 (B) S-R Flip-Flop with inputs $X = S$ and $Y = R$.
 (C) J-K Flip-Flop with inputs $X = J$ and $Y = K$.
 (D) J-K Flip-Flop with inputs $X = K$ and $Y = J$.

Q.14 An S-R latch is implemented using TTL gates as shown in the figure. The set and reset pulse inputs are provided using the push-button switches. It is observed that the circuit fails to work as desired. The S-R latch can be made functional by changing

[GATE 2015, IIT Kanpur]



- (A) NOR gates to NAND gates.
 (B) Inverters to buffers.
 (C) NOR gates to NAND gates and inverters to buffers.
 (D) 5 V to ground.

Synchronous Counter :

Q.1 Two D flip-flops are connected as a synchronous counter that goes through the following $Q_B Q_A$ sequence

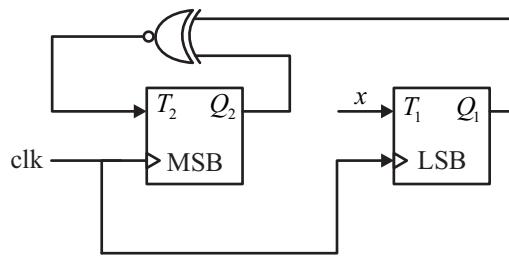
$$00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \dots$$

The connections to the inputs D_A and D_B are

[GATE 2011, IIT Madras]

- (A) $D_A = Q_B$, $D_B = Q_A$
 (B) $D_A = \bar{Q}_A$, $D_B = \bar{Q}_B$
 (C) $D_A = (Q_A \bar{Q}_B + \bar{Q}_A Q_B)$, $D_B = Q_A$
 (D) $D_A = (Q_A Q_B + \bar{Q}_A \bar{Q}_B)$, $D_B = \bar{Q}_B$

Q.2 Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below.



To complete the circuit, the input X should be

[GATE 2004, IIT Delhi]

- (A) Q_2' (B) $Q_2 + Q_1$
 (C) $(Q_1 \oplus Q_2)'$ (D) $(Q_1 \oplus Q_2)$

Q.3 The next state table of a 2-bit saturating up-counter is given below.

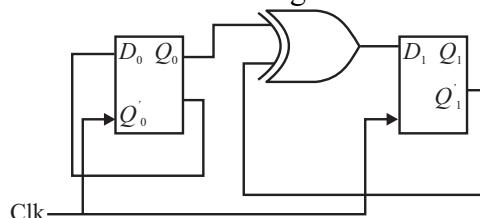
Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expression for T_1 and T_0 are

[GATE 2017, IIT Roorkee]

- (A) $T_1 = Q_1 Q_0$, $T_0 = \bar{Q}_1 \bar{Q}_0$
 (B) $T_1 = \bar{Q}_1 Q_0$, $T_0 = \bar{Q}_1 + \bar{Q}_0$
 (C) $T_1 = Q_1 + Q_0$, $T_0 = \bar{Q}_1 + \bar{Q}_0$
 (D) $T_1 = \bar{Q}_1 Q_0$, $T_0 = Q_1 + Q_0$

Q.4 Consider the following circuit.



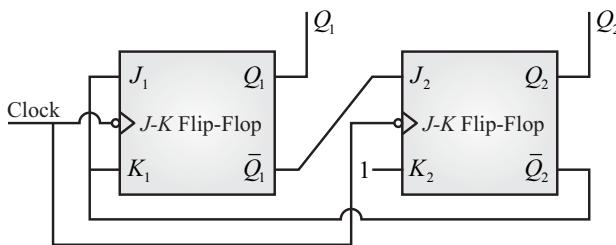
The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string $Q_0 Q_1$. Let the initial state be 00. The state transition sequence is

[GATE 2005, IIT Bombay]

- (A) $00 \rightarrow 11 \rightarrow 01$ (B) $00 \rightarrow 11$
 (C) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$ (D) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

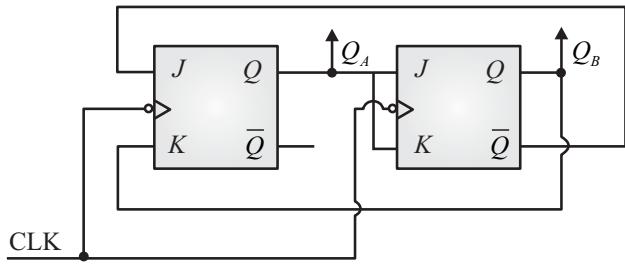
Q.5 What are the counting state (Q_1, Q_2) for the counter shown in the figure below?

[GATE 2009, IIT Roorkee]



- (A) 11, 10, 00, 11, 10,....
 (B) 01, 10, 11, 00, 01,....
 (C) 00, 11, 01, 10, 00,....
 (D) 01, 10, 00, 01, 10,....

Q.6 A 2-bit counter circuit is shown below,



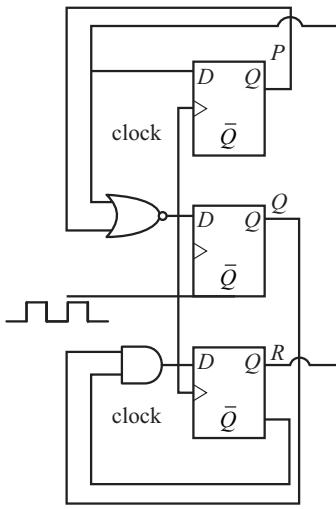
If the state $Q_A Q_B$ of the counter at the clock time t_n is "10" then the state $Q_A Q_B$ of the counter at $t_n + 3$ (after three cycles) will be

[GATE 2011, IIT Madras]

- (A) 00 (B) 01
 (C) 10 (D) 11

Common Data for Questions 7 & 8

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



Q.7 If all the flip-flops were reset to 0 at power on, what is the total number of distinct

outputs (states) represented by PQR generated by the counter?

[GATE 2011, IIT Madras]

- (A) 3 (B) 4
 (C) 5 (D) 6

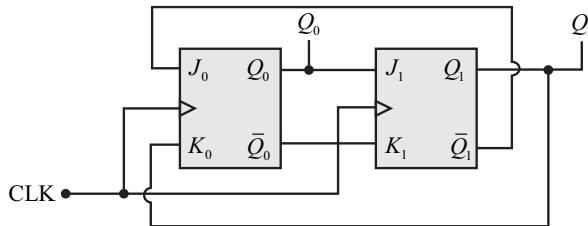
Q.8 If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

[GATE 2011, IIT Madras]

- (A) 000 (B) 001
 (C) 010 (D) 011

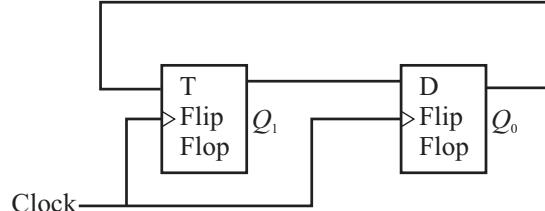
Q.9 In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1 Q_0 = 00$. The state $(Q_1 Q_0)$, immediately after the 333rd clock pulse is

[GATE 2015, IIT Kanpur]



- (A) 00 (B) 01
 (C) 10 (D) 11

Q.10 Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

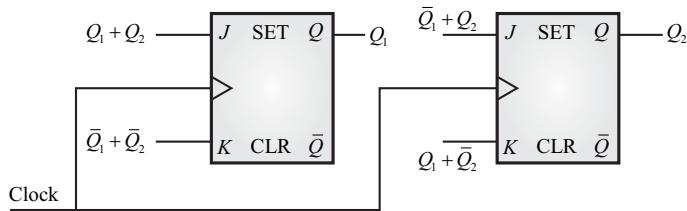
[GATE 2017, IIT Roorkee]

- (A) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
 (B) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

- (C) $Q_1 Q_0$ after the 3rd cycle are 00 and after the 4th cycle are 11 respectively
(D) $Q_1 Q_0$ after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

Q.11 A 2-bit synchronous counter using two *J-K* flip flops is shown. The expressions for the inputs to the *J-K* flip flops are also shown in the figure. The output sequence of the counter starting from $Q_1 Q_2 = 00$ is

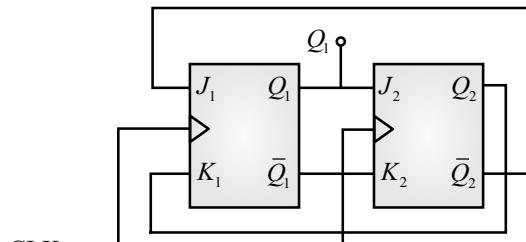
[GATE 2018, IIT Guwahati]



- (A) 00 → 11 → 10 → 01 → 00...
(B) 00 → 01 → 10 → 11 → 00...
(C) 00 → 01 → 11 → 10 → 00...
(D) 00 → 10 → 11 → 01 → 00...

Q.12 The outputs of the two flip-flops Q_1, Q_2 in the figure shown are initialized to 0, 0. The sequence generated at Q_1 upon application of clock signal is

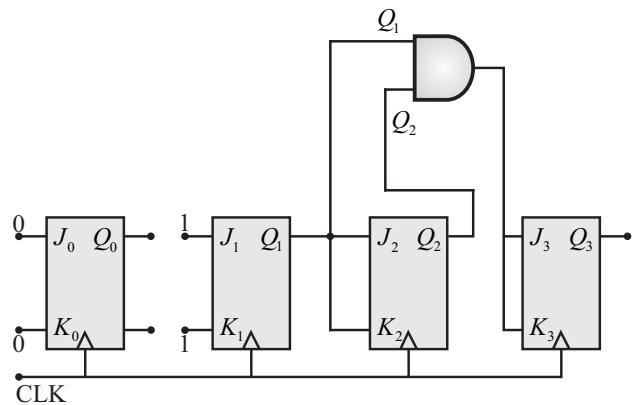
[GATE 2014, IIT Kharagpur]



- (A) 01110.... (B) 01010....
(C) 00110... (D) 01100.....

Q.13 Figure shows a sequential circuit with four *J-K* flip-flops and generate a table of output ($Q_3 Q_2 Q_1 Q_0$) changes with each clock pulse. Start with $Q_3 Q_2 Q_1 Q_0 = 0001$ and the next state after the first clock pulse

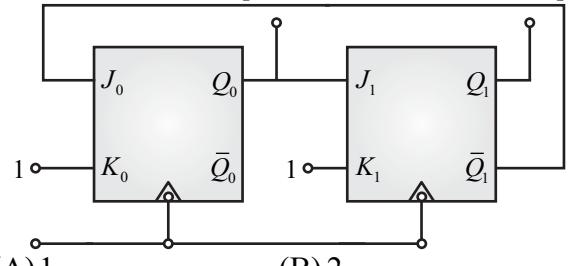
[GATE 1995, IIT Kanpur]



- (A) 1111 (B) 1100
(C) 0001 (D) 0011

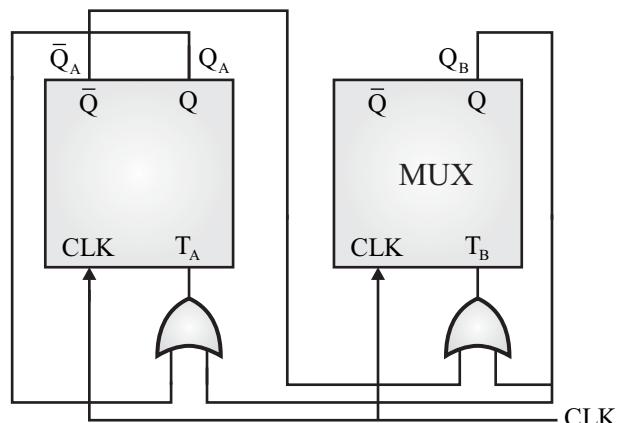
Q.14 Given below figure shows a MOD-*k* counter, here *k* is equal to

[GATE 1998, IIT Delhi]



- (A) 1 (B) 2
(C) 3 (D) 4

Q.15 A sequential circuit is shown in the figure below. Let the state of the circuit be encoded as Q_A, Q_B . The notation $X \rightarrow Y$ implies that state Y is reachable from state X in a finite number of clock transitions.



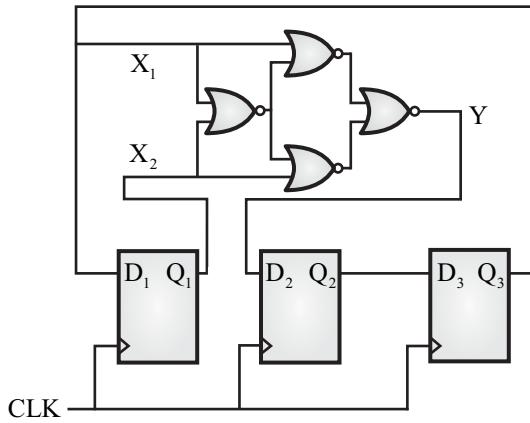
Identify the INCORRECT statement.

[GATE 2007, IIT Kanpur]

- (A) 01 → 00 (B) 11 → 01
(C) 01 → 11 (D) 01 → 10

Common Data for
Questions 16 & 17

Consider the circuit shown in the following figure.



- Q.16** The correct input-output relationship between Y and (X_1X_2) is

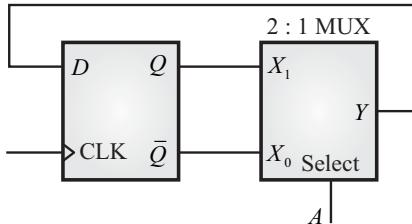
[GATE 2007, IIT Kanpur]

- (A) $Y = X_1 + X_2$ (B) $Y = X_1X_2$
 (C) $Y = X_1 \oplus X_2$ (D) $Y = \overline{X_1 \oplus X_2}$

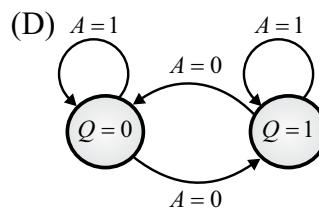
- Q.17** The D flip-flop are initialized to $Q_1Q_2Q_3 = 000$. After 1 clock cycle, $Q_1Q_2Q_3$ is equal to [GATE 2007, IIT Kanpur]

- (A) 001 (B) 010
 (C) 100 (D) 101

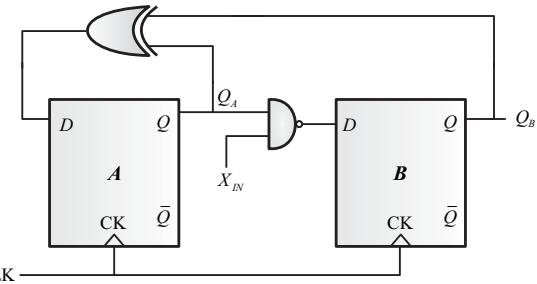
- Q.18** The state transition diagram for the logic circuit shown is [GATE 2012, IIT Delhi]



- (A) $A = 1$
 (B) $A = 0$
 (C) $A = 1$



- Q.19** A finite state machine (FSM) is implemented using the D flip-flops A and B and logic gates, as shown in the figure below. The four possible states of the FSM are $Q_AQ_B = 00, 01, 10$ and 11 .

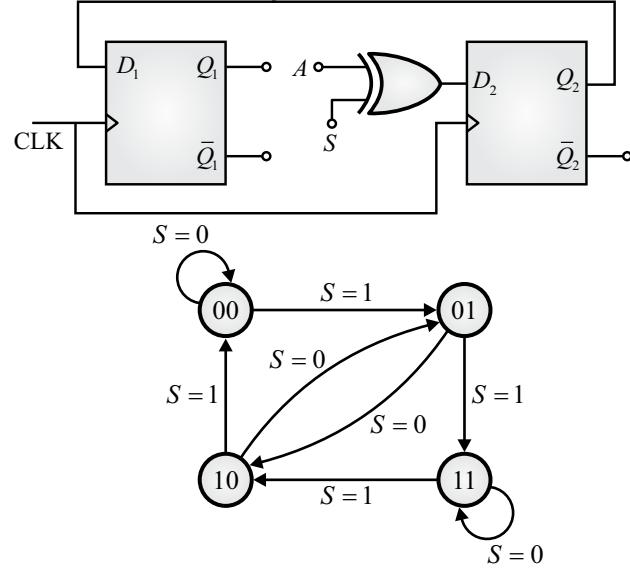


Assume that X_{IN} is held at a constant logic level throughout the operation of the FSM. When the FSM is initialized to the state $Q_AQ_B = 00$ and clocked, after a few clock cycles, it starts cycling through

[GATE 2017, IIT Roorkee]

- (A) all of the four possible states if $X_{IN} = 1$.
 (B) three of the four possible states if $X_{IN} = 0$.
 (C) only two of the four possible states if $X_{IN} = 1$.
 (D) only two of the four possible states if $X_{IN} = 0$.

- Q.20** The digital logic shown in the figure satisfies the given state diagram when Q_1 is connected to input A of the XOR gate.



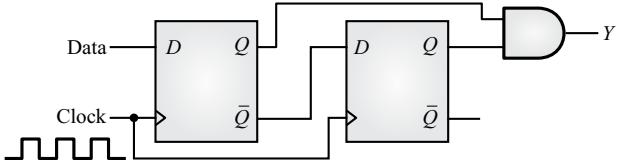
Suppose the XOR gate is replaced by an XNOR gate. Which one of the following option preserves the state diagram?

[GATE 2014, IIT Kharagpur]

- (A) Input A is connected to \bar{Q}_2
- (B) Input A is connected to Q_2
- (C) Input A is connected to \bar{Q}_1 and S is complemented
- (D) Input A is connected to \bar{Q}_1

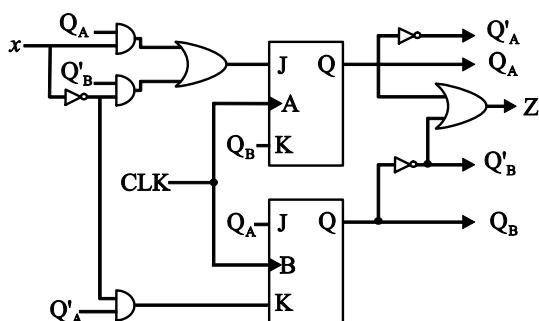
Q.21 When the output Y in the circuit below is “1”, it implies that data has

[GATE 2011, IIT Madras]



- (A) changed from “0” to “1”.
- (B) changed from “1” to “0”.
- (C) changed in either direction.
- (D) not changed.

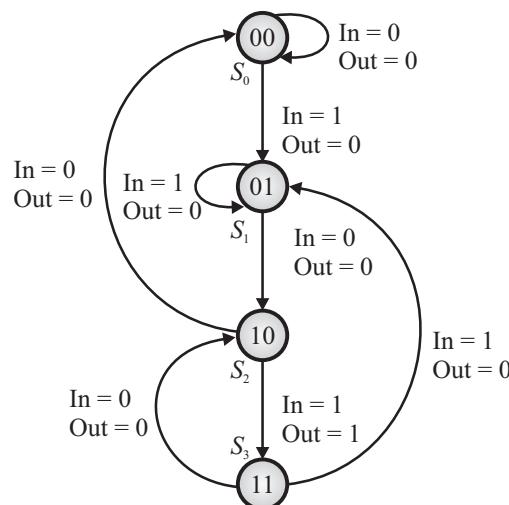
Q.22



Analyze the sequential circuit shown above in figure. Assuming that initial state is 00, determine what input sequence would lead to state 11?

- (A) 1 – 1
- (B) 1 – 0
- (C) 0 – 0
- (D) state 11 is unreachable

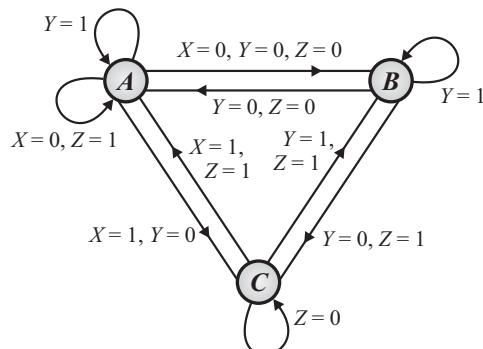
Q.23 The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input ‘In’ and an output ‘Out’. The initial state of the FSM is S_0 .



If the input sequence is 10101101001101, starting with the left-most bit, then the number of times ‘Out’ will be 1 is ____.

Q.24 The state transition diagram for a finite state machine with states A, B and C, and binary inputs X, Y and Z is shown in the figure.

[GATE 2016, IISc Bangalore]



Which one of the following statements is correct?

- (A) Transitions from State A are ambiguously defined.
- (B) Transitions from State B are ambiguously defined.
- (C) Transitions from State C are ambiguously defined.
- (D) All of the state transitions are defined unambiguously.

Miscellaneous Questions (FF & Counters) :

Q.10 The minimum number of flip-flops needed to make mod-2 counter is

[GATE 1998, IIT Delhi]

- (A) 1
- (B) 2
- (C) 3
- (D) 4

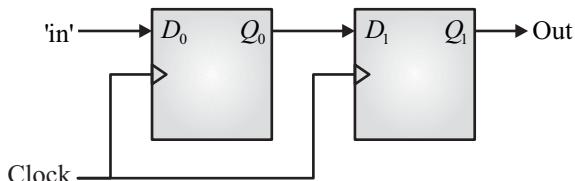
- Q.11** The minimum number of J-K flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0,) is _____.

[GATE 2015, IIT Kanpur]

- Q.12** We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____. [GATE 2016, IISc Bangalore]

- Q.13** Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.

[GATE 2018, IIT Guwahati]



The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is _____.

- Q.14** Given the following state table of an FSM with two states A and B, one input and one output :

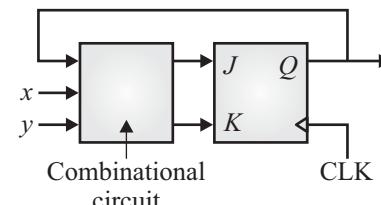
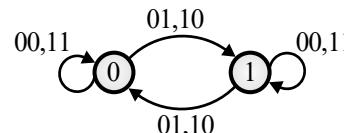
Present state A	Present state B	Input	Next state A	Next state B	Output
0	0	0	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	1	0	0
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	0	0	1

If the initial state is A = 0, B = 0, what is the minimum length of an input string which will take the machine to the state A = 0, B = 1 with Output = 1?

[GATE 2009, IIT Roorkee]

- (A) 3 (B) 4
 (C) 5 (D) 6

- Q.15** Consider the following state diagram and its realization by a JK flip flop.



The combinational circuit generates J and K in terms of x, y and Q. The Boolean expressions for J and K are :

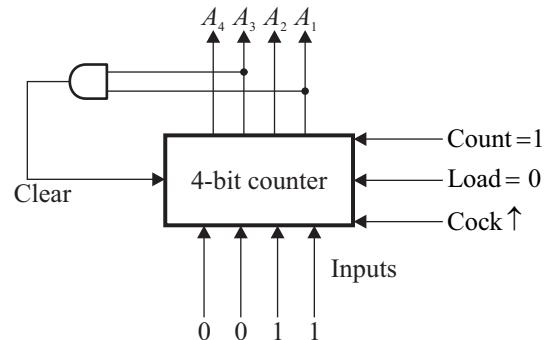
[GATE 2008, IISc Bangalore]

- (A) $\overline{x \oplus y}$ and $\overline{x \oplus y}$
 (B) $\overline{x \oplus y}$ and $x \oplus y$
 (C) $x \oplus y$ and $\overline{x \oplus y}$
 (D) $x \oplus y$ and $x \oplus y$

- Q.16** The control signal functions of a 4-bit binary counter are given below (where X is "don't care") :

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows :



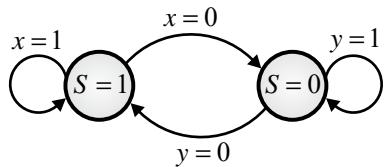
Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequences :

[GATE 2007, IIT Kanpur]

- (A) 0, 3, 4 (B) 0, 3, 4, 5
 (C) 0, 1, 2, 3, 4 (D) 0, 1, 2, 3, 4, 5

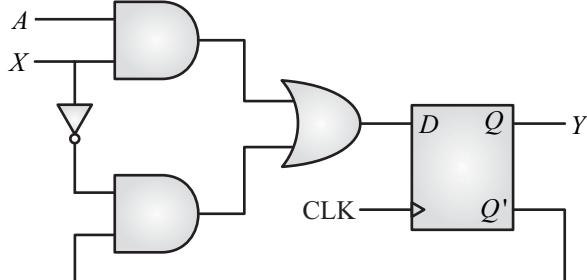
- Q.17** For a state machine with the following state diagram the expression for the next state S^+ in terms of the current state S and the input variables x and y is

[GATE 2006, IIT Kharagpur]

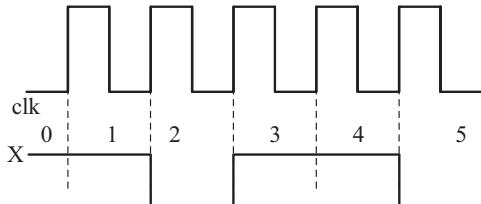


- (A) $S^+ = S' y' + Sx$ (B) $S^+ = Sxy' + S' yx'$
 (C) $S^+ = xy'$ (D) $S^+ = S'y + Sx'$

- Q.18** Consider the following circuit involving a positive edge triggered D-flip-flop.



Consider the following timing diagram. Let A_i represent the logic level on the line A in the i -th clock period.



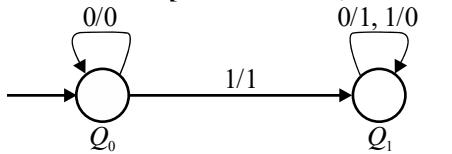
Let A' represent the complement of A. The correct output sequence on Y over the clock periods 1 through 5 is :

[GATE 2005, IIT Bombay]

- (A) $A_0 \ A_1 \ A_1' \ A_3 \ A_4$
 (B) $A_0 \ A_1 \ A_2' \ A_3 \ A_4$
 (C) $A_1 \ A_2 \ A_2' \ A_3 \ A_4$
 (D) $A_1 \ A_2' \ A_3 \ A_4 \ A_5'$

- Q.19** The following diagram represents a finite state machine which takes as input a binary number from the least significant bit.

[GATE 2005, IIT Bombay]

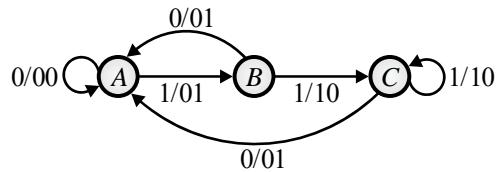


Which one of the following is TRUE?

- (A) It computes 1's complement of the input number
 (B) It computes 2's complement of the input number
 (C) It increments the input number
 (D) It decrements the input number

- Q.20** The finite state machine described by the following state diagram with A as starting state, where an arc label x/y and x stands for 1-bit input and y stands for 2-bit output

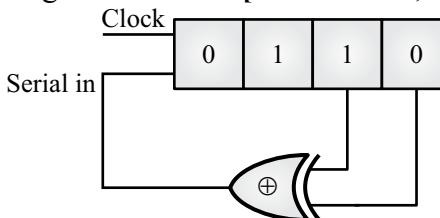
[GATE 2002, IISc Bangalore]



- (A) Outputs the sum of the present and the previous bits of the input.
 (B) Outputs 01 whenever the input sequence contains 11.
 (C) Outputs 00 whenever the input sequence contains 10.
 (D) None of the above

Shift Registers

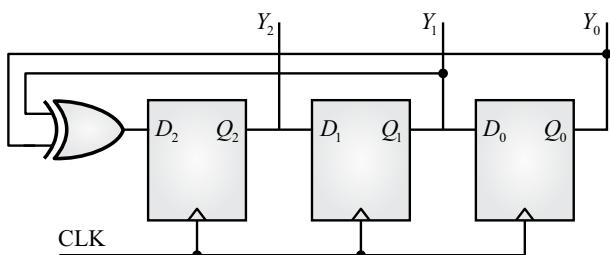
- Q.1** The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After three clock pulses are applied, the contents of the Shift Register will be [GATE 1992, IIT Delhi]



- (A) 0000 (B) 0101
 (C) 1010 (D) 1111

- Q.2** A three bit pseudo random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y after three clock cycles is

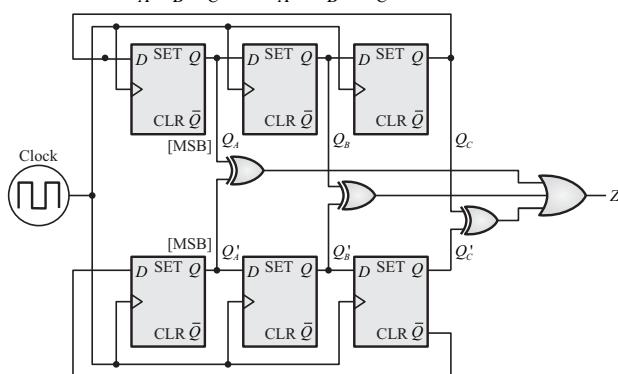
[GATE 2015, IIT Kanpur]



- (A) 000 (B) 001
 (C) 010 (D) 100

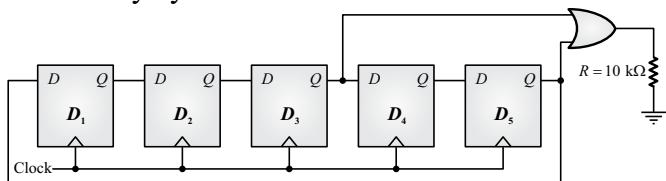
Q.3 For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions

$$Q_A Q_B Q_C = Q_A' Q_B' Q_C' = 100$$



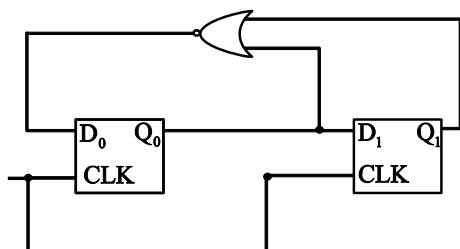
The minimum number of clock cycles after which the output Z would again become zero is _____. [GATE 2017, IIT Roorkee]

Q.4 Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10 \text{ k}\Omega$ and the supply voltage is 5 V. The D flip-flops D_1, D_2, D_3, D_4 and D_5 are initialized with logic values 0, 1, 0, 1 and 0 respectively. The clock has a 30% duty cycle.



The average power dissipated (in mW) in the resistor R is _____. [GATE 2016, IISc Bangalore]

Q.5

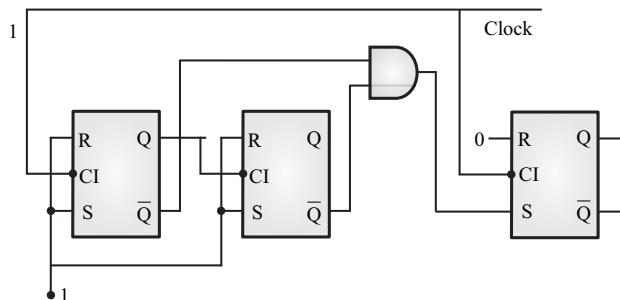


For the circuit shown, the counter state ($Q_2 Q_1 Q_0$) follows the sequence :

- (A) 00, 01, 10, 11, 00
 (B) 00, 01, 10, 00, 01
 (C) 00, 01, 11, 00, 01
 (D) 00, 10, 11, 00, 01

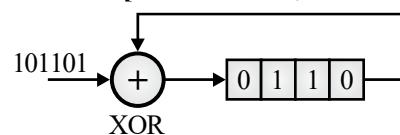
Q.7 In the digital circuit shown in fig. the flip flops have set time of 5 ns and a worst case delay of 15 ns. The AND gate has a delay of 5 ns. Maximum possible clock rate for the circuit to operate faithfully is

[GATE 2004, IIT Delhi]



- (A) 21 MHz (B) 22 MHz
 (C) 25 MHz (D) 30 MHz

Q.8 What is the final value stored in the linear feedback shift register if the input is 101101? [GATE 2007, IIT Kanpur]

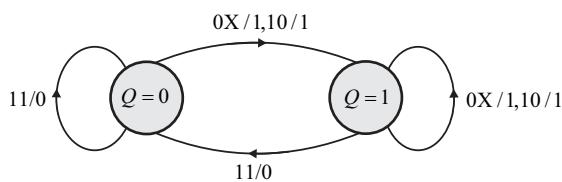


- (A) 0110 (B) 1011
 (C) 1101 (D) 1111

Self-Practice Questions :

Q.1 A 4-bit synchronous counter with a series carry, uses flip-flop and AND gates, having a propagation delay of 30 ns and 10 ns respectively. The maximum time interval required between two successive clock pulses for reliable operation of the counter is
 (A) 10 ns (B) 30 ns
 (C) 40 ns (D) 50 ns

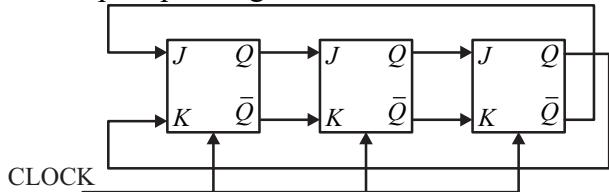
Q.2 A state diagram of a logic which exhibits a delay in the output is shown in the figure, where X is the don't care condition, and Q is the output representing the state.



The logic gate represented by the state diagram is

- (A) XOR (B) OR
 (C) AND (D) NAND

- Q.3** For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is



- (A) Shift Register (B) Mod-3 Counter
 (C) Mod-6 Counter (D) Mod-2 Counter

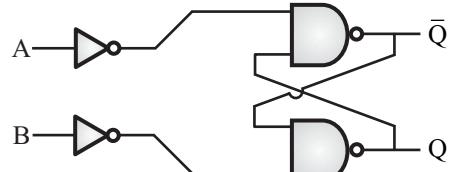
- Q.4** The output Q_{n+1} of a J-K flip-flop for the input $J=1, K=1$ is

- (A) 0 (B) 1
 (C) Q_n (D) \bar{Q}_n

- Q.5** The minimum number of flip-flop required to design a MOD-10 counter is

- (A) 3 (B) 10
 (C) 4 (D) 5

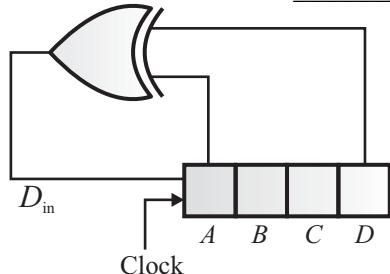
- Q.6**



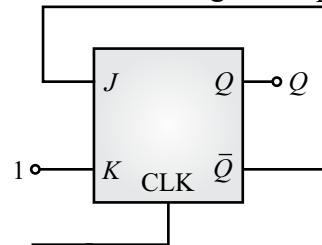
The circuit shown in figure is a

- (A) R-S latch (B) R-S flip-flop
 (C) D latch (D) D flip-flop

- Q.7** A 4-bit shift register circuit configured for right-shift operation, i.e. $D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$, is shown. If the present state of the shift register is $ABCD = 1101$, the number of clock cycles required to reach the state $ABCD = 1111$ is _____.



- Q.8** Consider the following J-K flip-flop

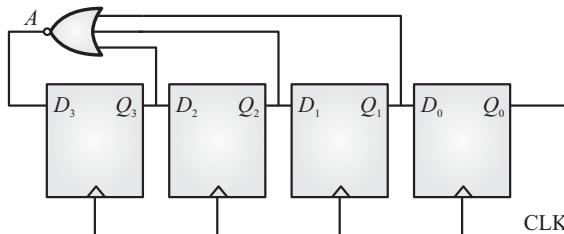


In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$

Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

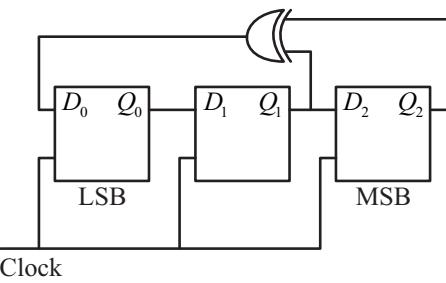
- (A) 010000 (B) 011001
 (C) 010010 (D) 010101

- Q.9** The circuit shown in the figure is a MOD- N ring counter. Value of N is (assume initial state of the counter is 1110 i.e. $Q_3 Q_2 Q_1 Q_0 = 1110$)



- (A) 4 (B) 5
 (C) 7 (D) 6

- Q.10** Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value of $4Q_2 + 2Q_1 + Q_0$.

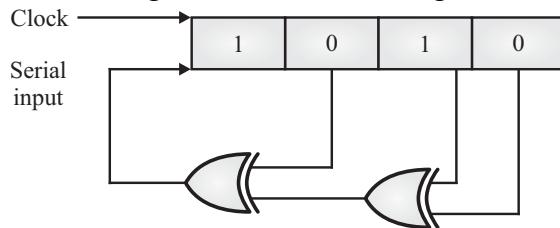


Which one of the following is the correct state sequence of the circuit?

- (A) 1, 3, 4, 6, 7, 5, 2 (B) 1, 2, 5, 3, 7, 6, 4
 (C) 1, 2, 7, 3, 5, 6, 4 (D) 1, 6, 5, 7, 2, 3, 4

- Q.11** The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked and with each clock pulse the pattern gets

shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register becomes 1010 again?



- (A) 3 (B) 7
 (C) 11 (D) 15

Q.12 Choose the correct one from among the alternatives A, B, C, D after matching an item from Group 1 with the most appropriate item in Group 2.

Group 1

P : Shift register

Group 2

1 : Frequency

Division

Q : Counter

2 : Addressing in
memory chips

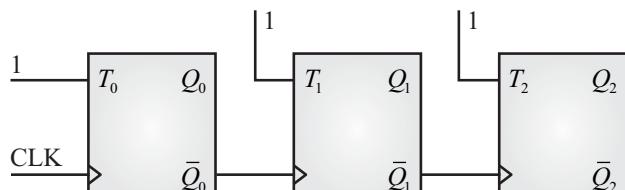
R : Decoder

3 : Serial to
parallel data
conversion

Codes : P Q R

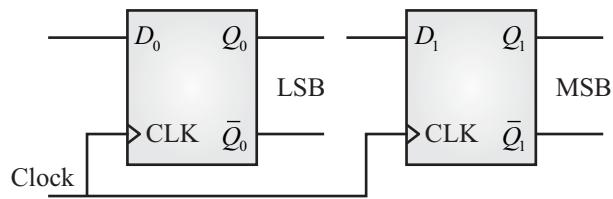
- (A) 3 2 1
 (B) 3 1 2
 (C) 2 1 3
 (D) 1 3 2

Q.13 The given figure shows a ripple counter using positive edge triggered Flip-Flops. If the present state of the counter is $Q_2Q_1Q_0 = 011$ then its next state $Q_2Q_1Q_0$ will be



- (A) 010 (B) 100
 (C) 111 (D) 101

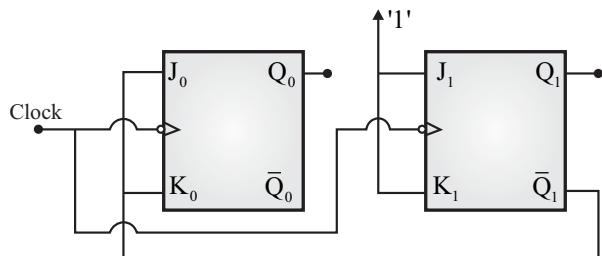
Q.14 Two D flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$



The inputs D_0 and D_1 respectively should be connected as

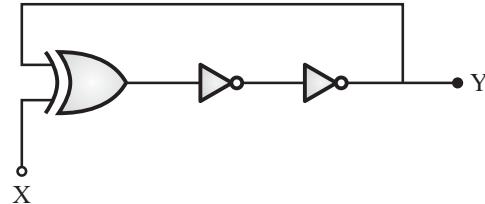
- (A) \bar{Q}_1 and Q_0 (B) \bar{Q}_0 and Q_1
 (C) \bar{Q}_1Q_0 and \bar{Q}_1Q_0 (D) $\bar{Q}_1\bar{Q}_0$ and Q_1Q_0

Q.15 Given that the initial state (Q_1Q_0) is 00, the counting sequence of the counter shown in the following figure for, Q_1Q_0 is



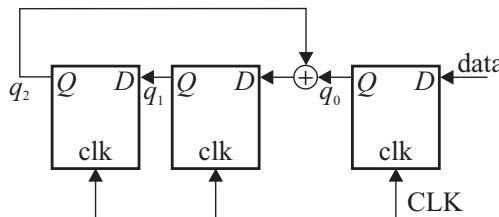
- (A) 00 – 11 – 01 – 10 – 00
 (B) 00 – 01 – 11 – 10 – 00
 (C) 00 – 11 – 10 – 01 – 00
 (D) 00 – 10 – 01 – 11 – 00

Q.16 All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



- (A) X = 0 (B) X = 1
 (C) X = 0 or 1 (D) X = Y

Q.17 Consider the circuit in the diagram. The \oplus operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).

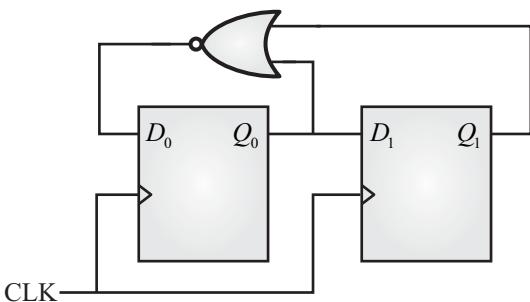


The following data: 100110000 is supplied to the “data” terminal in nine clock cycles.

After that the values of $q_2 q_1 q_0$ are

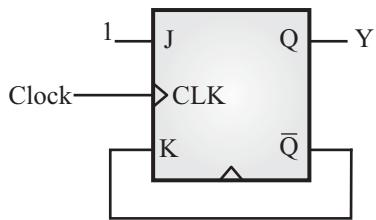
- | | |
|---------|---------|
| (A) 000 | (B) 001 |
| (C) 010 | (D) 101 |

- Q.18** For the circuit shown, the counter state ($Q_1 Q_0$) follows the sequence



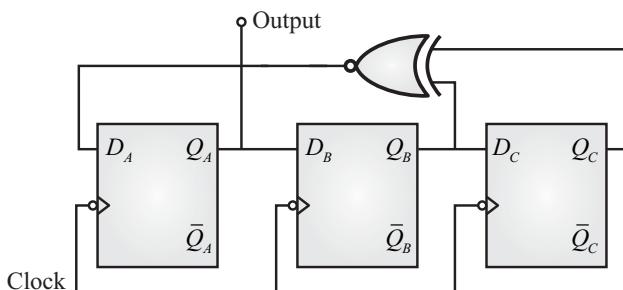
- | |
|----------------------------|
| (A) 00, 01, 10, 11, 00 ... |
| (B) 00, 01, 10, 00, 01 ... |
| (C) 00, 01, 11, 00, 01 ... |
| (D) 00, 10, 11, 00, 10 ... |

- Q.19** In the figure shown, the initial state Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is



- | | |
|-------------|-------------|
| (A) 0000... | (B) 1010... |
| (C) 1111... | (D) 1000... |

- Q.20** Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is

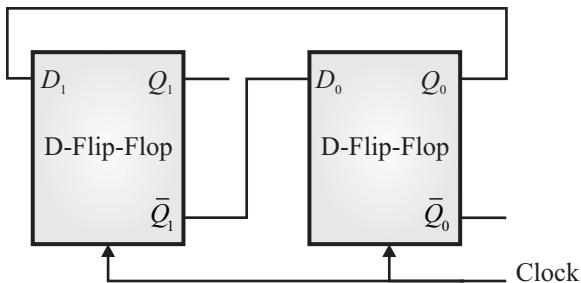


- | | |
|----------------|----------------|
| (A) 0010111... | (B) 0001011... |
| (C) 0101111... | (D) 0110100... |

- Q.21** The minimum number of D flip-flops needed to design a mod-258 counter is

- | | |
|---------|---------|
| (A) 9 | (B) 8 |
| (C) 512 | (D) 258 |

- Q.22** The digital circuit shown below uses two negative edge-triggered D-flip-flops. Assuming initial condition of Q_1 and Q_0 as zero, the output $Q_1 Q_0$ of this circuit is

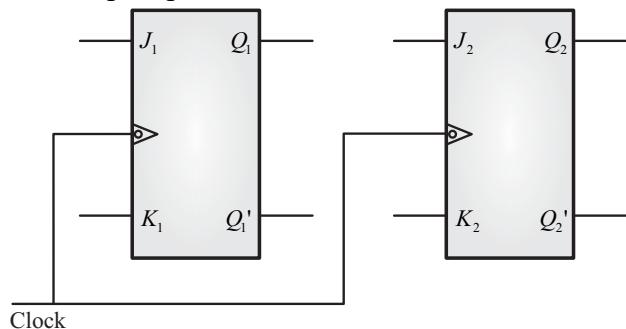


- | |
|----------------------------|
| (A) 00, 01, 10, 11, 00 ... |
| (B) 00, 01, 11, 10, 00 ... |
| (C) 00, 11, 10, 01, 00... |
| (D) 00, 01, 11, 11, 00 ... |

- Q.23** Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

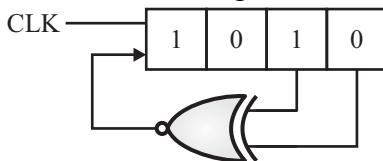
- | |
|-------------------------------------|
| (A) 0, 1, 3, 7, 15, 14, 12, 8, 0 |
| (B) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0 |
| (C) 0, 2, 4, 6, 8, 10, 12, 14, 0 |
| (C) 0, 8, 12, 14, 15, 7, 3, 1, 0 |

- Q.24** A synchronous counter using two $J - K$ flip flops that goes through the sequence of states : $Q_1 Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$ is required. To achieve this, the inputs to the flip flops are

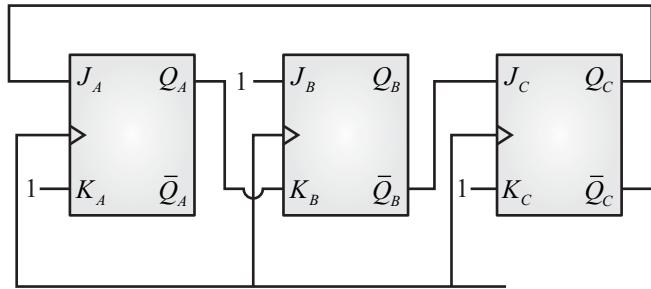


- | |
|---|
| (A) $J_1 = Q_2$, $K_1 = 0$; $J_2 = Q_1'$, $K_2 = Q_1$ |
| (B) $J_1 = 1$, $K_1 = 1$; $J_2 = Q_1$, $K_2 = Q_1$ |
| (C) $J_1 = Q_2$, $K_1 = Q_2'$; $J_2 = Q_2$, $K_2 = 1$ |
| (D) $J_1 = Q_2'$, $K_1 = Q_2$; $J_2 = Q_21'$, $K_2 = Q_1'$ |

- Q.25** The initial contents of the 4 bit serial-in parallel out right shift register shown below, is 1010. After 6 clock pulses are applied, the content of the shift register will be _____.



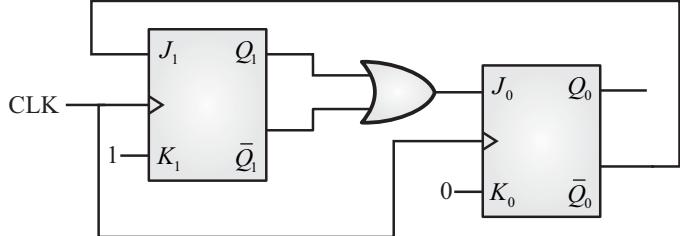
- Q.26** Consider the circuit shown below. The sequence of $Q_A Q_B Q_C$ after 4th clock pulse is [Initially $Q_A Q_B Q_C = 000$]



- (A) 010 (B) 101
(C) 011 (D) 110

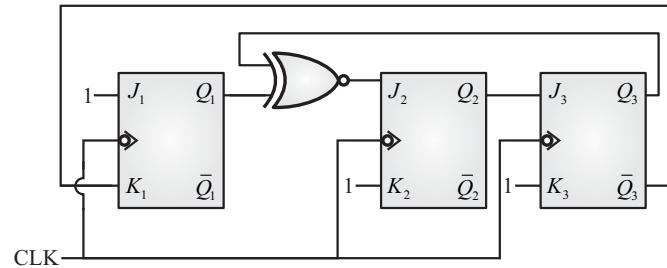
- Q.27** A flip-flop has a delay of 10 n sec. The clock edge applied to the time the output is obtained. There is a mod-10 ripple counter that uses this type of flip-flops. The maximum delay in output is _____ n sec.

- Q.28** Consider the below edge triggered JK flip-flops, Present output at $Q_1 Q_0$ is 00, The output for next 3 clocks is



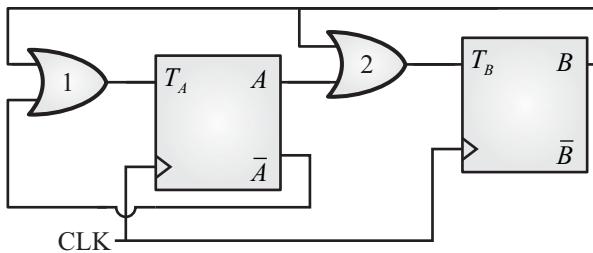
- (A) 11, 01, 01 (B) 11, 01, 10
(C) 11, 10, 01 (D) 11, 11, 11

- Q.29** Consider the circuit shown below. If all the flip-flops are initially cleared then the count ($Q_1 Q_2 Q_3$) after 114 clock pulses is?



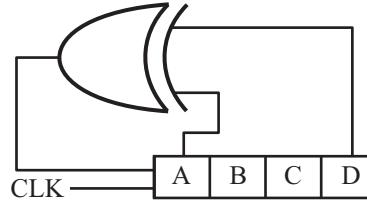
- (A) 000 (B) 110
(C) 101 (D) 001

- Q.30** Determine the counting sequence AB of the following counter



- (A) 00, 01, 10, 11, 00
(B) 00, 01, 10, 00
(C) 00, 10, 11, 00
(D) 00, 10, 01, 11, 00

- Q.31** A 4- bit shift register circuit configured for right shift operation is shown below. If the present state of the shift register is ABCD = 1000, the number of pulses required to reach the state ABCD = 1111 is



- (A) 2 (B) 3
(C) 4 (D) 5

- Q.32** On the third clock pulse a 4- bit johnson sequence is 1110 at Q_0, Q_1, Q_2, Q_3 , what will be the initial sequence of the register.

- (A) 1000 (B) 0001
(C) 1110 (D) 0011

- Q.33** Identify the characteristic equation of X-Y flip flop whose truth table is given

X	Y	$Q(n+1)$
0	0	0
0	1	\bar{Q}_0
1	0	Q_n
1	1	1

- (A) $XY\bar{Q}$ (B) $XY + X\bar{Q}$
(C) $XQ + Y\bar{Q}$ (D) $XY + XQ + YQ$



Answer Keys

Classroom Practice Type Questions									
Flip-Flops									
1.	C	2.	C	3.	A	4.	A	5.	A
6.	C	7.	A	8.	B	9.	B	10.	D
11.	B	12.	C	13.	D	14.	D		
Synchronous Counter									
1.	D	2.	D	3.	B	4.	B	5.	A
6.	C	7.	A	8.	A	9.	B	10.	B
11.	C	12.	D	13.	D	14.	C	15.	C
16.	D	17.	B	18.	D	19.	D	20.	D
21.	A	22.	C	23.	4	24.	C		
Miscellaneous Questions (FF & Counters)									
10.	A								
11.	3	12.	4	13.	2	14.	A	15.	D
16.	C	17.	A	18.	A	19.	B	20.	A
Shift Registers									
1.	C	2.	D	3.	6	4.	1.5	5.	B
7.	C	8.	A						
Self-Practice Questions									
1.	C	2.	D	3.	B	4.	D	5.	C
6.	A	7.	10	8.	D	9.	A	10.	B
11.	B	12.	B	13.	B	14.	A	15.	A
16.	B	17.	C	18.	B	19.	C	20.	D
21.	D	22.	B	23.	C	24.	B	25.	1100
26.	B	27.	38 – 42	28.	A	29.	4	30.	3
31.	3	32.	D	33.	C				

Space for Rough Work